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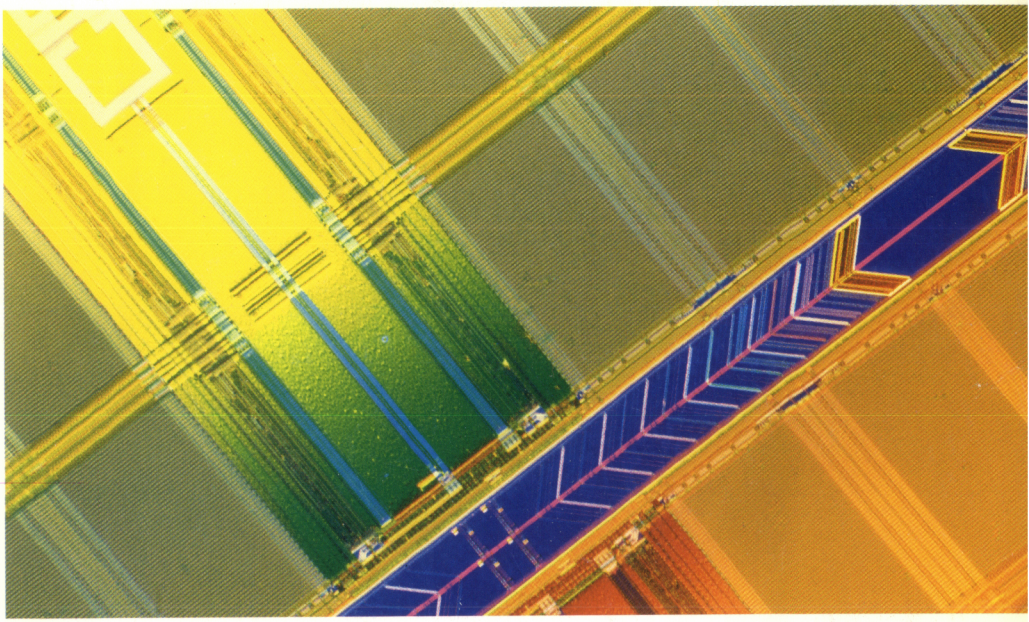

Memory Components

Data Book 06.95

Edition 06/95

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Introduction

The DRAM market is truly dynamic. It is difficult to keep pace with the increasing spectrum of available organisations, refresh modes, packages and application specific features, such as 'Burst' and 'Extended Data Out', that seem to be flooding the market place. One trend is for sure; the DRAM can no longer be considered as a 'commodity product' but is diversifying into an 'application specific commodity product'.

One good example of an application segment demanding specific DRAM features is the portable computer market. To serve this market a low power consuming, space saving device is needed which means 3.3 V supply voltage, long retention (t_{ref} = 256 ms) and a TSOP package. In the PC market, the requirements of the 'Green PC' is pushing in this direction but on the whole we believe it will take some time until the conventional desktop-PC switches over to using 3.3 V and TSOP. With the increasing presence of the 64 M bit DRAM in the market place, only offered as a 3.3 V part, the cut between 5 V and 3.3 V will have to be made.

Another good example of application specific features is the DRAM in the graphics environment. Here is the bandwidth available from a device of upmost importance. A shallow depth, wide organisation is most suitable for this application. The 256K×4 and 256K×16 are most suitable. Details of these products can be found in the data book. Furthermore, the introduction of the Extended Data Out feature and its extention to the Burst-mode has been the answer to many a graphic's designer's prayer. Please contact your nearest sales office for further information on this product.

The drive to higher system performance and memory consumption in workstations and PCs is unsatiable. Two new range of products have been included in our program this year to meet these needs: As the clock rates of all microprocessor based systems are constantly increasing, the memory subsystems have been struggling to keep pace. Therefore, SIEMENS has introduced the 50 ns speed category for most of the DRAM products. The Extended Data Out mode, for main memory applications, seems to have come out of the blue to also solve this problems. This new feature is included in our program in the 16 M generation for all organisations and we believe will be a 'hot'-product in 1995/96. Furthermore, the need for more and more MBytes of main memory can be met with the newest generation product, 64 Mbit, currently available in ×4, ×8, ×16 organisations. A memory configuration of 32 MByte can be realized with only 4 pieces of the 4M×16 (64 bit data path) compared to 16 pieces of 1M×16.

For the upcoming 64 bit wide buses in PC's SIEMENS has available a new family of DRAM modules - the 168 pin DIMM modules in 1M×64 and 1M×72 bit organisations.

Summary of Types (incl. ordering codes)

Summary of Types

Type	Ordering Code	Package	Description DRAM	Page
Memory Components				
HYB 511000BJ-50	Q67100-Q1056	P-SOJ-26/20-1 300 mil	1 M × 1, 50 ns	33
HYB 511000BJ-60	Q67100-Q518	P-SOJ-26/20-1 300 mil	1 M × 1, 60 ns	33
HYB 511000BJ-70	Q67100-Q519	P-SOJ-26/20-1 300 mil	1 M × 1, 70 ns	33
HYB 511000BJL-50	on request	P-SOJ-26/20-1 300 mil	1 M × 1, Lp, 50 ns	33
HYB 511000BJL-60	Q67100-Q526	P-SOJ-26/20-1 300 mil	1 M × 1, Lp, 60 ns	33
HYB 511000BJL-70	Q67100-Q527	P-SOJ-26/20-1 300 mil	1 M × 1, Lp, 70 ns	33
HYB 514256B-50	Q67100-Q1044	P-DIP-20-2 300 mil	256 k × 4, 50 ns	55
HYB 514256B-60	Q67100-Q530	P-DIP-20-2 300 mil	256 k × 4, 60 ns	55
HYB 514256B-70	Q67100-Q433	P-DIP-20-2 300 mil	256 k × 4, 70 ns	55
HYB 514256BJ-50	Q67100-Q1054	P-SOJ-26/20-1 300 mil	256 k × 4, 50 ns	55
HYB 514256BJ-60	Q67100-Q536	P-SOJ-26/20-1 300 mil	256 k × 4, 60 ns	55
HYB 514256BJ-70	Q67100-Q537	P-SOJ-26/20-1 300 mil	256 k × 4, 70 ns	55
HYB 514256BL-50	on request	P-DIP-20-2 300 mil	256 k × 4, Lp, 50 ns	55
HYB 514256BL-60	Q67100-Q542	P-DIP-20-2 300 mil	256 k × 4, Lp, 60 ns	55
HYB 514256BL-70	Q67100-Q543	P-DIP-20-2 300 mil	256 k × 4, Lp, 70 ns	55
HYB 514256BJL-50	on request	P-SOJ-26/20-1 300 mil	256 k × 4, Lp, 50 ns	55
HYB 514256BJL-60	Q67100-Q608	P-SOJ-26/20-1 300 mil	256 k × 4, Lp, 60 ns	55
HYB 514256BJL-70	Q67100-Q607	P-SOJ-26/20-1 300 mil	256 k × 4, Lp, 70 ns	55
HYB 514100BJ-50	Q67100-Q971	P-SOJ-26/20-5 300 mil	4 M × 1, 50 ns	77
HYB 514100BJ-60	Q67100-Q759	P-SOJ-26/20-5 300 mil	4 M × 1, 60 ns	77
HYB 514100BJ-70	Q67100-Q760	P-SOJ-26/20-5 300 mil	4 M × 1, 70 ns	77
HYB 514100BJL-50	on request	P-SOJ-26/20-5 300 mil	4 M × 1, Lp, 50 ns	77
HYB 514100BJL-60	Q67100-Q1029	P-SOJ-26/20-5 300 mil	4 M × 1, Lp, 60 ns	77
HYB 514100BJL-70	Q67100-Q763	P-SOJ-26/20-5 300 mil	4 M × 1, Lp, 70 ns	77

Lp = Low power
1k = 1 k-refresh
2k = 2 k-refresh
4k = 4 k-refresh
8k = 8 k-refresh

Summary of Types (cont'd)

Type	Ordering Code	Package	Description DRAM	Page
Memory Components				
HYB 514100BT-50	Q67100-Q2011	P-TSOPII-26/20-1 300 mil	4 M × 1, 50 ns	77
HYB 514100BT-60	Q67100-Q746	P-TSOPII-26/20-1 300 mil	4 M × 1, 60 ns	77
HYB 514100BT-70	Q67100-Q747	P-TSOPII-26/20-1 300 mil	4 M × 1, 70 ns	77
HYB 514100BTL-50	on request	P-TSOPII-26/20-1 300 mil	4 M × 1, Lp, 50 ns	77
HYB 514100BTL-60	on request	P-TSOPII-26/20-1 300 mil	4 M × 1, Lp, 60 ns	77
HYB 514100BTL-70	on request	P-TSOPII-26/20-1 300 mil	4 M × 1, Lp, 70 ns	77
HYB 514400BJ-50	Q67100-Q973	P-SOJ-26/20-5 300 mil	1 M × 4, 50 ns	99
HYB 514400BJ-60	Q67100-Q756	P-SOJ-26/20-5 300 mil	1 M × 4, 60 ns	99
HYB 514400BJ-70	Q67100-Q757	P-SOJ-26/20-5 300 mil	1 M × 4, 70 ns	99
HYB 514400BJL-50	Q67100-Q2012	P-SOJ-26/20-5 300 mil	1 M × 4, Lp, 50 ns	99
HYB 514400BJL-60	Q67100-Q1030	P-SOJ-26/20-5 300 mil	1 M × 4, Lp, 60 ns	99
HYB 514400BJL-70	Q67100-Q762	P-SOJ-26/20-5 300 mil	1 M × 4, Lp, 70 ns	99
HYB 514400BT-50	Q67100-Q2013	P-TSOPII-26/20-1 300 mil	1 M × 4, 50 ns	99
HYB 514400BT-60	Q67100-Q749	P-TSOPII-26/20-1 300 mil	1 M × 4, 60 ns	99
HYB 514400BT-70	Q67100-Q750	P-TSOPII-26/20-1 300 mil	1 M × 4, 70 ns	99
HYB 514400BTL-50	on request	P-TSOPII-26/20-1 300 mil	1 M × 4, Lp, 50 ns	99
HYB 514400BTL-60	on request	P-TSOPII-26/20-1 300 mil	1 M × 4, Lp, 60 ns	99
HYB 514400BTL-70	on request	P-TSOPII-26/20-1 300 mil	1 M × 4, Lp, 70 ns	99
HYB 514800BJ-60	Q67100-Q849	P-SOJ-28-2 400 mil	512 k × 8, 60 ns	125
HYB 514800BJ-70	Q67100-Q850	P-SOJ-28-2 400 mil	512 k × 8, 70 ns	125
HYB 514800BJ-80	Q67100-Q851	P-SOJ-28-2 400 mil	512 k × 8, 80 ns	125
HYB 514171BJ-60	Q67100-Q727	P-SOJ-40-1 400 mil	256 k × 16, 60 ns	147
HYB 514171BJ-70	Q67100-Q728	P-SOJ-40-1 400 mil	256 k × 16, 70 ns	147
HYB 514171BJL-60	Q67100-Q932	P-SOJ-40-1 400 mil	256 k × 16, Lp, 60 ns	147
HYB 514171BJL-70	Q67100-Q931	P-SOJ-40-1 400 mil	256 k × 16, Lp, 70 ns	147

Lp = Low power
1k = 1 k-refresh
2k = 2 k-refresh
4k = 4 k-refresh
8k = 8 k-refresh

Summary of Types (cont'd)

Type	Ordering Code	Package	Description DRAM	Page
Memory Components				
HYB 5116400BJ-50	Q67100-Q1049	P-SOJ-26/24-1 300 mil	4 M × 4, 4k, 50 ns	171
HYB 5116400BJ-60	Q67100-Q1050	P-SOJ-26/24-1 300 mil	4 M × 4, 4k, 60 ns	171
HYB 5116400BJ-70	Q67100-Q1051	P-SOJ-26/24-1 300 mil	4 M × 4, 4k, 70 ns	171
HYB 3116400BJ-50	on request	P-SOJ-26/24-1 300 mil	4 M × 4, 4k, 3.3 V, 50 ns	223
HYB 3116400BJ-60	on request	P-SOJ-26/24-1 300 mil	4 M × 4, 4k, 3.3 V, 60 ns	223
HYB 3116400BJ-70	on request	P-SOJ-26/24-1 300 mil	4 M × 4, 4k, 3.3 V, 70 ns	223
HYB 5116405BJ-50	Q67100-Q1098	P-SOJ-26/24-1 300 mil	4 M × 4, 4k, EDO, 50 ns	275
HYB 5116405BJ-60	Q67100-Q1099	P-SOJ-26/24-1 300 mil	4 M × 4, 4k, EDO, 60 ns	275
HYB 5116405BJ-70	Q67100-Q1100	P-SOJ-26/24-1 300 mil	4 M × 4, 4k, EDO, 70 ns	275
HYB 5116400BT-50	on request	P-TSOPII-26/24-1 300 mil	4 M × 4, 4k, 50 ns	171
HYB 5116400BT-60	on request	P-TSOPII-26/24-1 300 mil	4 M × 4, 4k, 60 ns	171
HYB 5116400BT-70	on request	P-TSOPII-26/24-1 300 mil	4 M × 4, 4k, 70 ns	171
HYB 3116400BT-50	on request	P-TSOPII-26/24-1 300 mil	4 M × 4, 4k, 3.3 V, 50 ns	223
HYB 3116400BT-60	on request	P-TSOPII-26/24-1 300 mil	4 M × 4, 4k, 3.3 V, 60 ns	223
HYB 3116400BT-70	on request	P-TSOPII-26/24-1 300 mil	4 M × 4, 4k, 3.3 V, 70 ns	223
HYB 5116405BT-50	on request	P-TSOPII-26/24-1 300 mil	4 M × 4, 4k, EDO, 50 ns	275
HYB 5116405BT-60	on request	P-TSOPII-26/24-1 300 mil	4 M × 4, 4k, EDO, 60 ns	275
HYB 5116405BT-70	on request	P-TSOPII-26/24-1 300 mil	4 M × 4, 4k, EDO, 70 ns	275
HYB 5117400BJ-50	Q67100-Q1086	P-SOJ-26/24-1 300 mil	4 M × 4, 2k, 50 ns	197
HYB 5117400BJ-60	Q67100-Q1087	P-SOJ-26/24-1 300 mil	4 M × 4, 2k, 60 ns	197
HYB 5117400BJ-70	Q67100-Q1088	P-SOJ-26/24-1 300 mil	4 M × 4, 2k, 70 ns	197
HYB 3117400BT-50	on request	P-TSOPII-26/24-1 300 mil	4 M × 4, 2k, 3.3 V, 50 ns	249
HYB 3117400BT-60	on request	P-TSOPII-26/24-1 300 mil	4 M × 4, 2k, 3.3 V, 60 ns	249
HYB 3117400BT-70	on request	P-TSOPII-26/24-1 300 mil	4 M × 4, 2k, 3.3 V, 70 ns	249

Lp = Low power
1k = 1 k-refresh
2k = 2 k-refresh
4k = 4 k-refresh
8k = 8 k-refresh

Summary of Types (cont'd)

Type	Ordering Code	Package	Description DRAM	Page
Memory Components				
HYB 5117405BJ-50	Q67100-Q1101	P-SOJ-26/24-1 300 mil	4 M × 4, 2k, EDO, 50 ns	275
HYB 5117405BJ-60	Q67100-Q1102	P-SOJ-26/24-1 300 mil	4 M × 4, 2k, EDO, 60 ns	275
HYB 5117405BJ-70	Q67100-Q1103	P-SOJ-26/24-1 300 mil	4 M × 4, 2k, EDO, 70 ns	275
HYB 5117400BT-50	on request	P-TSOPII-26/24-1 300 mil	4 M × 4, 2k, 50 ns	197
HYB 5117400BT-60	on request	P-TSOPII-26/24-1 300 mil	4 M × 4, 2k, 60 ns	197
HYB 5117400BT-70	on request	P-TSOPII-26/24-1 300 mil	4 M × 4, 2k, 70 ns	197
HYB 3117400BJ-50	on request	P-SOJ-26/24-1 300 mil	4 M × 4, 2k, 3.3 V, 50 ns	249
HYB 3117400BJ-60	on request	P-SOJ-26/24-1 300 mil	4 M × 4, 2k, 3.3 V, 60 ns	249
HYB 3117400BJ-70	on request	P-SOJ-26/24-1 300 mil	4 M × 4, 2k, 3.3 V, 70 ns	249
HYB 5117405BT-50	on request	P-TSOPII-26/24-1 300 mil	4 M × 4, 2k, EDO, 50 ns	275
HYB 5117405BT-60	on request	P-TSOPII-26/24-1 300 mil	4 M × 4, 2k, EDO, 60 ns	275
HYB 5117405BT-70	on request	P-TSOPII-26/24-1 300 mil	4 M × 4, 2k, EDO, 70 ns	275
HYB 5117800BSJ-50	Q67100-Q1092	P-SOJ-28-3 400 mil	2 M × 8, 2k, 50 ns	303
HYB 5117800BSJ-60	Q67100-Q1093	P-SOJ-28-3 400 mil	2 M × 8, 2k, 60 ns	303
HYB 5117800BSJ-70	Q67100-Q1094	P-SOJ-28-3 400 mil	2 M × 8, 2k, 70 ns	303
HYB 5117805BJ-50	Q67100-Q1104	P-SOJ-28-3 400 mil	2 M × 8, 2k, EDO, 50 ns	329
HYB 5117805BJ-60	Q67100-Q1105	P-SOJ-28-3 400 mil	2 M × 8, 2k, EDO, 60 ns	329
HYB 5117805BJ-70	Q67100-Q1106	P-SOJ-28-3 400 mil	2 M × 8, 2k, EDO, 70 ns	329
HYB 5118160BSJ-50	Q67100-Q1072	P-SOJ-42-1 400 mil	1 M × 16, 1k, 50 ns	355
HYB 5118160BSJ-60	Q67100-Q1073	P-SOJ-42-1 400 mil	1 M × 16, 1k, 60 ns	355
HYB 5118160BSJ-70	Q67100-Q1074	P-SOJ-42-1 400 mil	1 M × 16, 1k, 70 ns	355
HYB 3118160BSJ-50	on request	P-SOJ-42-1 400 mil	1 M × 16, 1k, 3.3 V, 50 ns	403
HYB 3118160BSJ-60	on request	P-SOJ-42-1 400 mil	1 M × 16, 1k, 3.3 V, 60 ns	403

Lp = Low power
1k = 1 k-refresh
2k = 2 k-refresh
4k = 4 k-refresh
8k = 8 k-refresh

Summary of Types (cont'd)

Type	Ordering Code	Package	Description DRAM	Page
Memory Components				
HYB 3118160BSJ-70	on request	P-SOJ-42-1 400 mil	1 M × 16, 1k, 3.3 V, 70 ns	403
HYB 5118165BSJ-50	Q67100-Q1107	P-SOJ-42-1 400 mil	1 M × 16, 1k, EDO, 50 ns	429
HYB 5118165BSJ-60	Q67100-Q1108	P-SOJ-42-1 400 mil	1 M × 16, 1k, EDO, 60 ns	429
HYB 5118165BSJ-70	Q67100-Q1109	P-SOJ-42-1 400 mil	1 M × 16, 1k, EDO, 70 ns	429
HYB 5116160BSJ-50	on request	P-SOJ-42-1 400 mil	1 M × 16, 4k, 50 ns	379
HYB 5116160BSJ-60	on request	P-SOJ-42-1 400 mil	1 M × 16, 4k, 60 ns	379
HYB 5116160BSJ-70	on request	P-SOJ-42-1 400 mil	1 M × 16, 4k, 70 ns	379
HYB 3116160BSJ-50	on request	P-SOJ-42-1 400 mil	1 M × 16, 4k, 3.3 V, 50 ns	403
HYB 3116160BSJ-60	on request	P-SOJ-42-1 400 mil	1 M × 16, 4k, 3.3 V, 60 ns	403
HYB 3116160BSJ-70	on request	P-SOJ-42-1 400 mil	1 M × 16, 4k, 3.3 V, 70 ns	403
HYB 5116165BSJ-50	on request	P-SOJ-42-1 400 mil	1 M × 16, 4k, EDO, 50 ns	429
HYB 5116165BSJ-60	on request	P-SOJ-42-1 400 mil	1 M × 16, 4k, EDO, 60 ns	429
HYB 5116165BSJ-70	on request	P-SOJ-42-1 400 mil	1 M × 16, 4k, EDO, 70 ns	429
HYB 3164160T-50	on request	P-TSOPII-54-1 500 mil	4 M × 16, 8k, 3.3 V, 50 ns	511
HYB 3164160T-60	on request	P-TSOPII-54-1 500 mil	4 M × 16, 8k, 3.3 V, 60 ns	511
HYB 3165160T-50	on request	P-TSOPII-54-1 500 mil	4 M × 16, 4k, 3.3 V, 50 ns	511
HYB 3165160T-60	on request	P-TSOPII-54-1 500 mil	4 M × 16, 4k, 3.3 V, 60 ns	511

Lp = Low power
1k = 1 k-refresh
2k = 2 k-refresh
4k = 4 k-refresh
8k = 8 k-refresh

Summary of Types (cont'd)

Type	Ordering Code	Package	Description DRAM	Page
Memory Components				
HYB 3164800J-50	on request	P-SOJ-34-1 500 mil	8 M × 8, 8k, 3.3 V, 50 ns	483
HYB 3164800J-60	on request	P-SOJ-34-1 500 mil	8 M × 8, 8k, 3.3 V, 60 ns	483
HYB 3164800T-50	on request	P-TSOPII-34-1 500 mil	8 M × 8, 8k, 3.3 V, 50 ns	483
HYB 3164800T-60	on request	P-TSOPII-34-1 500 mil	8 M × 8, 8k, 3.3 V, 60 ns	483
HYB 3165800J-50	on request	P-SOJ-34-1 500 mil	8 M × 8, 4k, 3.3 V, 50 ns	483
HYB 3165800J-60	on request	P-SOJ-34-1 500 mil	8 M × 8, 4k, 3.3 V, 60 ns	483
HYB 3165800T-50	on request	P-TSOPII-34-1 500 mil	8 M × 8, 4k, 3.3 V, 50 ns	483
HYB 3165800T-60	on request	P-TSOPII-34-1 500 mil	8 M × 8, 4k, 3.3 V, 60 ns	483
HYB 3164400J-50	on request	P-SOJ-34-1 500 mil	16 M × 4, 8k, 3.3 V, 50 ns	455
HYB 3164400J-60	on request	P-SOJ-34-1 500 mil	16 M × 4, 8k, 3.3 V, 60 ns	455
HYB 3164400T-50	on request	P-TSOPII-34-1 500 mil	16 M × 4, 8k, 3.3 V, 50 ns	455
HYB 3164400T-60	on request	P-TSOPII-34-1 500 mil	16 M × 4, 8k, 3.3 V, 60 ns	455
HYB 3165400J-50	on request	P-SOJ-34-1 500 mil	16 M × 4, 4k, 3.3 V, 50 ns	455
HYB 3165400J-60	on request	P-SOJ-34-1 500 mil	16 M × 4, 4k, 3.3 V, 60 ns	455
HYB 3165400T-50	on request	P-TSOPII-34-1 500 mil	16 M × 4, 4k, 3.3 V, 50 ns	455
HYB 3165400T-50	on request	P-TSOPII-34-1 500 mil	16 M × 4, 4k, 3.3 V, 60 ns	455

Lp = Low power
1k = 1 k-refresh
2k = 2 k-refresh
4k = 4 k-refresh
8k = 8 k-refresh

= SMD

Summary of Types

Type	Ordering Code	Package	Description	Page
Memory Modules				
HYM 321160S-60	Q67100-Q2010	L-SIM-72-11	60 ns 1 M × 32 Module	541
HYM 321160S-70	on request	L-SIM-72-11	70 ns 1 M × 32 Module	541
HYM 321160GS-60	Q67100-Q2009	L-SIM-72-11	60 ns 1 M × 32 Module	541
HYM 321160GS-70	on request	L-SIM-72-11	70 ns 1 M × 32 Module	541
HYM 322030S-60	Q67100-Q976	L-SIM-72-9	60 ns 2 M × 32 Module	561
HYM 322030S-70	Q67100-Q977	L-SIM-72-9	70 ns 2 M × 32 Module	561
HYM 322030GS-60	Q67100-Q2018	L-SIM-72-9	60 ns 2 M × 32 Module	561
HYM 322030GS-70	Q67100-Q2019	L-SIM-72-9	70 ns 2 M × 32 Module	561
HYM 322160S-60	Q67100-Q2014	L-SIM-72-11	60 ns 2 M × 32 Module	551
HYM 322160S-70	Q67100-Q2015	L-SIM-72-11	70 ns 2 M × 32 Module	551
HYM 322160GS-60	Q67100-Q2016	L-SIM-72-11	60 ns 2 M × 32 Module	551
HYM 322160GS-70	Q67100-Q2017	L-SIM-72-11	70 ns 2 M × 32 Module	551
HYM 324020S-60	Q67100-Q979	L-SIM-72-12	60 ns 4 M × 32 Module	571
HYM 324020S-70	Q67100-Q980	L-SIM-72-12	70 ns 4 M × 32 Module	571
HYM 324020GS-60	Q67100-Q2005	L-SIM-72-12	60 ns 4 M × 32 Module	571
HYM 324020GS-70	on request	L-SIM-72-12	70 ns 4 M × 32 Module	571
HYM 328020S-60	Q67100-Q2001	L-SIM-72-15	60 ns 8 M × 32 Module	581
HYM 328020S-70	on request	L-SIM-72-15	70 ns 8 M × 32 Module	581
HYM 328020GS-60	Q67100-Q2008	L-SIM-72-15	60 ns 8 M × 32 Module	581
HYM 328020GS-70	on request	L-SIM-72-15	70 ns 8 M × 32 Module	581
HYM 361120S-60	Q67100-Q942	L-SIM-72-3	60 ns 1 M × 36 Module	591
HYM 361120S-70	Q67100-Q741	L-SIM-72-3	70 ns 1 M × 36 Module	591
HYM 361140S-60	Q67100-Q959	L-SIM-72-8	60 ns 1 M × 36 Module	591
HYM 361140S-70	Q67100-Q958	L-SIM-72-8	70 ns 1 M × 36 Module	591
HYM 361120GS-60	Q67100-Q961	L-SIM-72-3	60 ns 1 M × 36 Module	591
HYM 361120GS-70	Q67100-Q960	L-SIM-72-3	70 ns 1 M × 36 Module	591
HYM 361140GS-60	Q67100-Q1019	L-SIM-72-8	60 ns 1 M × 36 Module	591
HYM 361140GS-70	Q67100-Q651	L-SIM-72-8	70 ns 1 M × 36 Module	591
HYM 362140S-60	Q67100-Q955	L-SIM-72-8	60 ns 2 M × 36 Module	601
HYM 362140S-70	Q67100-Q954	L-SIM-72-8	70 ns 2 M × 36 Module	601
HYM 362140GS-60	Q67100-Q957	L-SIM-72-8	60 ns 2 M × 36 Module	601

Summary of Types (cont'd)

Type	Ordering Code	Package	Description	Page
Memory Modules				
HYM 362140GS-70	Q67100-Q956	L-SIM-72-8	70 ns 2 M × 36 Module	601
HYM 364020S-60	Q67100-Q2006	L-SIM-72-12	60 ns 4 M × 36 Module	611
HYM 364020S-70	on request	L-SIM-72-12	70 ns 4 M × 36 Module	611
HYM 364020GS-60	Q67100-Q982	L-SIM-72-12	60 ns 4 M × 36 Module	611
HYM 364020GS-70	Q67100-Q983	L-SIM-72-12	70 ns 4 M × 36 Module	611
HYM 368020S-60	Q67100-Q985	L-SIM-72-14	60 ns 8 M × 36 Module	621
HYM 368020S-70	Q67100-Q986	L-SIM-72-14	70 ns 8 M × 36 Module	621
HYM 368020GS-60	Q67100-Q2007	L-SIM-72-14	60 ns 8 M × 36 Module	621
HYM 368020GS-70	on request	L-SIM-72-14	70 ns 8 M × 36 Module	621
HYM 641020GS-60	Q67100-Q2003	L-DIM-168-1	60 ns 1 M × 64 Module	631
HYM 641020GS-70	on request	L-DIM-168-1	70 ns 1 M × 64 Module	631
HYM 641010GS-60	Q67100-Q2002	L-DIM-168-1	60 ns 1 M × 64 Module	631
HYM 641010GS-70	on request	L-DIM-168-1	70 ns 1 M × 64 Module	631
HYM 721000GS-60	Q67100-Q2004	L-DIM-168-2	60 ns 1 M × 72 Module	641
HYM 721000GS-70	on request	L-DIM-168-2	70 ns 1 M × 72 Module	641

Packing Information
Product View
Number Guide

DRAMS in Tape & Reel

Package Type	Device Type	Devices Per Reel	Tape Width
P-SOJ-26/20-1[1)]	HYB 511000BJ HYB 514256BJ	1500	24 mm
P-SOJ-26/20-5[2)]	HYB 514100BJ HYB 514400BJ	1500	24 mm
P-SOJ-28-2	HYB 514800BJ	1000	24 mm
P-SOJ-40-1	HYB 514171BJ	900	44 mm
P-TSOPII-26/20-1	HYB 514100BT HYB 514400BT	3000	24 mm
P-SOJ-26/24-1	HYB 5116400(5)BJ HYB 5117400(5)BJ HYB 3116400BJ HYB 3117400BJ	1500	24 mm
P-TSOPII-26/24-1	HYB 5116400(5)BT HYB 5117400(5)BT HYB 3116400BT HYB 3117400BT	3000	24 mm
P-SOJ-28-3	HYB 5117800BSJ HYB 5116805BSJ	1000	24 mm
P-SOJ-42-1	HYB 5116160(5)BSJ HYB 5118160(5)BSJ HYB 3116160BSJ HYB 3118160BSJ	1000	44 mm
P-SOJ-34-1	HYB 3164400J HYB 3165400J HYB 3164800J HYB 3165800J	on request	on request
P-TSOPII-34-1	HYB 3164400T HYB 3165400T HYB 3164800T HYB 3165800T	on request	on request
P-TSOP-54-1	HYB 3164160T HYB 3165160T	on request	on request

Notes see page 23.

DRAMS in Tubes and Boxes

Package Type	Device Type	Type of Tube	Devices per Tube	Tubes per Container	Devices per Container
P-DIP-20-2	HYB 514256BJ	volume conductive	20	40	800
P-SOJ-26/20-1 *)2)3)	HYB 511000BJ HYB 514256BJ	antistatic	25	100	2500
P-SOJ-26/20-5*)	HYB 514100BJ HYB 514400BJ	volume conductive	25	40	1000
P-SOJ-28-2*)	HYB 514800BJ	antistatic	27	50	1350
P-SOJ-40-1*)	HYB 514171BJ	antistatic	18	50	950
P-SOJ-26/24-1*)	HYB 5116400(5)BJ HYB 5117400(5)BJ HYB 3116400BJ HYB 3117400BJ	volume conductive	25	40	1000
P-SOJ-28-3*)	HYB 5117800BSJ HYB 5116805BSJ	volume conductive	27	50	1350
P-SOJ-42-1*)	HYB 5116160(5)BSJ HYB 5118160(5)BSJ HYB 3116160BSJ HYB 3118160BSJ	volume conductive	18	50	900
P-SOJ-34-1	HYB 3164400J HYB 3165400J HYB 3164800J HYB 3165800J	on request	on request		
P-TSOPII-34-1	HYB 3164400T HYB 3165400T HYB 3164800T HYB 3165800T	on request	on request		
P-TSOP-54-1	HYB 3164160T HYB 3165160T	on request	on request		

Notes see page 23.

DRAM Modules

Type	Packing	small	big
L-SIM-72-3	Trays Trays	40 1	80 1
L-SIM-72-8	Trays Trays	40 1	80 1
L-SIM-72-9	Trays Trays	40 1	80 1
L-SIM-72-11	Trays Trays	40 1	80 1
L-SIM-72-12	Trays Trays	40 1	80 1

Type	Packing	small	big
L-SIM-72-14	Trays Trays	20 1	40 1
L-SIM-72-15	Trays Trays	20 1	40 1
L-SIM-168-1	Trays Trays	40 1	80 1
L-SIM-168-2	Trays Trays	40 1	80 1

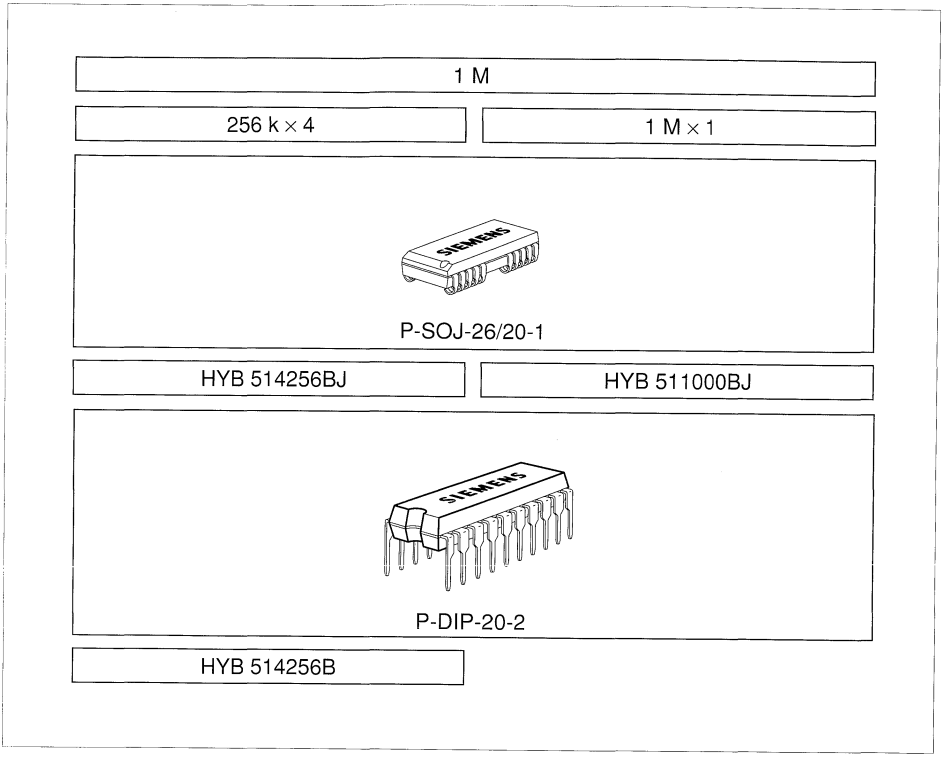
*) The ordering codes stated for DRAMs in these packages apply to tape and reel format. For further details of packing, refer to the data book "Semiconductor Package Information".

1) Dry packing on special request.

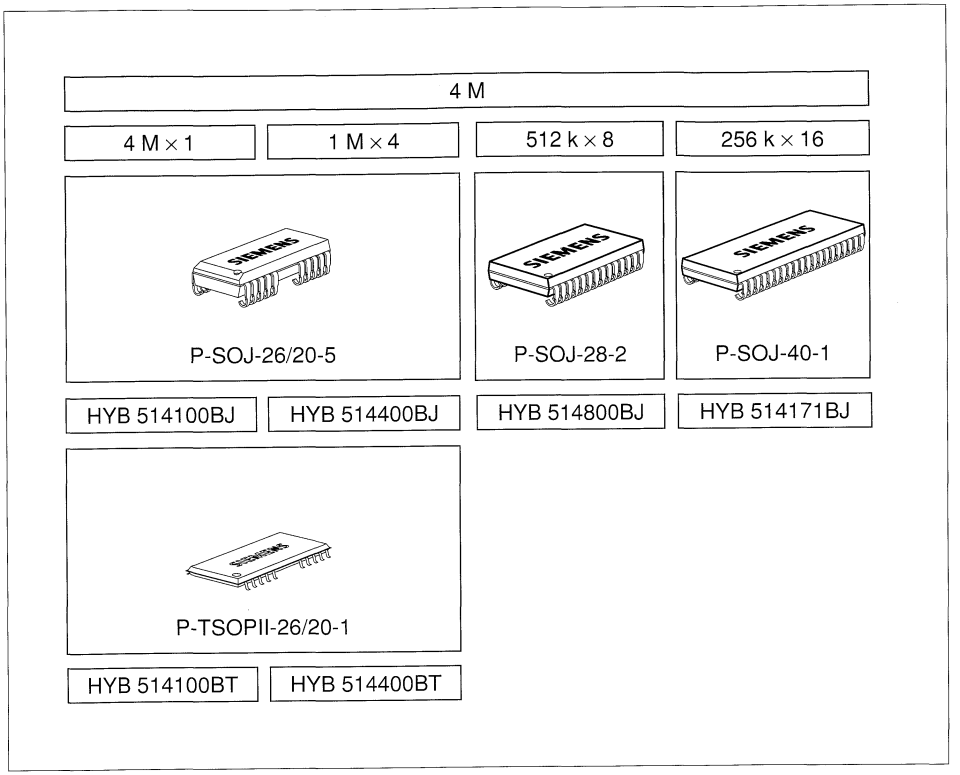
2) None dry packing on special request.

3) Dry packing on special request, VPE 25/1000.

1 M Product View

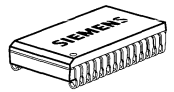
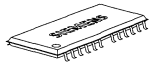


4 M Product View

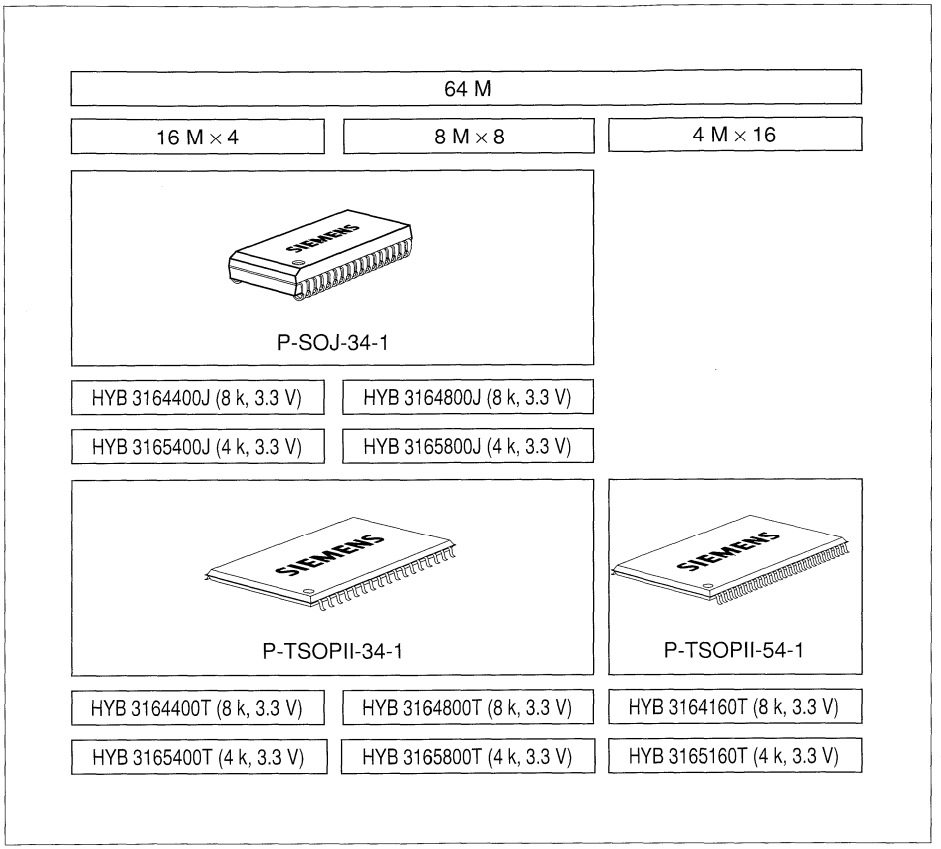


16 M Product View

16 M

4 M × 4	2 M × 8	1 M × 16
 P-SOJ-26/24-1	 P-SOJ-28-3	 P-SOJ-42-1
HYB 5116400BJ (4 k, 5 V)	HYB 5117800BSJ (2 k, 5 V)	HYB 5118160BSJ (1 k, 5 V)
HYB 5117400BJ (2 k, 5 V)	HYB 5117805BSJ (2 k, 5 V, EDO)	HYB 5116160BSJ (4 k, 5 V)
HYB 5116405BJ (4 k, 5V, EDO)		HYB 5116165BSJ (4 k, 5V, EDO)
HYB 5117405BJ (2 k, 5V, EDO)		HYB 5118165BSJ (1 k, 5V, EDO)
HYB 3116400BJ (4 k, 3.3V)		HYB 3116160BSJ (4 k, 3.3V)
HYB 3117400BJ (2 k, 3.3V)		HYB 3118160BSJ (1 k, 3.3V)
 P-TSOPII-26/24-1		
HYB 5116400BT (4 k, 5 V)		
HYB 5117400BT (2 k, 5 V)		
HYB 5116405BT (4 k, 5 V, EDO)		
HYB 5117405BT (2 k, 5 V, EDO)		
HYB 3116400BT (4 k, 3.3V)		
HYB 3117400BT (2 k, 3.3V)		

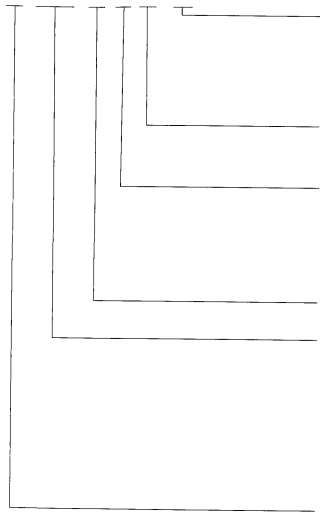
64 M Product View



Memory Components

Memory Components (1 M & 4 M DRAMS)

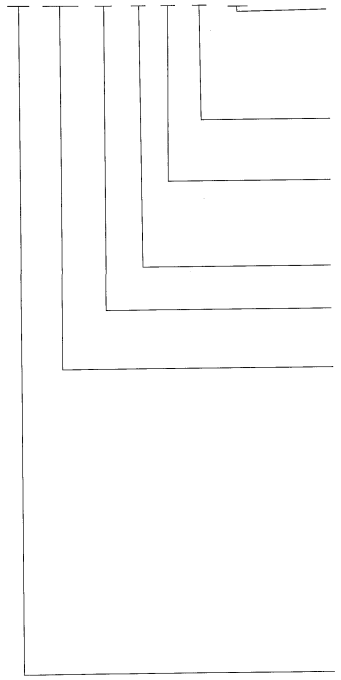
HYB 51 xxxx B J L - 60



Speed	50 = 50 ns 60 = 60 ns 70 = 70 ns 80 = 80 ns
Power	L = low power = standard
Package	= DIP J = SOJ Z = ZIP T = TSOP
	Design Revision
Organization	1000 = 1 M × 1 4100 = 4 M × 1 4171 = 256 k × 16 4256 = 256 k × 4 4400 = 1 M × 4 4800 = 512 k × 8
Power Supply Voltage	31 = 3.3 V 51 = 5 V

Memory Components (16 M & 64 M DRAMS)

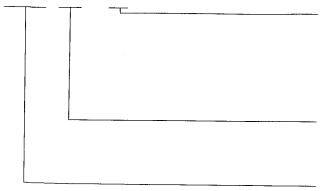
HYB 51 xxxx 0 B J L - 60



Speed	50 = 50 ns 60 = 60 ns 70 = 70 ns 80 = 80 ns
Power	L = low power = standard
Package	J = SOJ SJ = SOJ T = TSOP
	Design Revision
Function	0 = Fast Page Mode 5 = Hyper Page Mode (EDO)
Organization	1616 = 1 M × 16 (4 k-refresh) 1640 = 4 M × 4 (4 k-refresh) 1740 = 4 M × 4 (2 k-refresh) 1780 = 2 M × 8 (2 k-refresh) 1816 = 1 M × 16 (1 k-refresh) 6416 = 4 M × 16 (8 k-refresh) 6440 = 16 M × 4 (8 k-refresh) 6480 = 8 M × 8 (8 k-refresh) 6516 = 4 M × 16 (4 k-refresh) 6540 = 16 M × 4 (4 k-refresh) 6580 = 8 M × 8 (4 k-refresh)
Power Supply Voltage	31 = 3.3 V 51 = 5 V

Memory Modules

HYM xxxx GS - 60



Speed	50	= 50 ns
	60	= 60 ns
	70	= 70 ns
	80	= 80 ns
Contact Pads	GS	= gold
	S	= tin
Organization	321160	= 1 M × 32 (single sided)
	322030	= 2 M × 32 (single sided)
	322160	= 2 M × 32 (double sided)
	324020	= 4 M × 32 (single sided)
	328020	= 8 M × 32 (double sided)
	361120	= 1 M × 36 (double sided)
	361140	= 1 M × 36 (single sided)
	362140	= 2 M × 36 (double sided)
	364020	= 4 M × 36 (double sided)
	368020	= 8 M × 36 (double sided)
	641010/20	= 1 M × 64 (double sided)
	721000	= 1 M × 72 (doube sided)

Memory Components

1 M × 1-Bit Dynamic RAM
Low Power 1 M × 1-Bit Dynamic RAM

HYB 511000BJ-50/-60/-70
HYB 511000BJL-50/-60/-70

Advanced Information

- 1 048 576 words by 1-bit organization
- Fast access and cycle time
  50 ns access time
  95 ns cycle time (-50 version)
  60 ns access time
  130 ns cycle time (-60 version)
  70 ns access time
  130 ns cycle time (-70 version)
- Fast page mode cycle time
  35 ns (-50 version)
  40 ns (-60 version)
  45 ns (-70 version)
- Low power dissipation
  max. 495 mW active (-50 version)
  max. 440 mW active (-60 version)
  max. 385 mW active (-70 version)
  max. 5.5 mW standby
  max. 1.1 mW standby for L-version
- Single + 5 V (± 10 %) supply with a built-in V_{BB} generator
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "early write" operation
- Read-modify-write, $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$-only refresh, hidden-refresh, fast page mode capability and test mode capability
- All inputs, outputs and clocks TTL-compatible
- 512 refresh cycles/8 ms
  512 refresh cycles/64 ms
  for L-version only
- Plastic Packages: P-SOJ-26/20-1

Ordering Information

Type	Ordering Code	Package	Description
HYB 511000BJ-50	Q67100-Q1056	P-SOJ-26/20-1	DRAM (access time 50 ns)
HYB 511000BJ-60	Q67100-Q518	P-SOJ-26/20-1	DRAM (access time 60 ns)
HYB 511000BJ-70	Q67100-Q519	P-SOJ-26/20-1	DRAM (access time 70 ns)
HYB 511000BJL-50	on request	P-SOJ-26/20-1	DRAM (access time 50 ns)
HYB 511000BJL-60	Q67100-Q526	P-SOJ-26/20-1	DRAM (access time 60 ns)
HYB 511000BJL-70	Q67100-Q527	P-SOJ-26/20-1	DRAM (access time 70 ns)

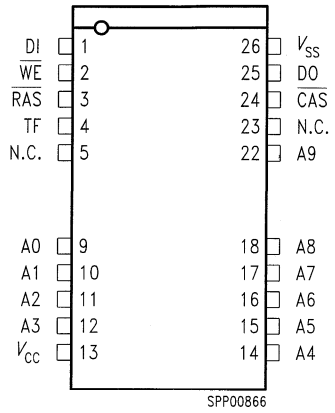
The HYB 511000BJ/BJL is the new generation dynamic RAM organized as 1 048 576 words by 1-bit. The HYB 511000BJ/BJL utilizes CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and for the system user. Multiplexed address inputs permit the HYB 511000BJ/BJL to be packaged in a standard plastic P-SOJ-26/20. This package size provides high system bit densities and is compatible with commonly used automatic testing and insertion equipment. System oriented features include single + 5 V (± 10 %) power supply, direct interfacing with high-performance logic device families such as Schottky TTL. "Test Mode" function is implemented. The HYB 511000BJL are specially selected for low power battery backup applications.

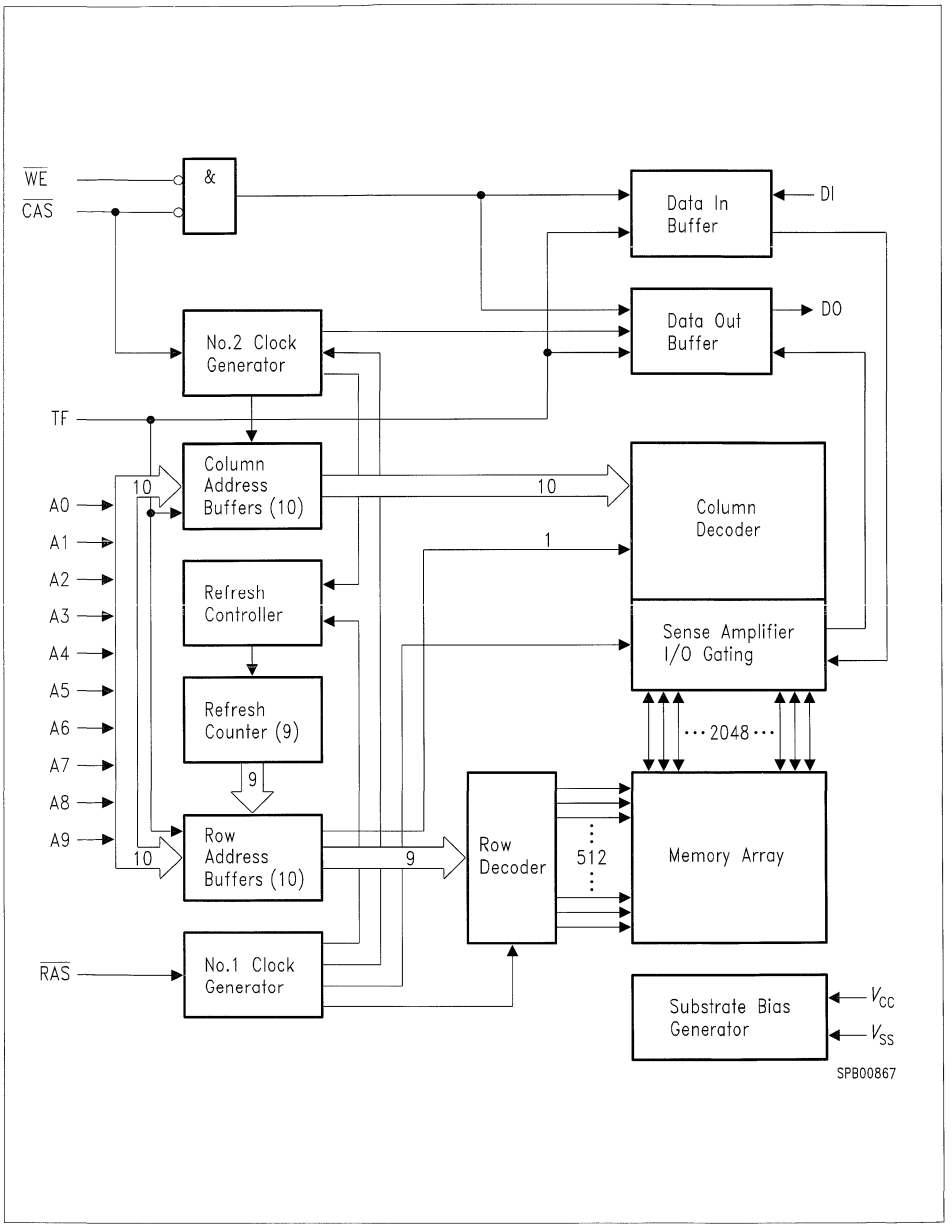
Pin Definitions and Functions

Pin No.	Function
A0-A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
DI	Data In
DO	Data Out
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground (0 V)
TF	Test Function
N.C.	No Connection

Pin Configuration
(top view)

SOJ-26/20-1





Block Diagram

Absolute Maximum Ratings

Operating temperature range ..... 0 to + 70 °C

Storage temperature range ..... – 55 to + 150 °C

Soldering temperature ..... 260 °C

Soldering time ..... 10 s

Input/output voltage ..... – 1 to + 7 V

Test Function Input voltage ..... – 1 to + 10.5 V

Power supply voltage ..... – 1 to + 7 V

Power dissipation ..... 0.6 W

Data out current (short circuit) ..... 50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{CC} = 5 V ± 10 %

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	6.5	V	1)
Input low voltage	V_{IL}	– 1.0	0.8	V	1)
Test enable input high voltage	$V_{IH(TF)}$	V_{CC} + 4.5	10.5	V	1)
Test disable input low voltage	$V_{IL(TF)}$	– 1.0	V_{CC} + 1.0	V	1)
Output high voltage (I_{OUT} = – 5 mA)	V_{OH}	2.4	–	V	1)
Output low voltage (I_{OUT} = 4.2 mA)	V_{OL}	–	0.4	V	1)
Input leakage current, any input except $\overline{TF}$ (0 V ≤ V_{IN} ≤ 6.5 V, all other pins = 0 V)	$I_{I(L)}$	– 10	10	µA	1)
Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ 5.5 V)	$I_{O(L)}$	– 10	10	µA	1)
Average V_{CC} supply current:	I_{CC1}				
-50 version		–	90	mA	2) 3)
-60 version		–	80	mA	2) 3)
-70 version		–	70	mA	2) 3)
($\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = t_{RC} min.)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	2	mA	–

DC Characteristics (cont'd)
T_A = 0 to 70 °C; V_{SS} = 0 V; V_{CC} = 5 V ± 10 %

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current during $\overline{RAS}$ only refresh cycles: -50 version	I_{CC3}	–	90	mA	2)
-60 version		–	80	mA	2)
-70 version		–	70	mA	2)
($\overline{RAS}$ cycling: $\overline{CAS}$ = V_{IH} : t_{RC} = t_{RC} min.)					
Average V_{CC} supply current during fast page modes: -50 version	I_{CC4}	–	70	mA	2) 3)
-60 version		–	60	mA	2) 3)
-70 version		–	50	mA	2) 3)
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling: t_{PC} = t_{PC} min.)					
Standby V_{CC} supply current	I_{CC5}	–	1	mA	1)
L-Version		–	200	µA	1)
($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)					
Average V_{CC} supply current during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode:	I_{CC6}				
-50 version		–	90	mA	2)
-60 version		–	80	mA	2)
-70 version		–	70	mA	2)
($\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = t_{RC} min.)					
For L-version only: Battery backup current: average power supply current, battery backup mode: ($\overline{CAS}$ = $\overline{CAS}$ before $\overline{RAS}$ cycling or 0.2 V, $\overline{WE}$ = V_{CC} – 0.2 V or 0.2 V, A0 to A9 = V_{CC} – 0.2 V or 0.2 V, DI = V_{CC} – 0.2 V or 0.2 V open, t_{RC} = 125 µs, t_{RAS} = t_{RAS} min. ~ 1 µs)	I_{CC7}	–	300	µA	2)
Input leakage current (only TF) (0 V ≤ V_{IN} (TF) ≤ V_{CC} + 0.5 V) All other pins not under test = 0 V	$I_{ITF(L)}$	– 10	+ 10	µA	1)
Test function input current (V_{CC} + 4.5 ≤ V_{IN} (TF) ≤ 10.5 V)	I_{TF}	–	1	mA	1)

AC Characteristics [4) 13)]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		-50		-60		-70		
		min.	max.	min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	95	–	110	–	130	–	ns
Read-write cycle time	t_{RWC}	115	–	130	–	155	–	ns
Fast page mode cycle time	t_{PC}	35	–	40	–	45	–	ns
Fast page mode read-write cycle time	t_{PRWC}	55	–	60	–	70	–	ns
Access time from $\overline{RAS}$ [6) 11)]	t_{RAC}	–	50	–	60	–	70	ns
Access time from $\overline{CAS}$ [6) 11)]	t_{CAC}	–	15	–	15	–	20	ns
Access time from column address [6) 12)]	t_{AA}	–	25	–	30	–	35	ns
Access time from $\overline{CAS}$ precharge [6)]	t_{CPA}	–	30	–	35	–	40	ns
$\overline{CAS}$ to output in low-Z [6)]	t_{CLZ}	0	–	0	–	0	–	ns
Output buffer turn-off delay [7)]	t_{OFF}	0	15	0	20	0	20	ns
Transition time (rise and fall) [5)]	t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	35	–	40	–	50	–	ns
$\overline{RAS}$ pulse width	t_{RAS}	50	10.000	60	10.000	70	10.000	ns
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	50	100.000	60	100.000	70	100.000	ns
$\overline{RAS}$ hold time	t_{RSH}	15	–	15	–	20	–	ns
$\overline{CAS}$ hold time	t_{CSH}	50	–	60	–	70	–	ns
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge (FPM)	t_{RHCP}	30	–	35	–	45	–	ns
$\overline{CAS}$ precharge to $\overline{WE}$ delay time (FPM RMW)	t_{CPWD}	30	–	35	–	45	–	ns
$\overline{CAS}$ pulse width	t_{CAS}	15	10.000	15	10.000	20	10.000	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time [11)]	t_{RCD}	20	35	20	45	20	50	ns

AC Characteristics (cont'd) [4] [13]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		-50		-60		-70		
		min.	max.	min.	max.	min.	max.	
$\overline{RAS}$ to column address delay time [12]	t_{RAD}	15	25	15	30	15	35	ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	5	–	ns
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10	–	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns
Row address hold time	t_{RAH}	10	–	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns
Column address hold time	t_{CAH}	15	–	15	–	15	–	ns
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	–	30	–	35	–	ns
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns
Read command hold time [8]	t_{RCH}	0	–	0	–	0	–	ns
Read command hold time referenced to $\overline{RAS}$ [8]	t_{RRH}	0	–	0	–	0	–	ns
Write command hold time	t_{WCH}	10	–	10	–	15	–	ns
Write command pulse width	t_{WP}	10	–	10	–	15	–	ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	–	15	–	20	–	ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	–	15	–	20	–	ns
Data setup time [9]	t_{DS}	0	–	0	–	0	–	ns
Data hold time [9]	t_{DH}	10	–	15	–	15	–	ns
Refresh period	t_{REF}	–	8	–	8	–	8	ms
Refresh period for L-version only	t_{REF}	–	64	–	64	–	64	ms

AC Characteristics (cont'd) [4) 13)]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		-50		-60		-70		
		min.	max.	min.	max.	min.	max.	
Write command setup time [10)]	t_{WCS}	0	–	0	–	0	–	ns
$\overline{CAS}$ to $\overline{WE}$ delay time [10)]	t_{CWD}	15	–	15	–	20	–	ns
$\overline{RAS}$ to $\overline{WE}$ delay time [10)]	t_{RWD}	50	–	60	–	70	–	ns
Column address to $\overline{WE}$ delay time [10)]	t_{AWD}	25	–	30	–	35	–	ns
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CSR}	5	–	5	–	5	–	ns
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CHR}	10	–	15	–	15	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	0	–	0	–	0	–	ns
$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ counter test cycle)	t_{CPT}	25	–	30	–	40	–	ns
Test mode enable setup time referenced to $\overline{RAS}$	t_{TES}	0	–	0	–	0	–	ns
Test mode enable hold time referenced to $\overline{RAS}$	t_{TEHR}	0	–	0	–	0	–	ns
Test mode enable hold time referenced to $\overline{CAS}$	t_{TEHC}	0	–	0	–	0	–	ns

Capacitance

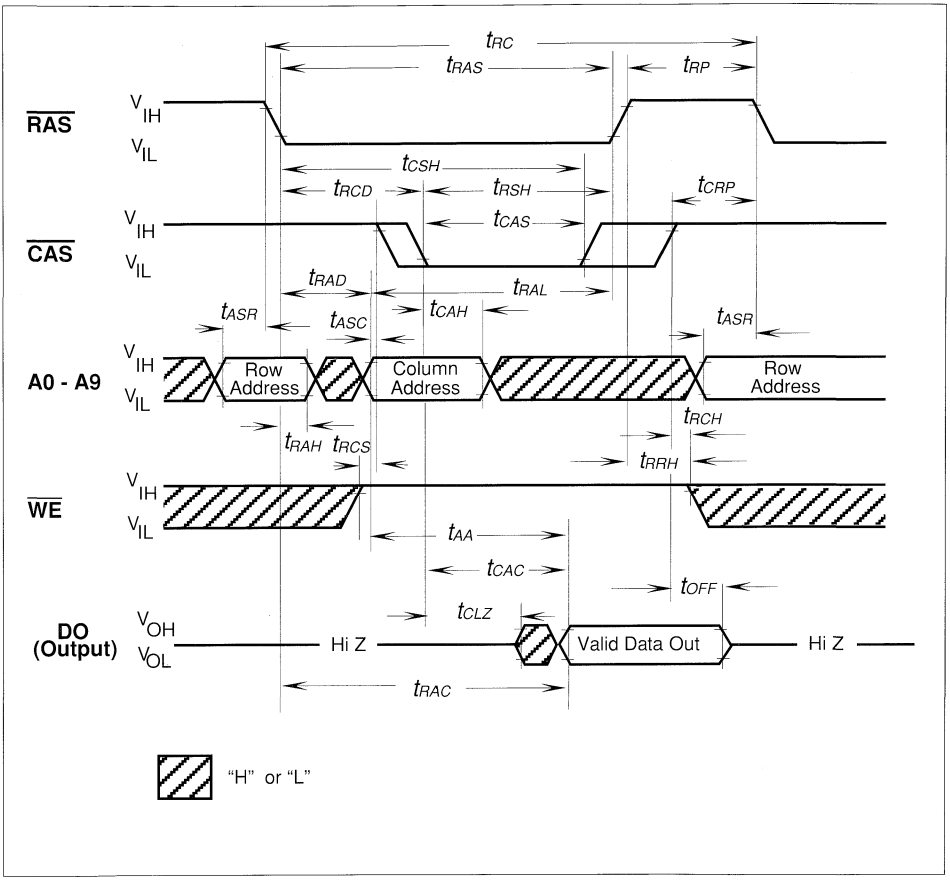
T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A9, DI)	C_{I1}	–	5	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, TF)	C_{I2}	–	7	pF
Output capacitance (DO)	C_O	–	7	pF

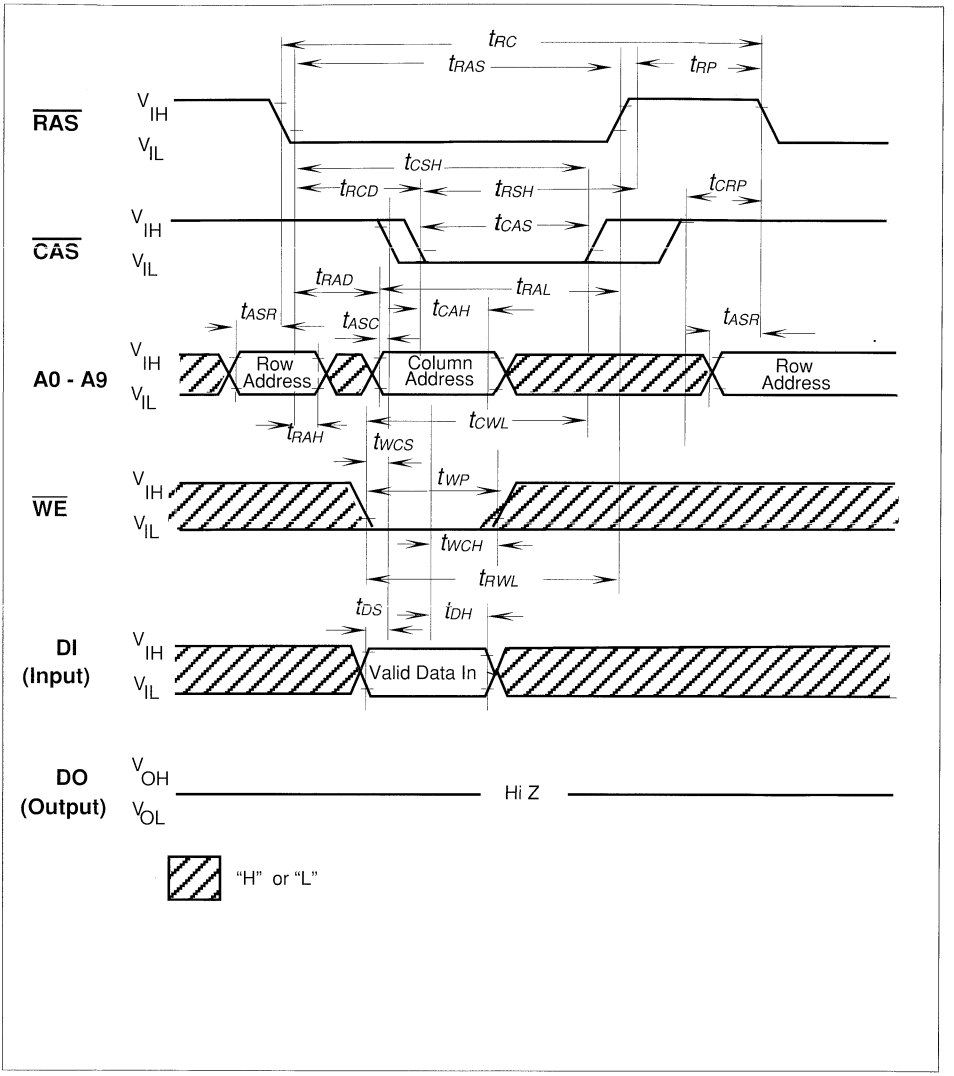
Notes :

1) All voltages are referenced to V_{SS}.
2) I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6}, I_{CC7} depend on cycle rate.
3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.
4) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
5) V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.
6) Measured with a load equivalent to 2 TTL loads and 100 pF.
7) t_{OFF} (max.) defines the time at which the output achieves the open-circuit conditions and is not referenced to output voltage levels.
8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9) These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.
10) t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only.
If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.) and $t_{AWD} \geq t_{AWD}$ (min.), the cycle is a read-write cycle and DO will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of DO (at access time) is indeterminate.
11) Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
12) Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.
13) AC measurements assume t_T = 5ns.

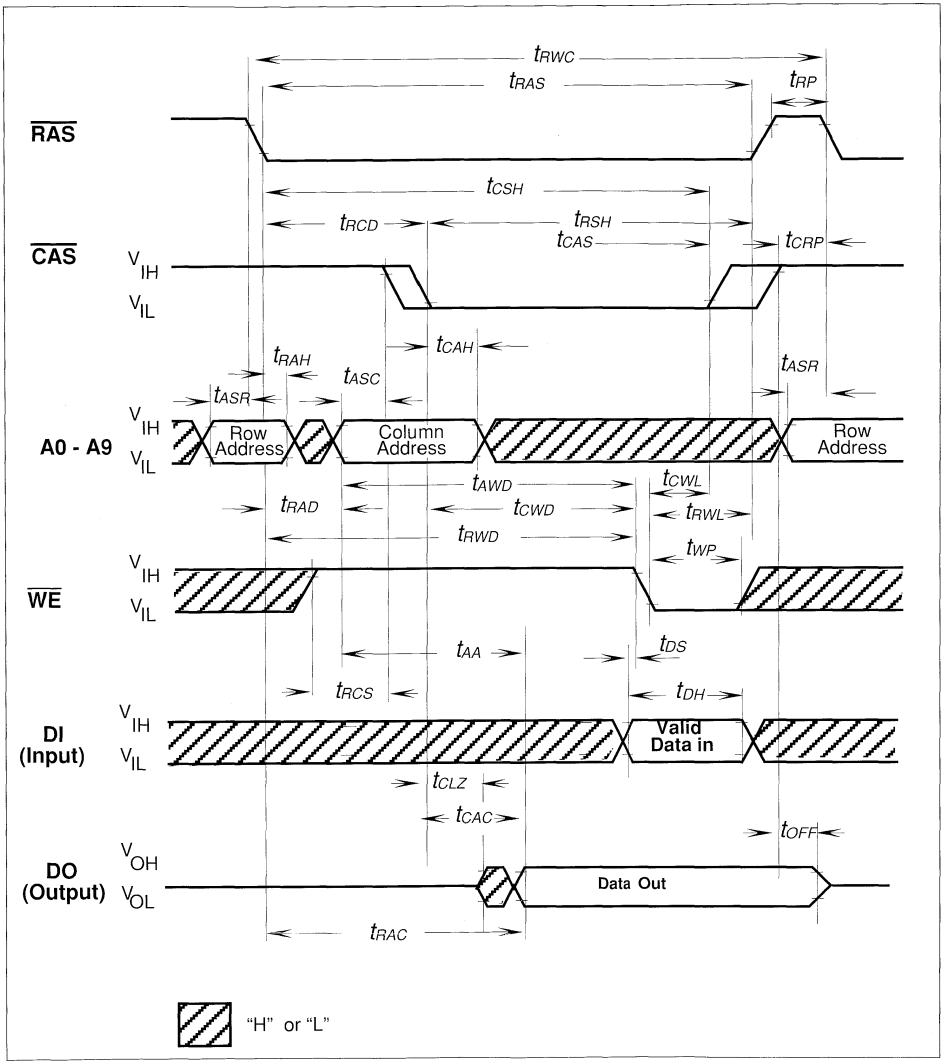
Waveforms



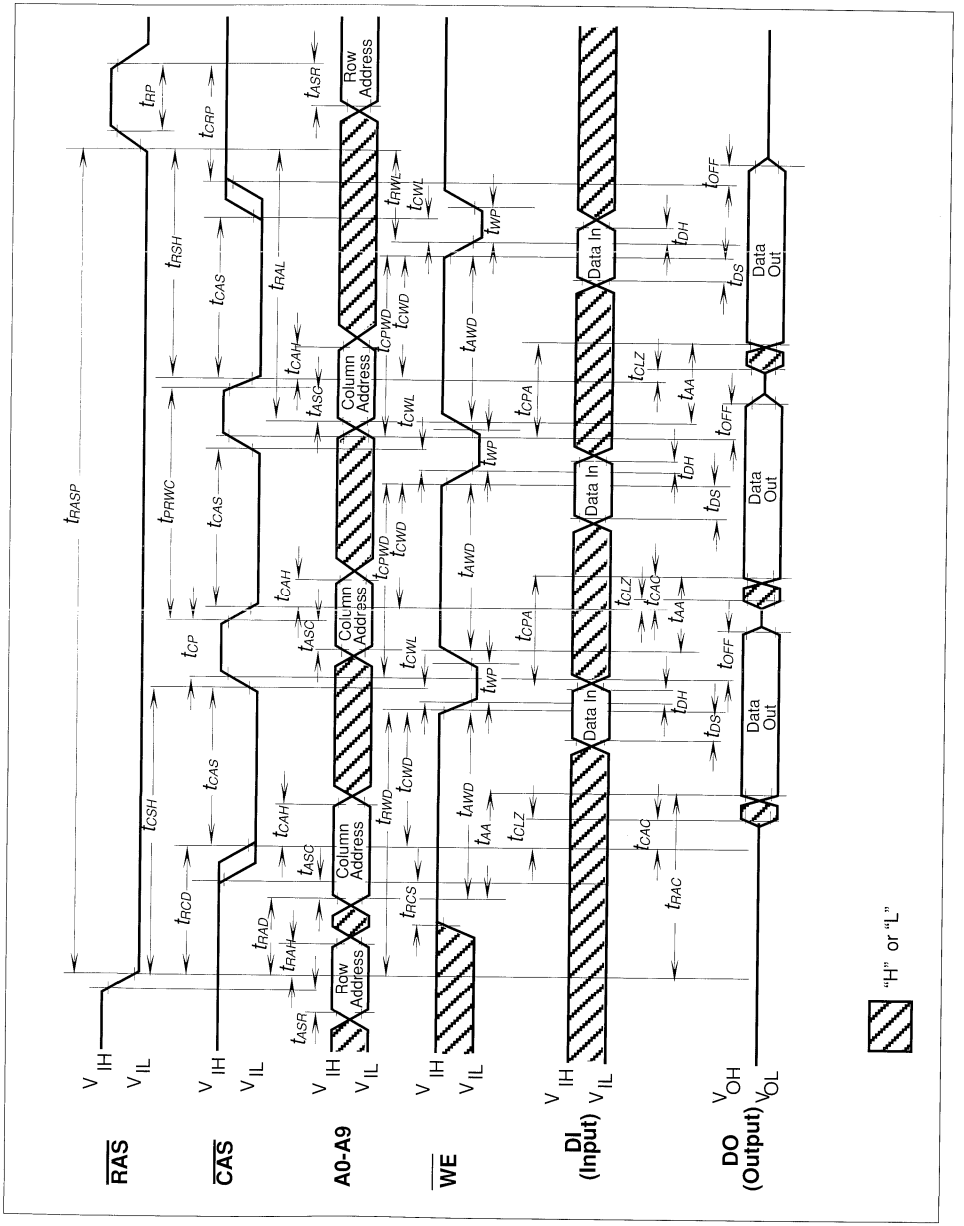
Read Cycle



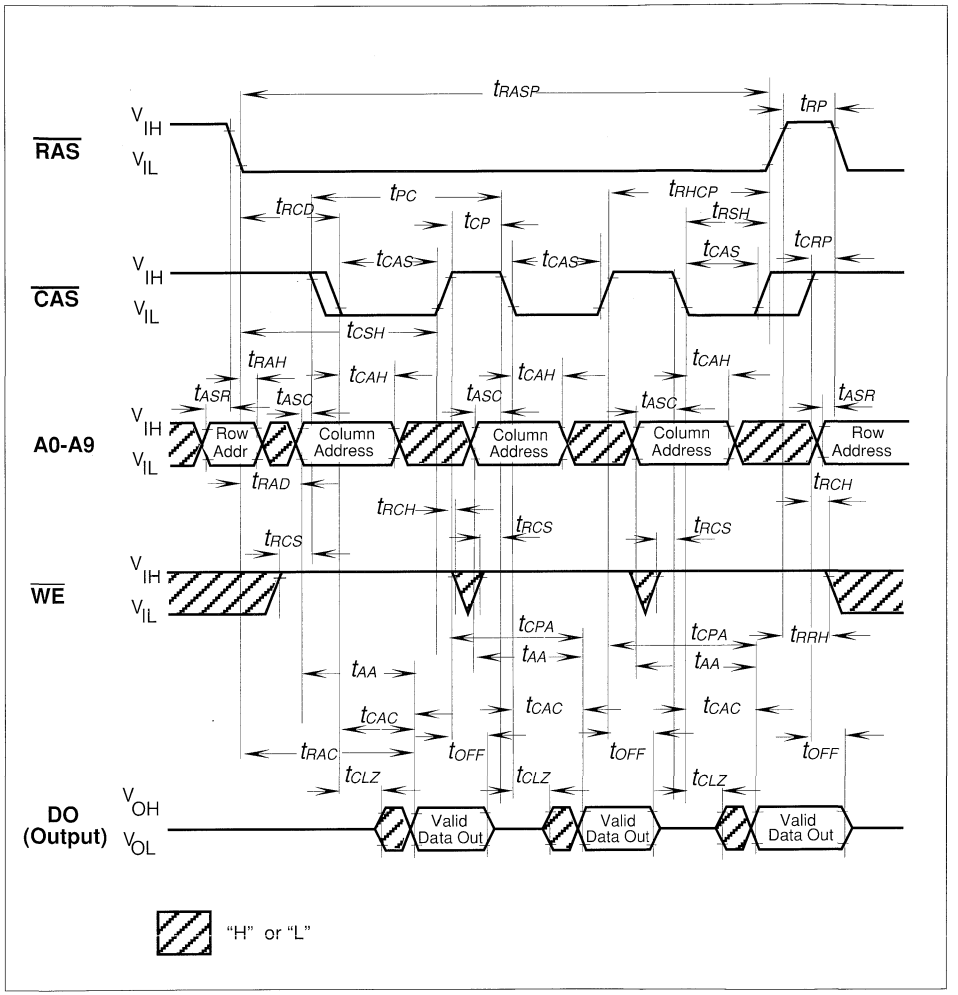
Write Cycle (Early Write)



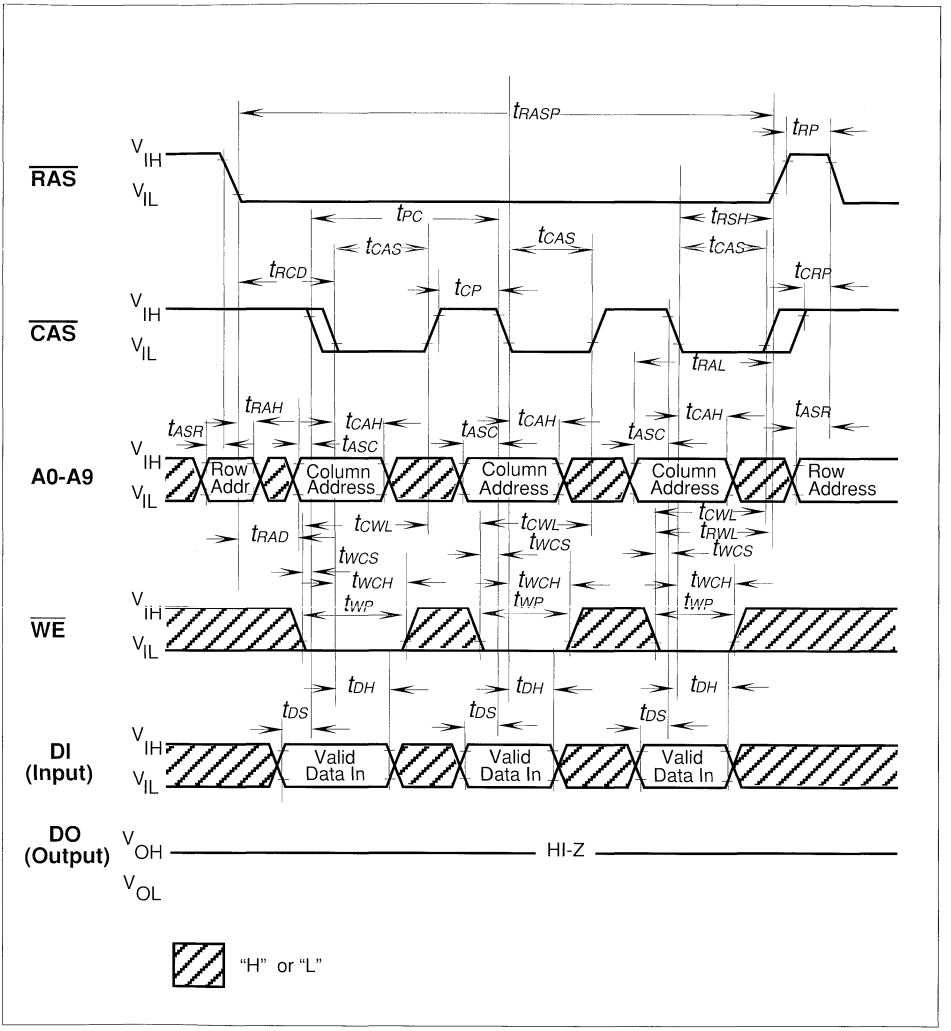
Read-Write (Read-Modify-Write) Cycle



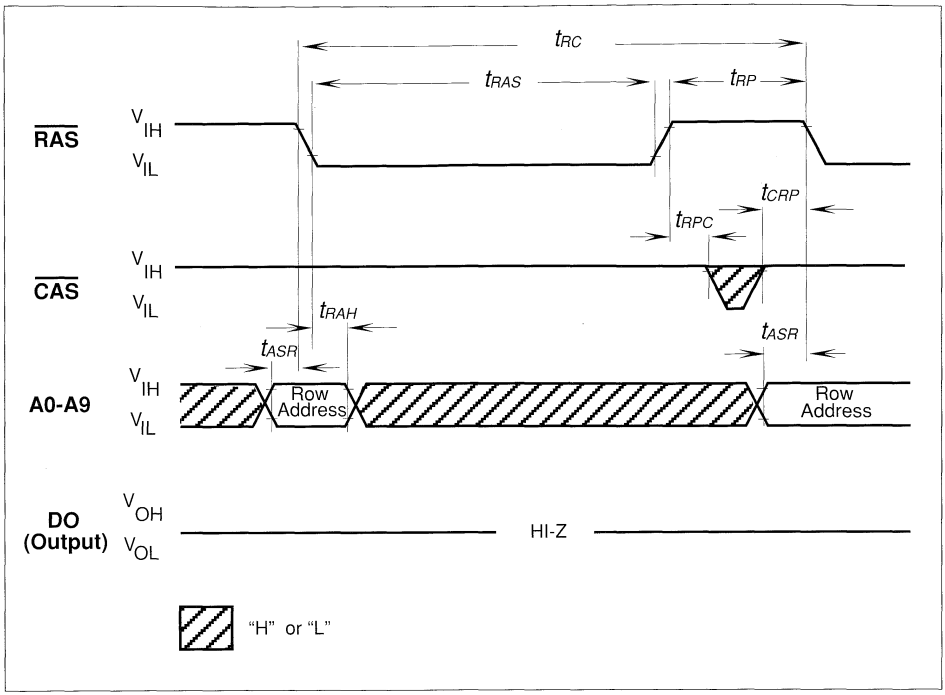
Fast Page Mode Read-Modify-Write Cycle



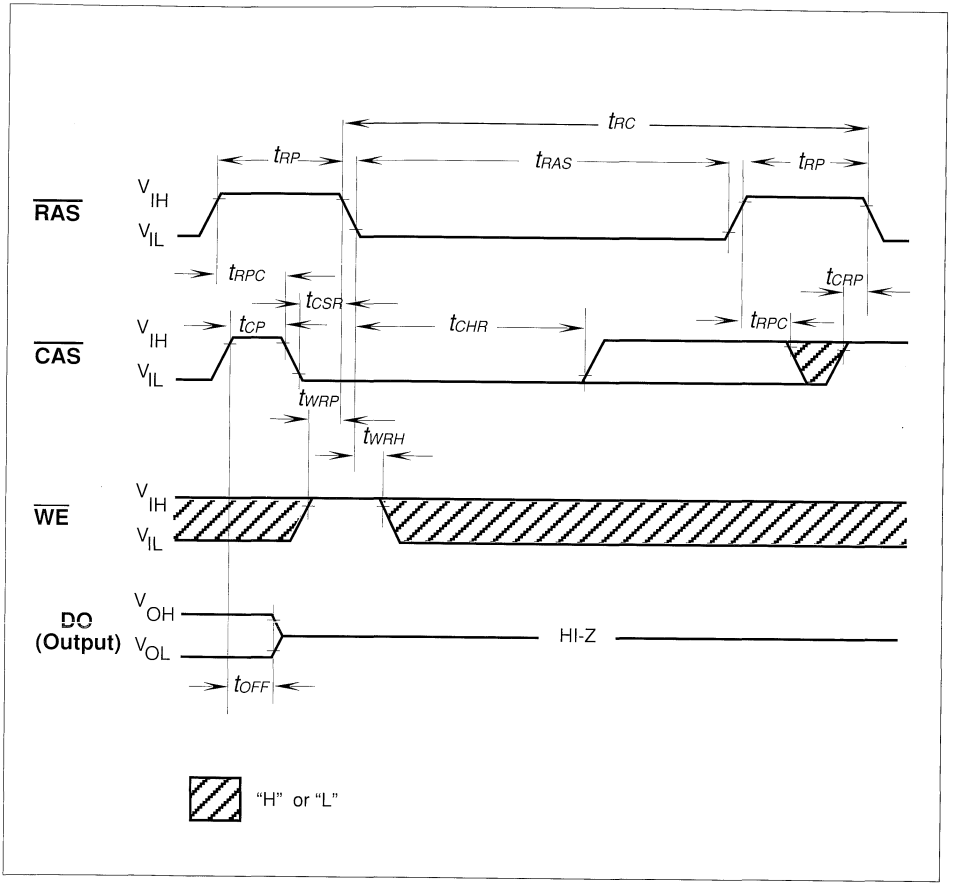
Fast Page Mode Read Cycle



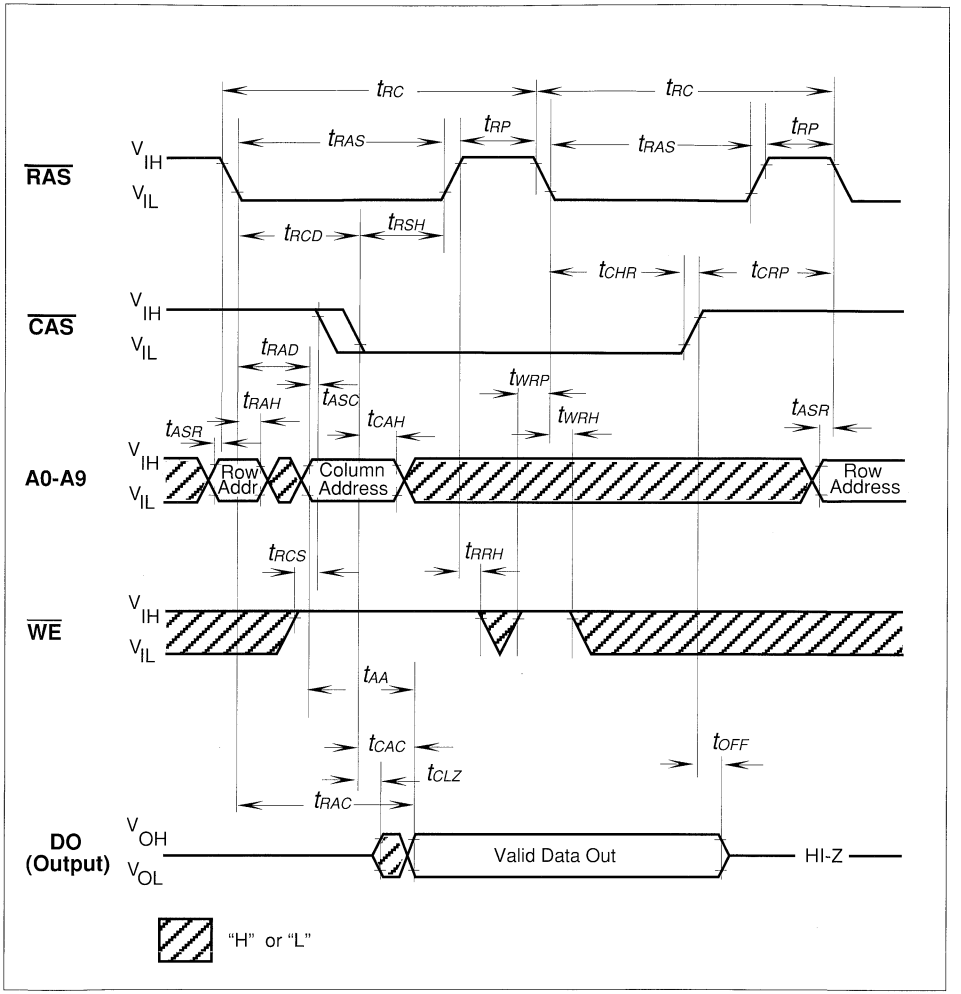
Fast Page Mode Early Write Cycle



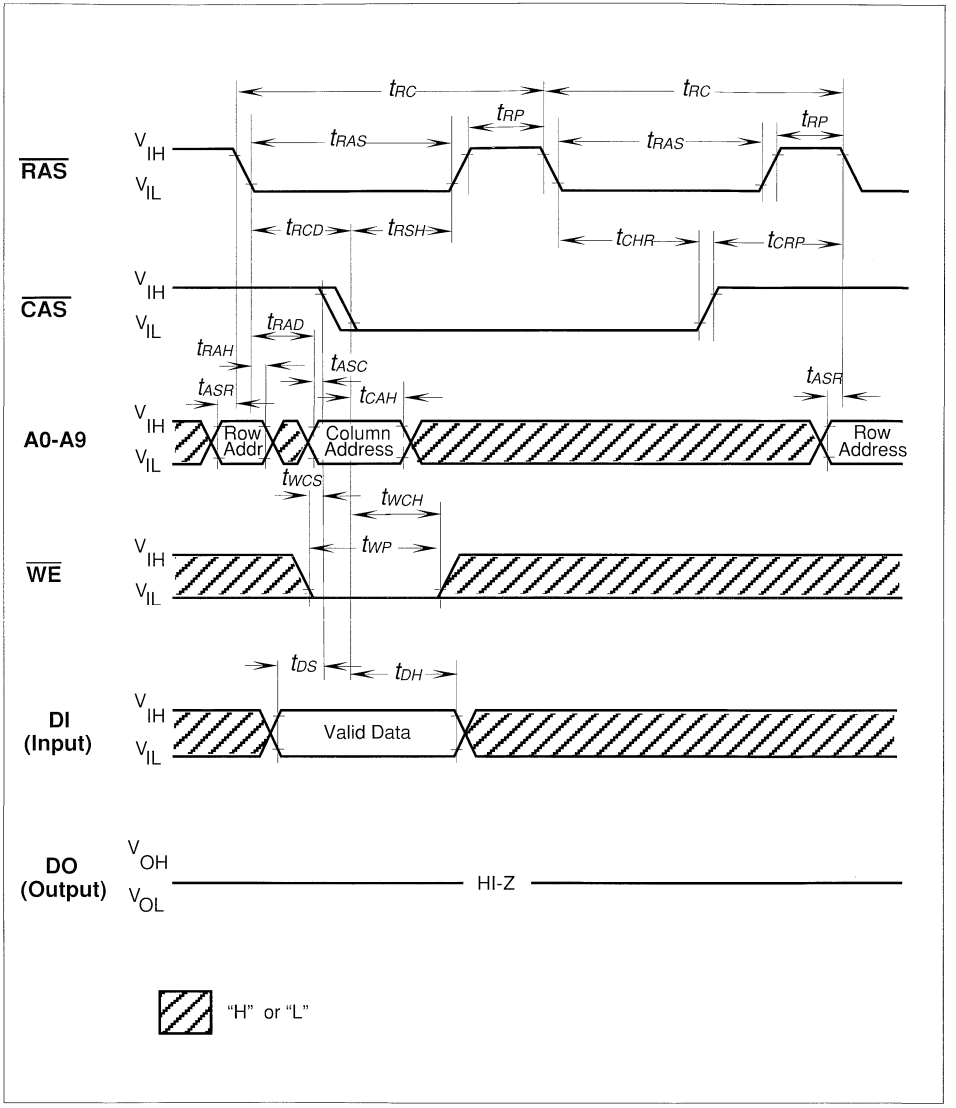
RAS-Only Refresh Cycle



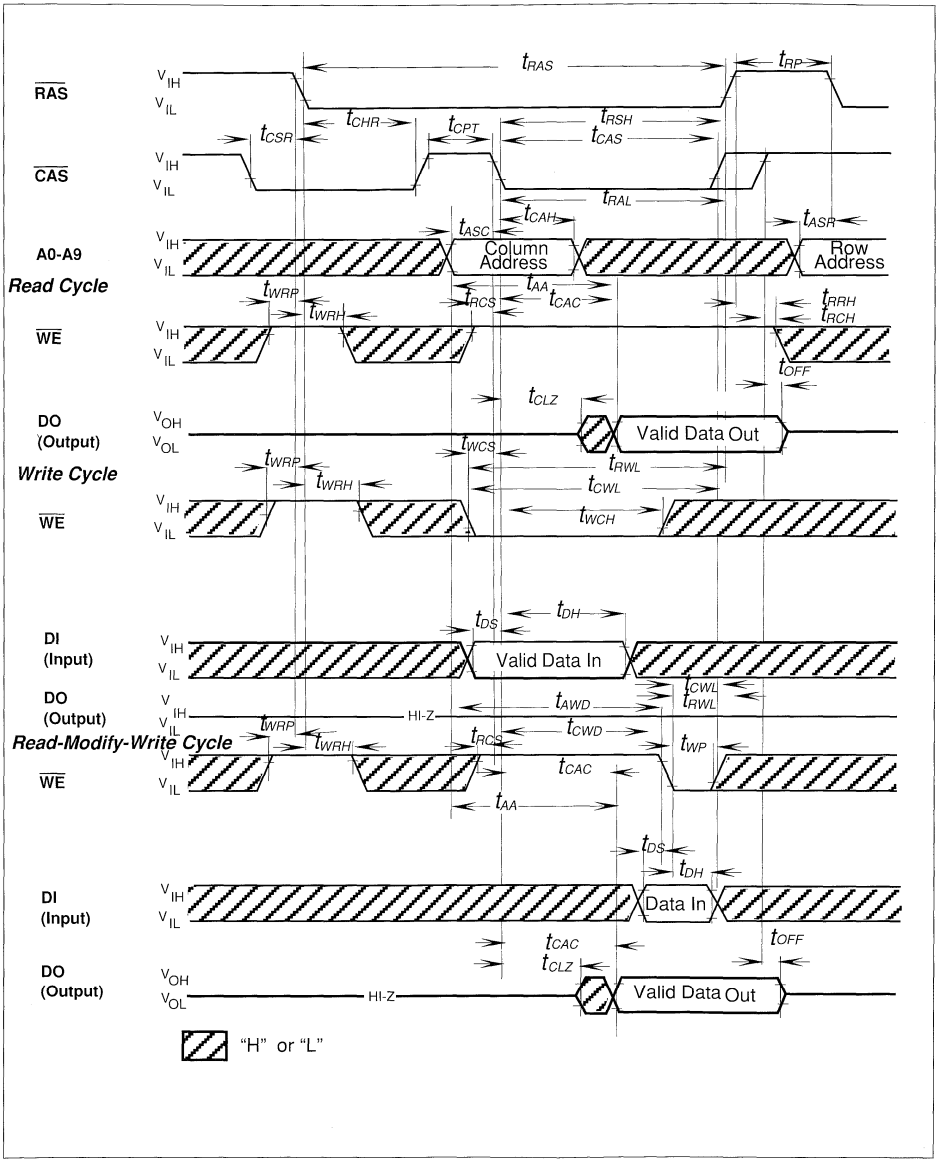
CAS-Before-RAS Refresh Cycle



Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Early Write)



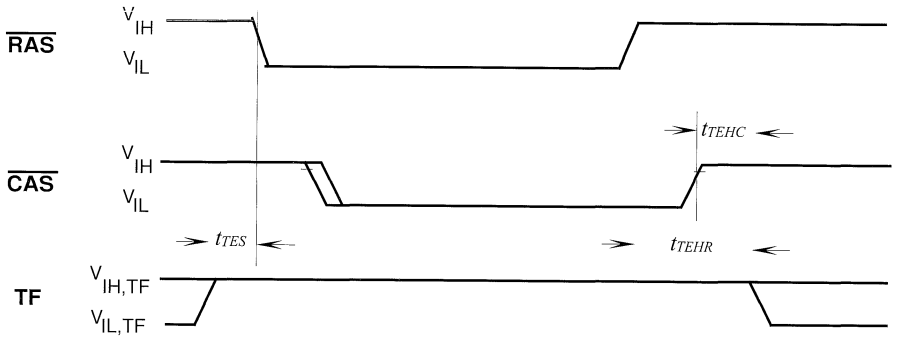
CAS-Before-RAS Refresh Counter Test Cycle

Test Mode

The HYB 511000B/BL is the RAM organized 1 048 576 words by 1-bit, it is internally organized 262 144 words by 4-bit. In "Test Mode", data would be written into a number of sectors (4 sectors) in parallel and retrieved the same way. If upon reading, all bits are equal (all "H" or "L"), the data output pin indicates a same data as all bits. In this case, the data output pin indicates an expected data for good parts, the data output pin indicates a complementary data for bad parts. And also, if any of the bits differed, the data output pin would indicate a high impedance state for bad parts. The next figure shows the block diagram including its truth table when "Test Mode" is used.

In test mode, 1M DRAM can be tested as if it were 256K DRAM by the following method.

"Test Mode" function is performed on any of the timing cycles including fast page mode when "TF" pin is held on "super voltage (V_{CC} + 4.5 V (V_{CC} = 5 V ± 10 %), max. voltage = 10.5 V)" for the specified period (t_{TES}, t_{TEHR} and t_{TEHC}; see next figure). The address input of A9 is ignored in the "Test Mode". On the other hand, normal operation requires the "TF" pin be connected to V_{IL}(TF) level, or left unconnected on the printed wiring board. The "Test Mode" function reduces test times (1/4; in case of using N test pattern).



Test Mode Cycle

256 K × 4-Bit Dynamic RAM
Low Power 256 K × 4-Bit Dynamic RAM

HYB 514256B/BJ-50/-60/-70
HYB 514256BL/BJL-50/-60/-70

Advanced Information

- 262 144 words by 4-bit organization
- Fast access and cycle time
  50 ns access time
  95 ns cycle time (-50 version)
  60 ns access time
  110 ns cycle time (-60 version)
  70 ns access time
  130 ns cycle time (-70 version)
- Fast page mode cycle time
  35 ns (-50 version)
  40 ns (-60 version)
  45 ns (-70 version)
- Low power dissipation
  max. 495 mW active (-50 version)
  max. 440 mW active (-60 version)
  max. 385 mW active (-70 version)
  max. 5.5 mW standby
  max. 1.1 mW standby for L-version
- Single + 5 V (± 10 %) supply with a built-in V_{BB} generator
- Output unlatched at cycle end allows two-dimensional chip selection
- Read-modify-write, $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$-only refresh, hidden-refresh and fast page mode capability
- All inputs, outputs and clocks TTL-compatible
- 512 refresh cycles/8 ms
  512 refresh cycles/64 ms
  for L-version only
- Plastic Packages: P-DIP-20-2,
  P-SOJ-26/20-1

Ordering Information

Type	Ordering Code	Package	Description
HYB 514256B-50	Q67100-Q1044	P-DIP-20-2	DRAM (access time 50ns)
HYB 514256B-60	Q67100-Q530	P-DIP-20-2	DRAM (access time 60 ns)
HYB 514256B-70	Q67100-Q433	P-DIP-20-2	DRAM (access time 70 ns)
HYB 514256BJ-50	Q67100-Q1054	P-SOJ-26/20-1	DRAM (access time 50 ns)
HYB 514256BJ-60	Q67100-Q536	P-SOJ-26/20-1	DRAM (access time 60 ns)
HYB 514256BJ-70	Q67100-Q537	P-SOJ-26/20-1	DRAM (access time 70 ns)
HYB 514256BL-50	on request	P-DIP-20-2	DRAM (access time 50 ns)
HYB 514256BL-60	Q67100-Q542	P-DIP-20-2	DRAM (access time 60 ns)
HYB 514256BL-70	Q67100-Q543	P-DIP-20-2	DRAM (access time 70 ns)
HYB 514256BJL-50	on request	P-SOJ-26/20-1	DRAM (access time 50 ns)
HYB 514256BJL-60	Q67100-Q608	P-SOJ-26/20-1	DRAM (access time 60 ns)
HYB 514256BJL-70	Q67100-Q607	P-SOJ-26/20-1	DRAM (access time 70 ns)

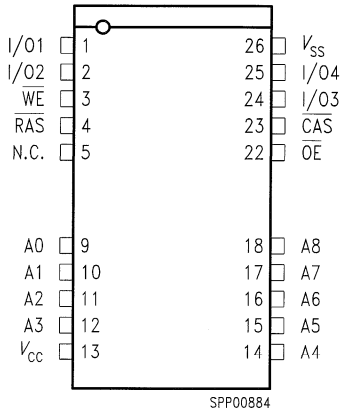
The HYB 514256B/BJ/BL/BJL is the new generation dynamic RAM organized as 262 144 words by 4-bit. The HYB 514256B/BJ/BL/BJL utilizes CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and for the system user. Multiplexed address inputs permit the HYB 514256B/BJ/BL/BJL to be packaged in a standard plastic P-DIP-20-2,or plastic P-SOJ-26/20-1. This package size provides high system bit densities and is compatible with commonly used automatic testing and insertion equipment. System oriented features include single + 5 V (± 10 %) power supply, direct interfacing with high-performance logic device families such as Schottky TTL. These HYB 514256BL/BJL are specially selected for battery backup applications.

Pin Definitions and Functions

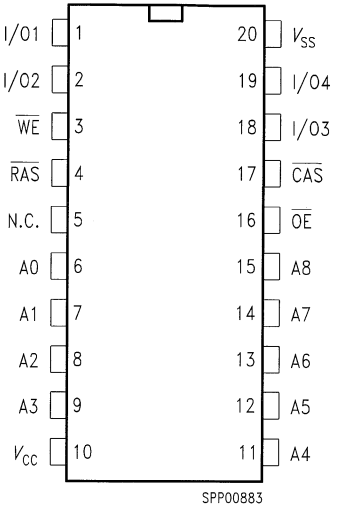
Pin No.	Function
A0-A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{OE}$	Output Enable
I/O1-I/O4	Data Input/Output
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground (0 V)
N.C.	No Connection

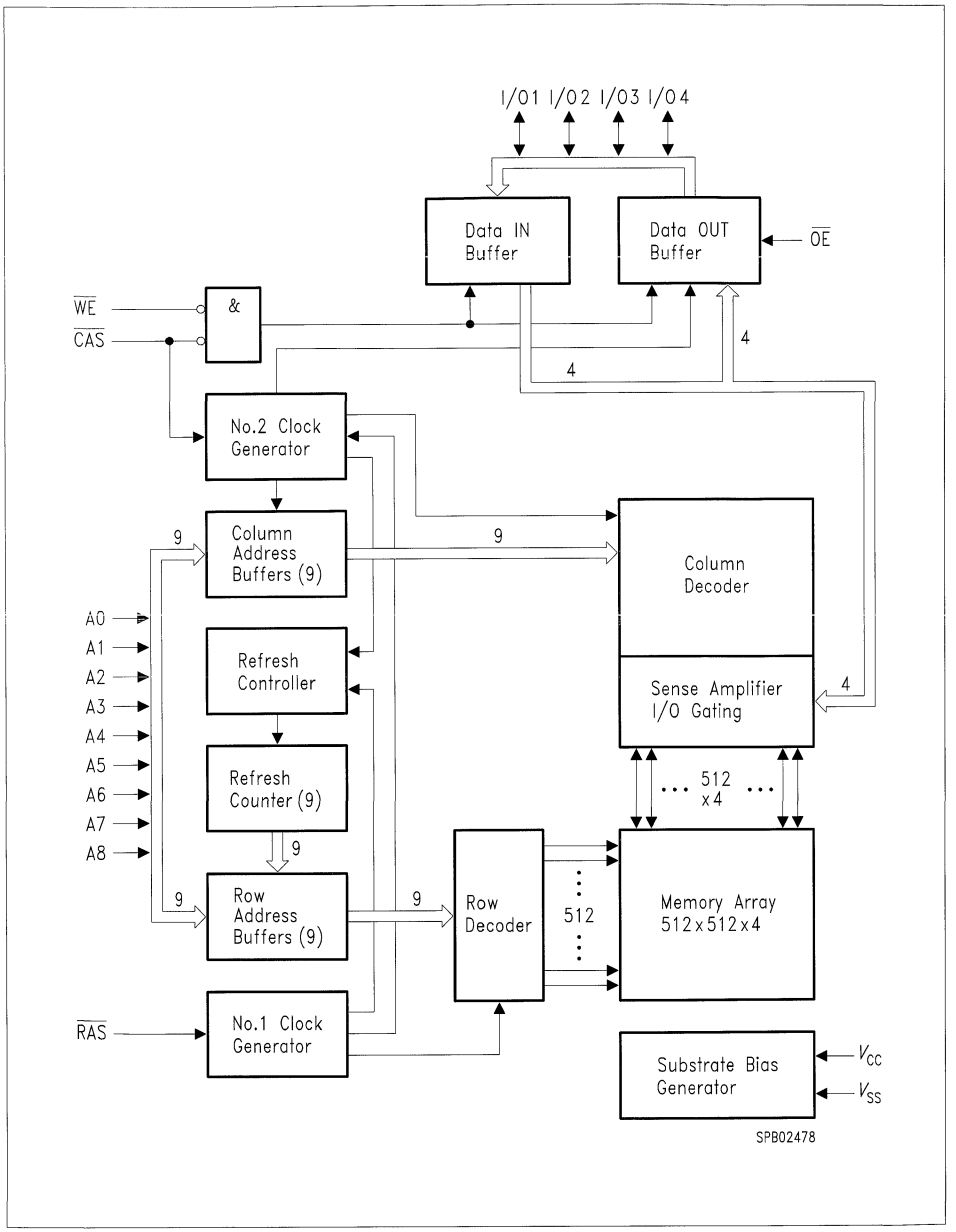
Pin Configuration
(top view)

P-SOJ-26/20-1



P-DIP-20-2





Block Diagram

Absolute Maximum Ratings

Operating temperature range ..... 0 to + 70 °C

Storage temperature range ..... – 55 to + 150 °C

Soldering temperature ..... 260 °C

Soldering time ..... 10 s

Input/output voltage ..... – 1 to + 7 V

Power supply voltage ..... – 1 to + 7 V

Power dissipation ..... 0.6 W

Data out current (short circuit) ..... 50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{CC} = 5 V ± 10 %

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	6.5	V	1)
Input low voltage	V_{IL}	– 1.0	0.8	V	1)
Output high voltage (I_{OUT} = – 5 mA)	V_{OH}	2.4	–	V	1)
Output low voltage (I_{OUT} = 4.2 mA)	V_{OL}	–	0.4	V	1)
Input leakage current, any input (0 V ≤ V_{IN} ≤ 6.5 V, all other pins = 0 V)	$I_{I(L)}$	– 10	10	µA	1)
Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ V_{CC})	$I_{O(L)}$	– 10	10	µA	1)
Average V_{CC} supply current:	I_{CC1}				
-50 version		–	90	mA	2) 3)
-60 version		–	80	mA	2) 3)
-70 version		–	70	mA	2) 3)
($\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = t_{RC} min.)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	2	mA	–
Average V_{CC} supply current, $\overline{RAS}$ only mode:	I_{CC3}				
-50 version		–	90	mA	2)
-60 version		–	80	mA	2)
-70 version		–	70	mA	2)
($\overline{RAS}$ cycling: $\overline{CAS}$ = V_{IH} : t_{RC} = t_{RC} min.)					

DC Characteristics (cont'd)

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{CC} = 5 V ± 10 %

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current, fast page mode:	I_{CC4}				
-60 version		–	70	mA	2) 3
-70 version		–	60	mA	2) 3)
-50 version		–	50	mA	2) 3)
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling: t_{PC} = t_{PC} min.)					
Standby V_{CC} supply current	I_{CC5}	–	1	mA	1)
L-Version		–	200	µA	1)
($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)					
Average V_{CC} supply current, $\overline{CAS}$-before-RAS refresh mode:	I_{CC6}				
-50 version		–	90	mA	2)
-60 version		–	80	mA	2)
-70 version		–	70	mA	2)
($\overline{RAS}$, $\overline{CAS}$ cycling: t_{RC} = t_{RC} min.)					
For L-version only: Battery backup current: average power supply current, battery backup mode: ($\overline{CAS}$ = $\overline{CAS}$ before $\overline{RAS}$ cycling or 0.2 V, $\overline{OE}$ = V_{CC} – 0.2 V $\overline{WE}$ = V_{CC} – 0.2 V or 0.2 V, A0 to A8 = V_{CC} – 0.2 V or 0.2 V, I/O1 to I/O4 = V_{CC} – 0.2 V or 0.2 V or open, t_{RC} = 125 µs, t_{RAS} = t_{RAS} min. ~ 1 µs)	I_{CC7}	–	300	µA	2)

AC Characteristics [4) 13)]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		-50		-60		-70		
		min.	max.	min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	95	–	110	–	130	–	ns
Read-modify-write cycle time	t_{RWC}	140	–	160	–	185	–	ns
Fast page mode cycle time	t_{PC}	35	–	40	–	45	–	ns
Fast page mode read-modify-write cycle time	t_{PRWC}	80	–	90	–	100	–	ns
Access time from $\overline{RAS}$ [6) 11)]	t_{RAC}	–	50	–	60	–	70	ns
Access time from $\overline{CAS}$ [6) 11)]	t_{CAC}	–	15	–	15	–	20	ns
Access time from column address [6) 12)]	t_{AA}	–	25	–	30	–	35	ns
Access time from $\overline{CAS}$ precharge [6) 12)]	t_{CPA}	–	30	–	35	–	40	ns
$\overline{CAS}$ to output in low-Z [4)]	t_{CLZ}	0	–	0	–	0	–	ns
Output buffer turn-off delay [7)]	t_{OFF}	0	15	0	20	0	20	ns
Transition time (rise and fall) [5)]	t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	35	–	40	–	50	–	ns
$\overline{RAS}$ pulse width	t_{RAS}	50	10.000	60	10.000	70	10.000	ns
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	50	100.000	60	100.000	70	100.000	ns
$\overline{RAS}$ hold time	t_{RSH}	15	–	15	–	20	–	ns
$\overline{CAS}$ hold time	t_{CSH}	50	–	60	–	70	–	ns
$\overline{CAS}$ pulse width	t_{CAS}	15	10.000	15	10.000	20	10.000	ns
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge (Fast Page Mode)	t_{RHCP}	30	–	35	–	45	–	ns
$\overline{CAS}$ precharge to $\overline{WE}$ delay time (FPM RMW)	t_{CPWD}	55	–	60	–	65	–	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time [11)]	t_{RCD}	20	35	20	45	20	50	
$\overline{RAS}$ to column address delay time [12)]	t_{RAD}	15	25	15	30	15	35	ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	5	–	ns
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	10	–	ns

AC Characteristics (cont'd) [4] [13]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		-50		-60		-70		
		min.	max.	min.	max.	min.	max.	
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns
Row address hold time	t_{RAH}	10	–	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns
Column address hold time	t_{CAH}	10	–	15	–	15	–	ns
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	–	30	–	35	–	ns
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns
Read command hold time [8]	t_{RCH}	0	–	0	–	0	–	ns
Read command hold time referenced to $\overline{RAS}$ [8]	t_{RRH}	0	–	0	–	0	–	ns
Write command hold time	t_{WCH}	10	–	10	–	15	–	ns
Write command pulse width	t_{WP}	10	–	10	–	15	–	ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	–	15	–	20	–	ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	–	15	–	20	–	ns
Data setup time [9]	t_{DS}	0	–	0	–	0	–	ns
Data hold time [9]	t_{DH}	10	–	15	–	15	–	ns
Refresh period	t_{REF}	–	8	–	8	–	8	ms
Refresh period L-version	t_{REF}	–	64	–	64	–	–	ms
Write command setup time [10]	t_{WCS}	0	–	0	–	0	–	ns
$\overline{CAS}$ to $\overline{WE}$ delay time [10]	t_{CWD}	40	–	45	–	50	–	ns
$\overline{RAS}$ to $\overline{WE}$ delay time [10]	t_{RWD}	75	–	90	–	100	–	ns
Column address to $\overline{WE}$ delay time [10]	t_{AWD}	50	–	60	–	65	–	ns
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CSR}	5	–	5	–	5	–	ns
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CHR}	10	–	15	–	15	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	0	–	0	–	0	–	ns

AC Characteristics (cont'd) [4) 13)]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		-50		-60		-70		
		min.	max.	min.	max.	min.	max.	
$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ counter test cycle)	t_{CPT}	25	–	30	–	40	–	ns
$\overline{OE}$ access time	t_{OEA}	–	15	–	15	–	20	ns
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	10	–	10	–	10	–	ns
Output buffer turn-off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	20	0	20	ns
Data to $\overline{CAS}$ low delay [14)]	t_{DZC}	0	–	0	–	0	–	ns
$\overline{CAS}$ high to data delay [15)]	t_{DZO}	0	–	0	–	0	–	
$\overline{OE}$ high to data delay [15)]	t_{CDD}	15	–	20	–	20	–	ns
$\overline{OE}$ to data delay [15)]	t_{ODD}	15	–	20	–	20	–	ns

Capacitance

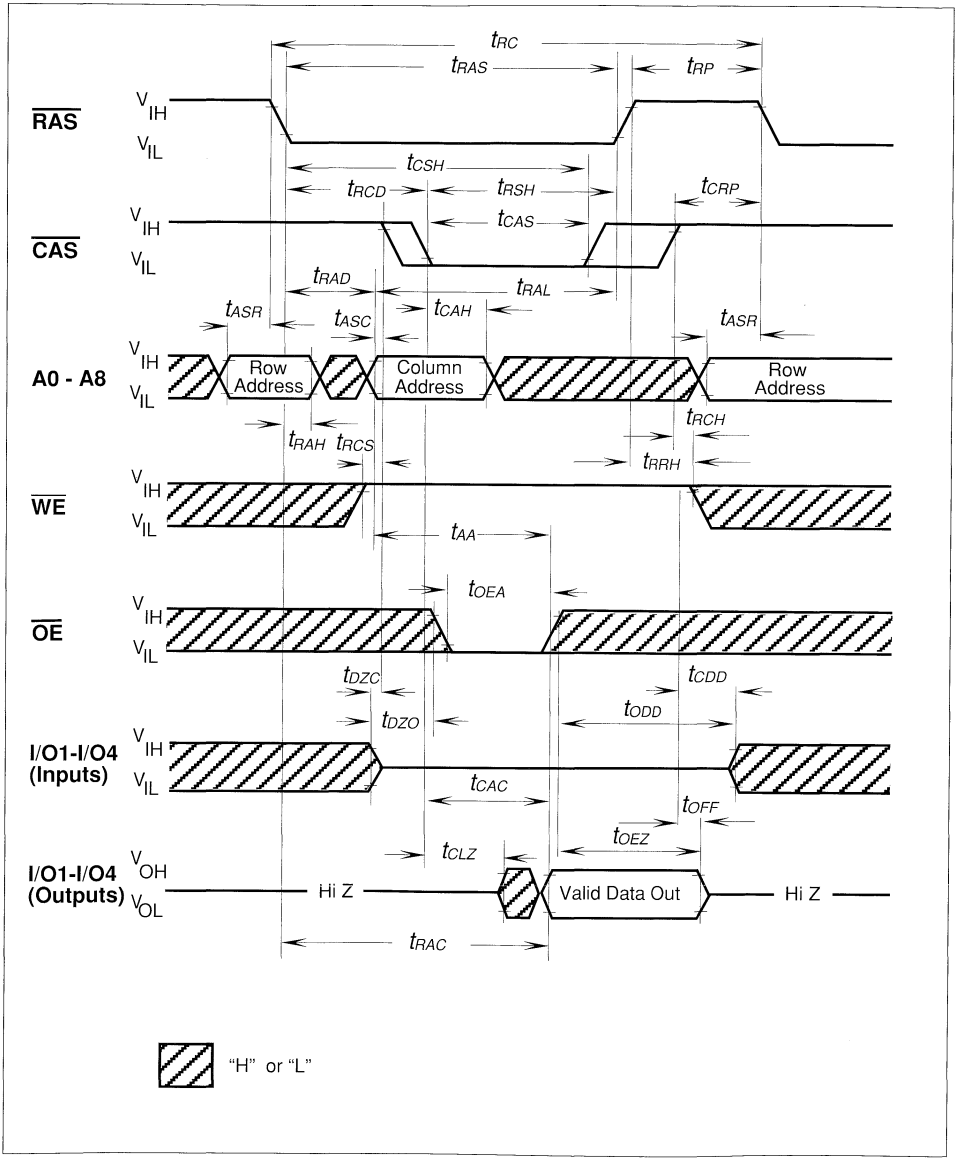
T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A8)	C_{I1}	–	5	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}	–	7	pF
Output capacitance (I/O1 ... I/O4)	C_{SO}	–	7	pF

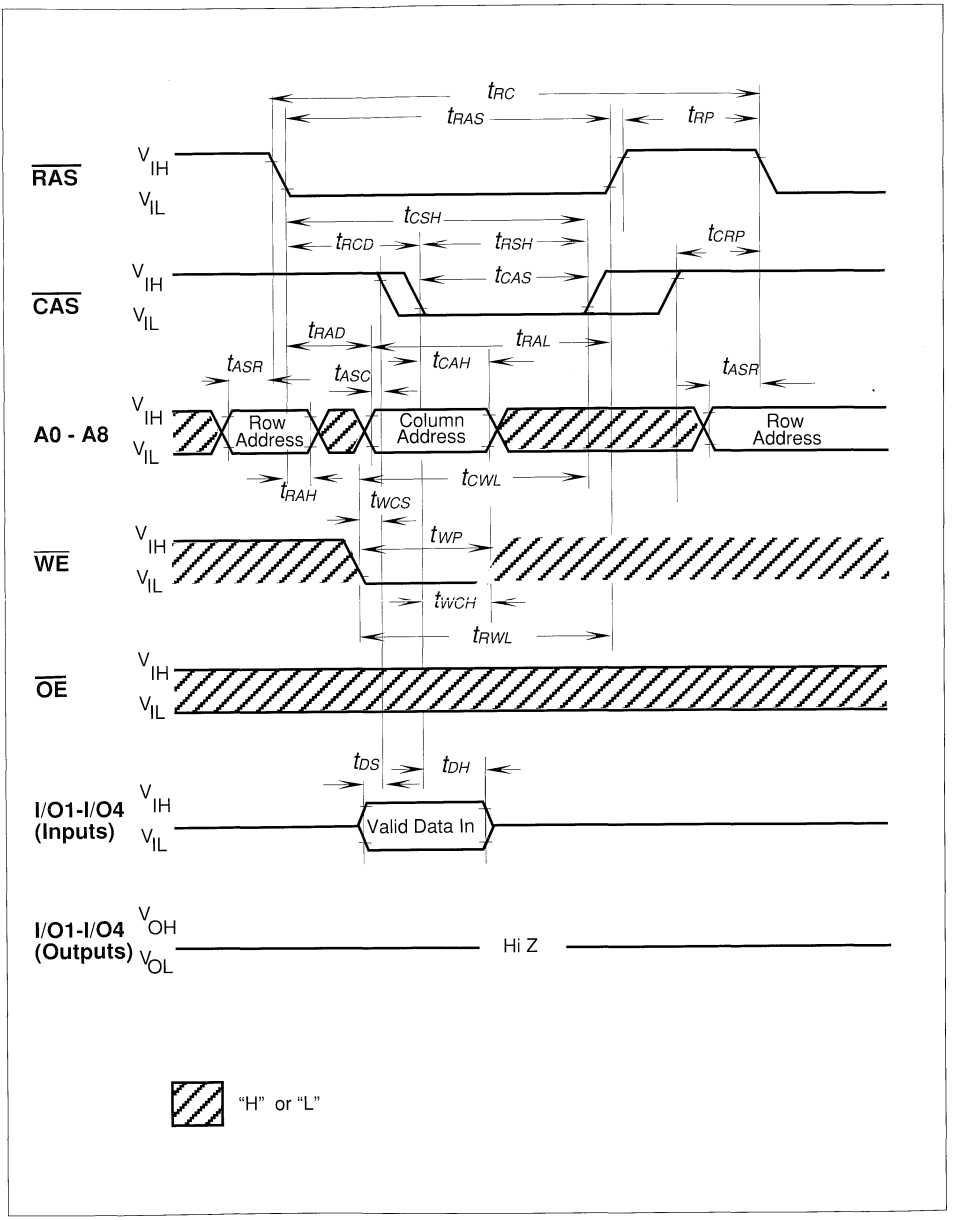
Notes :

1) All voltages are referenced to V_{SS}.
2) I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} and I_{CC7} depend on cycle rate.
3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.
4) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
5) V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.
6) Measured with a load equivalent to 2 TTL loads and 100 pF.
7) t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open-circuit conditions and is not referenced to output voltage levels.
8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9) These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-modify-write cycles.
10) t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.) and $t_{AWD} \geq t_{AWD}$ (min.), the cycle is a read-modify-write cycle and I/O will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of I/O (at access time) is indeterminate.
11) Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
12) Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.
13) AC measurements assume t_T = 5ns.
14) Either t_{DZC} or t_{DZO} must be satisfied.
15) Either t_{CDD} or t_{ODD} must be satisfied.

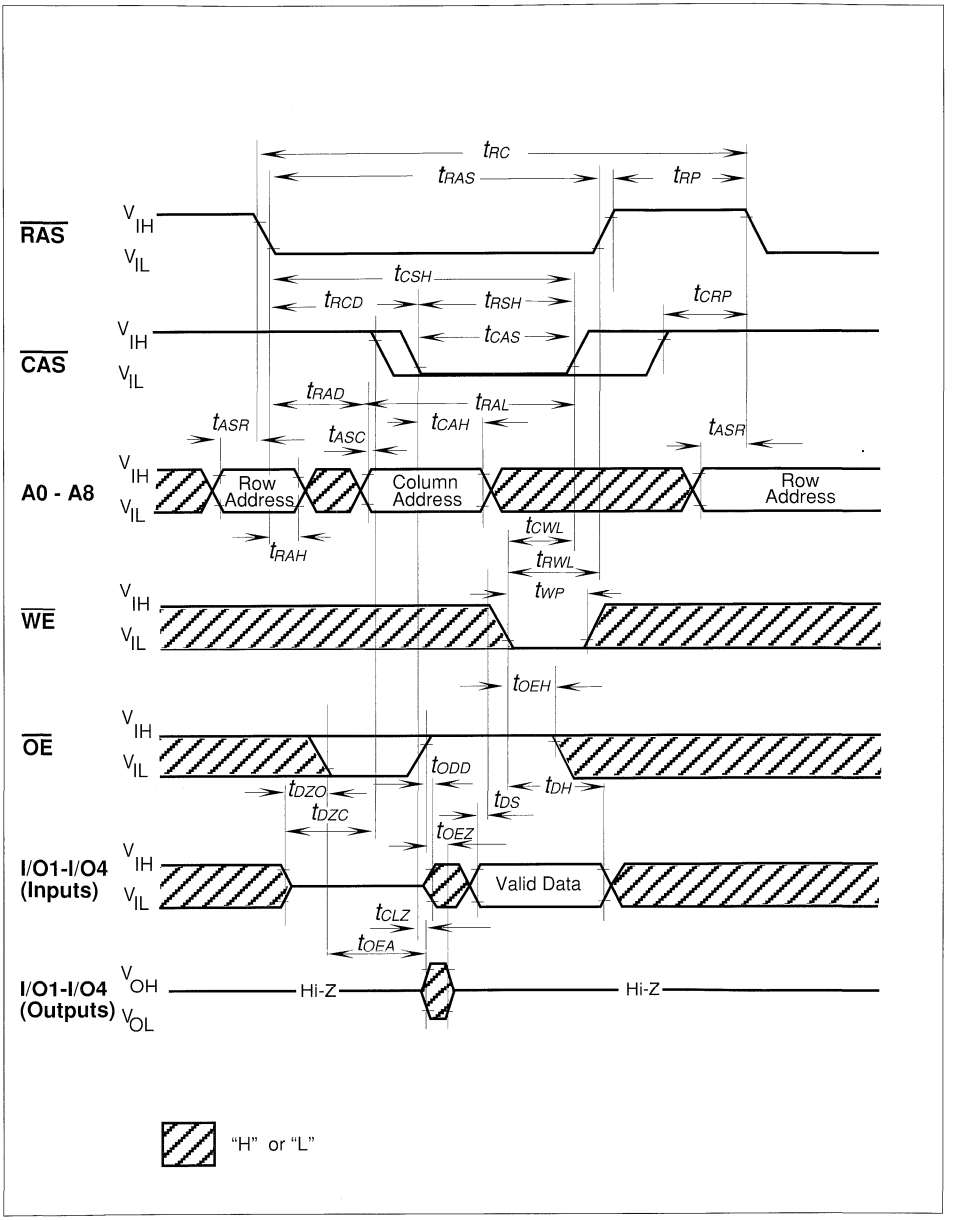
Waveforms



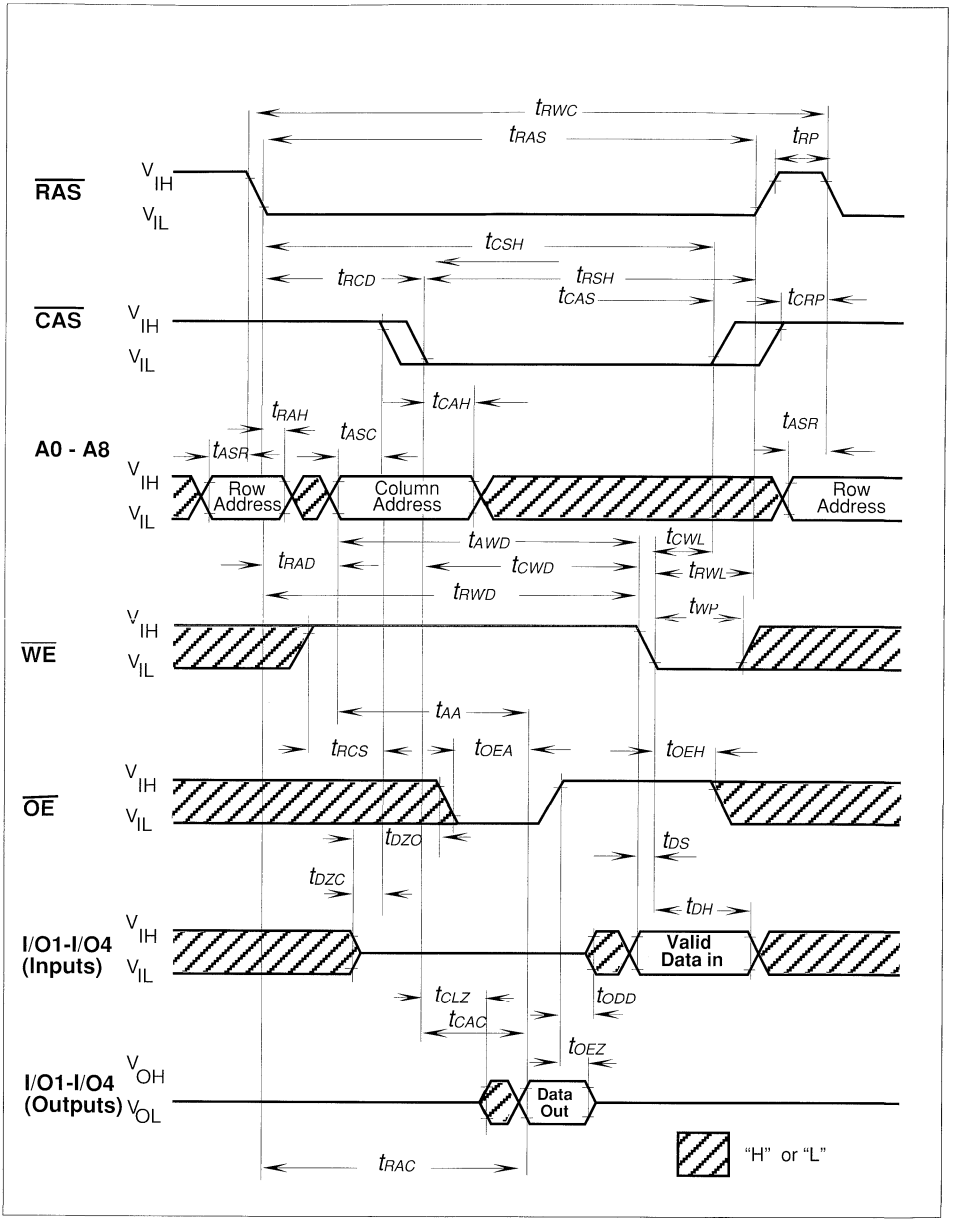
Read Cycle



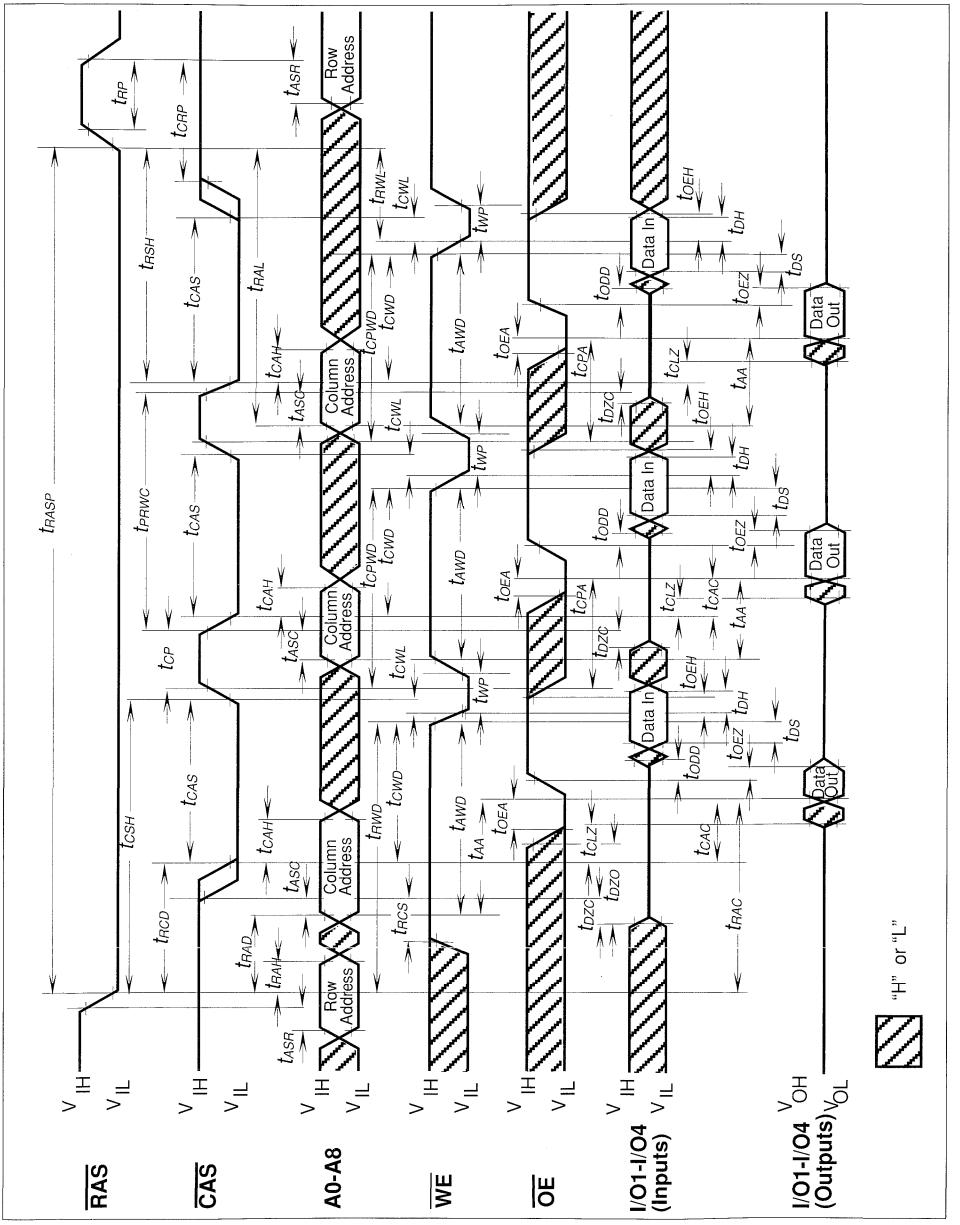
Write Cycle (Early Write)



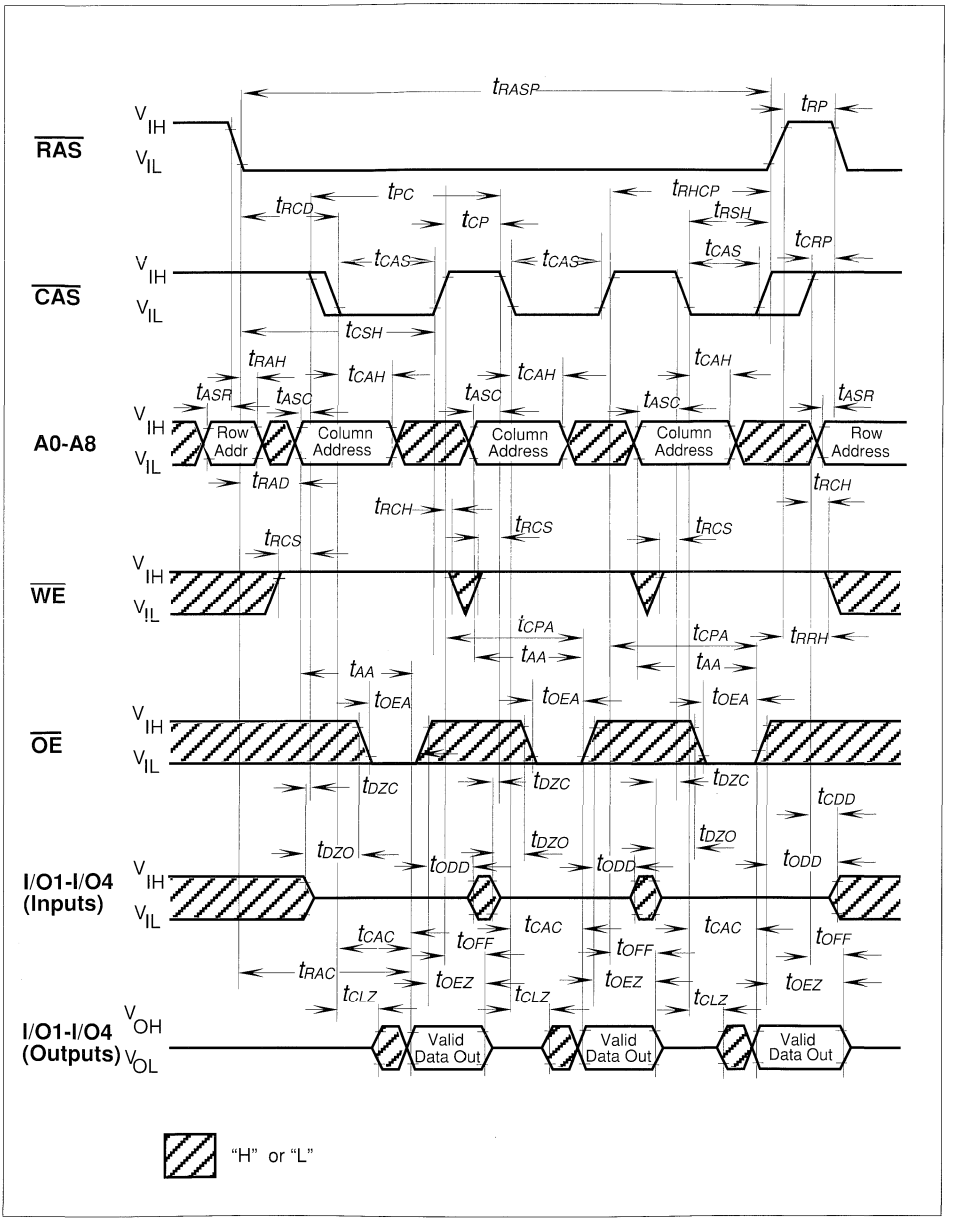
Write Cycle ($\overline{OE}$ Controlled Write)



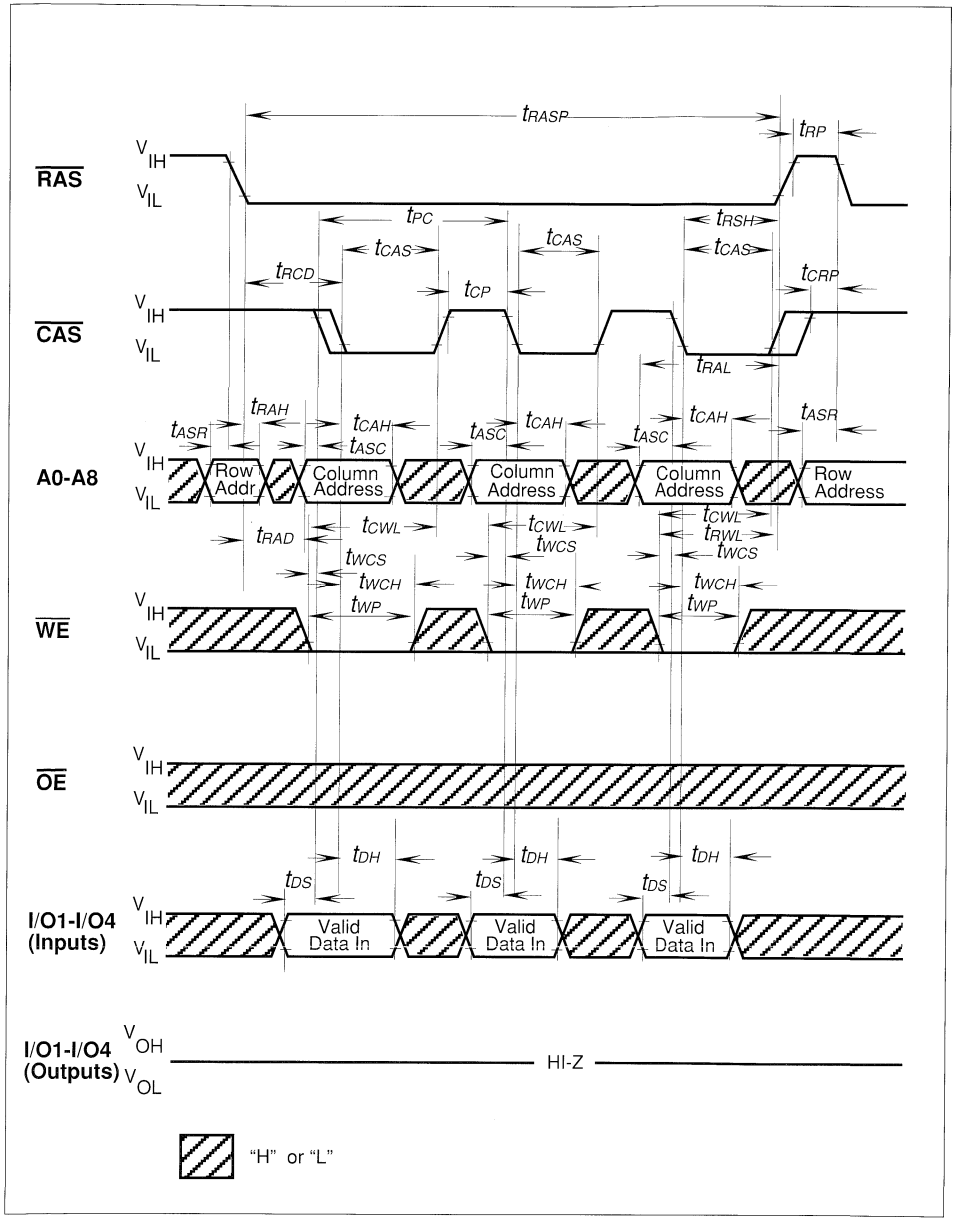
Read-Write (Read-Modify-Write) Cycle



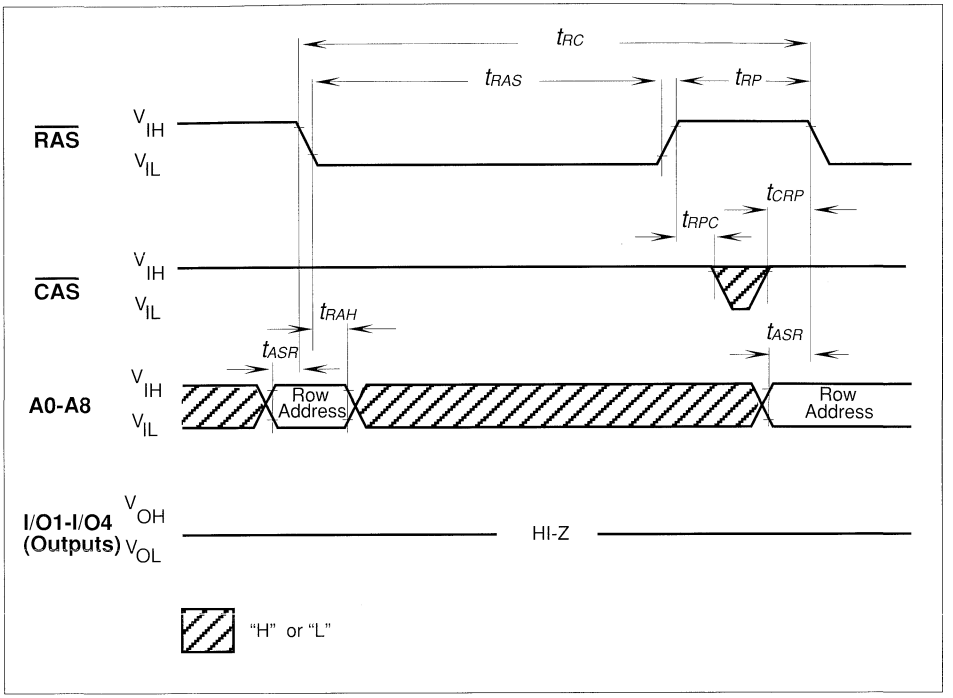
Fast Page Mode Read-Modify-Write Cycle



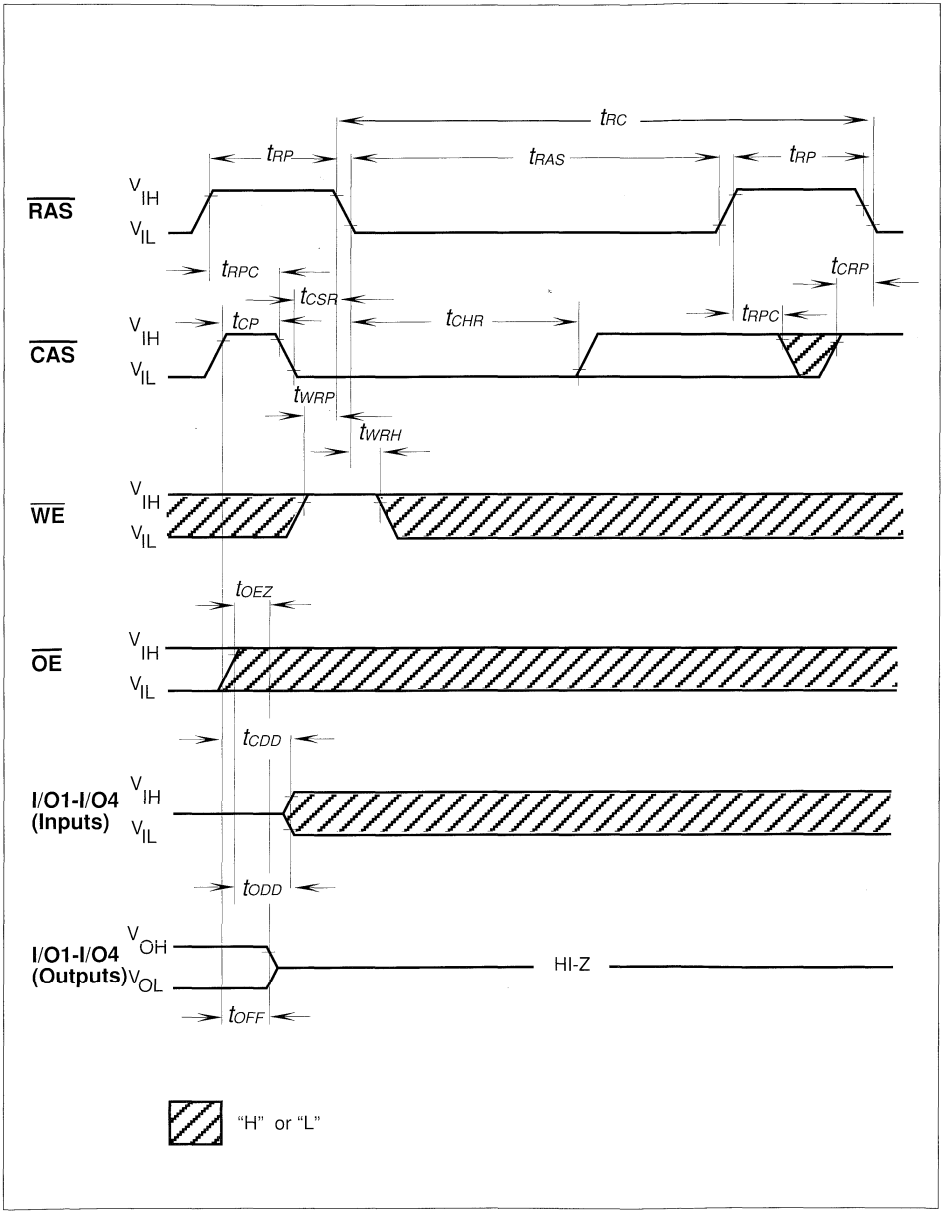
Fast Page Mode Read Cycle



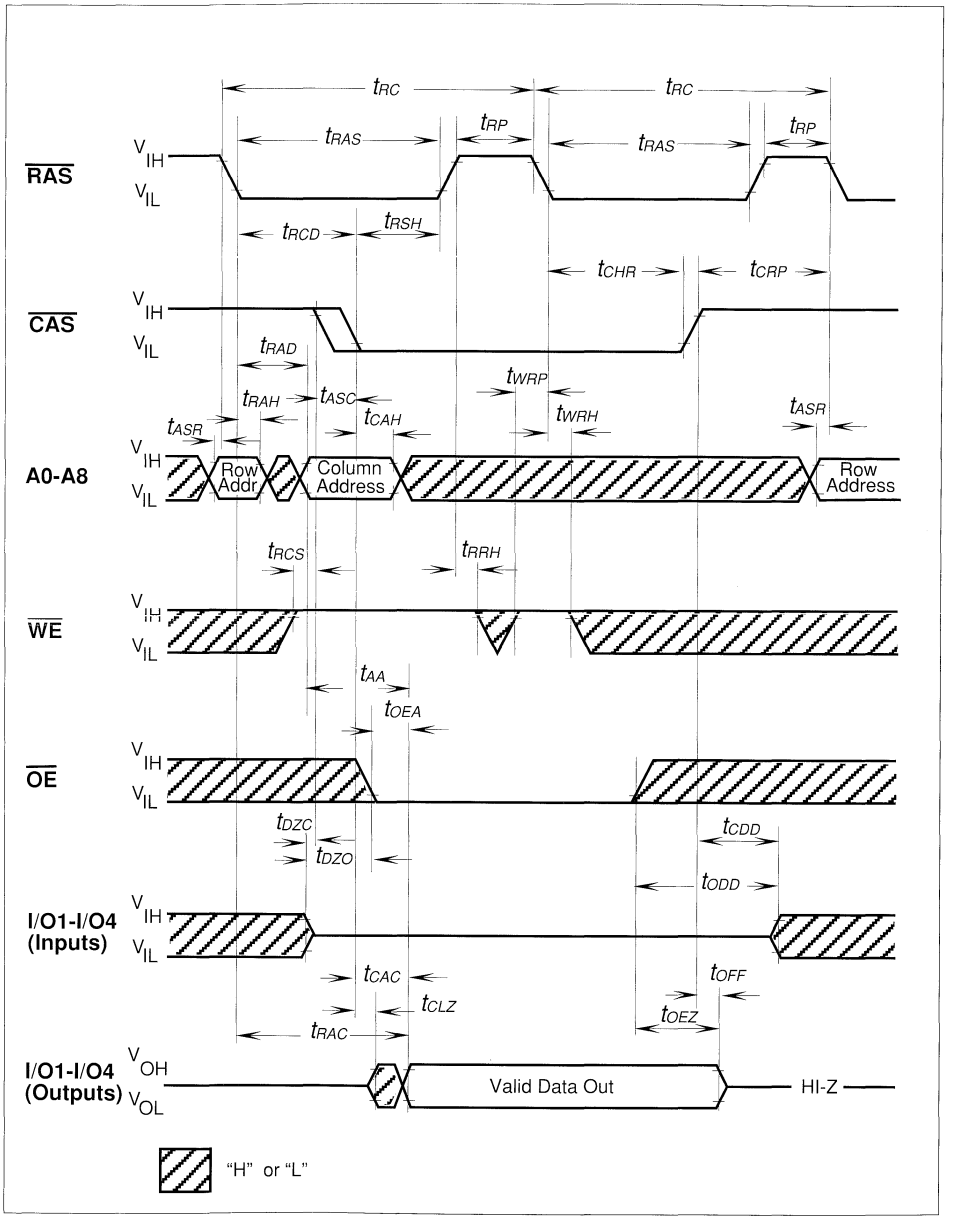
Fast Page Mode Early Write Cycle



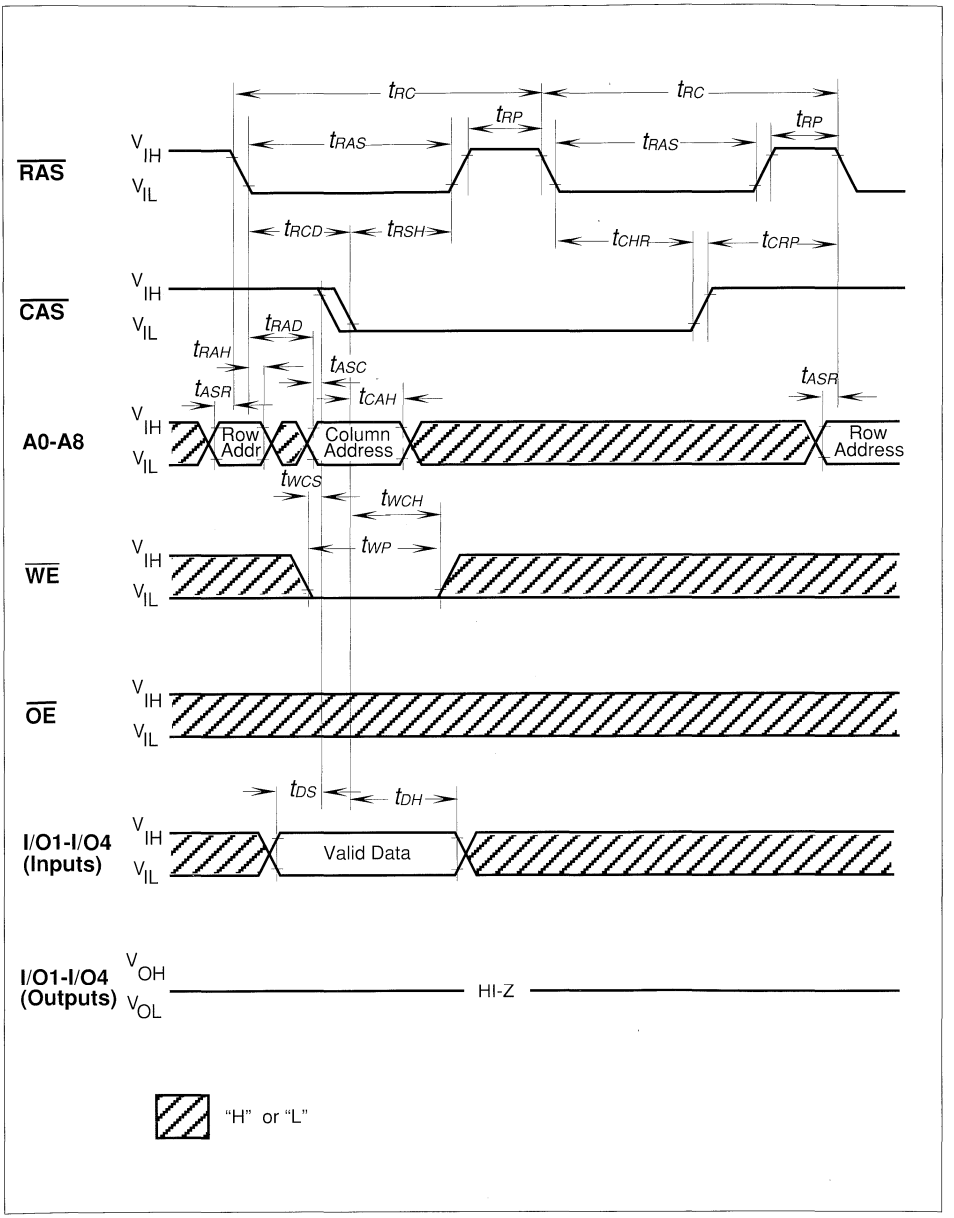
RAS-Only Refresh Cycle



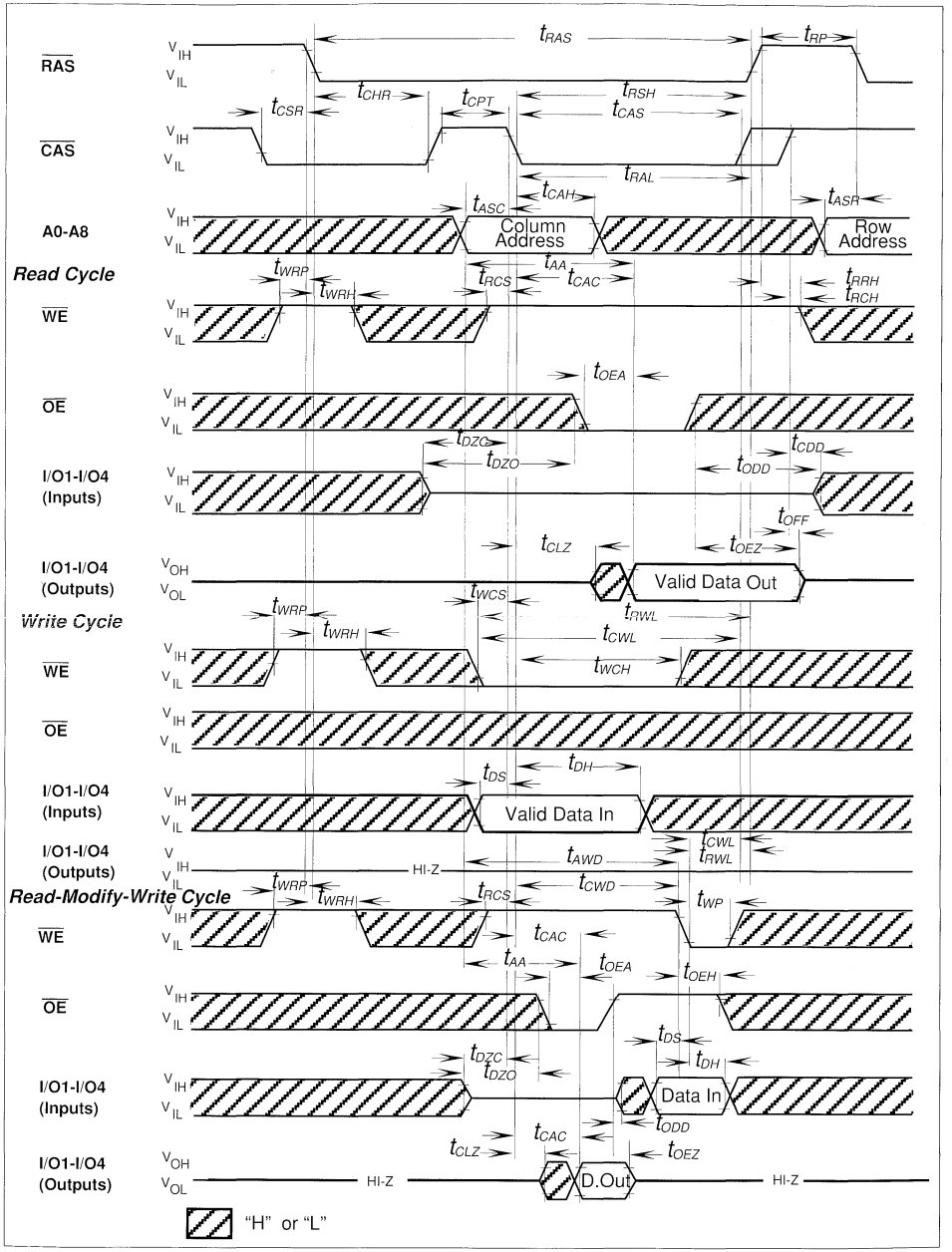
CAS-Before-RAS Refresh Cycle



Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Early Write)


RAS
CAS
A0-A8
Read Cycle
WE
OE
I/O1-I/O4 (Inputs)
I/O1-I/O4 (Outputs)
Write Cycle
Read-Modify-Write Cycle
tRAS
tRP
tCSR
tCHR
tCPT
tRSH
tCAS
tRAL
tCAH
tASC
tASR
Column Address
Row Address
tWRP
tWRH
tRCS
tAA
tCAC
tRRH
tRCH
tOEA
tDZC
tDZO
tCDD
tODD
tOFF
tCLZ
tOEZ
Valid Data Out
tWCS
tRWL
tCWL
tWCH
tDS
tDH
Valid Data In
tAWD
HI-Z
tCWD
tWP
tOEH
Data In
D.Out
"H" or "L"

4M x 1-Bit Dynamic RAM
Low Power 4M x 1-Bit Dynamic RAM

HYB 514100BJ/BT -50/-60/-70
HYB 514100BJL/BTL -50/-60/-70

Advanced Information

- 4 194 304 words by 1-bit organization
- 0 to 70 °C operating temperature
- Fast access time
  $\overline{RAS}$ access time:
  50 ns (-50 version)
  60 ns (-60 version)
  70 ns (-70 version)
  $\overline{CAS}$ access time:
  15 ns (-50,-60 version)
  20 ns (-70 version)
  Cycle time:
  95 ns (-50 version)
  110 ns (-60 version)
  130 ns (-70 version)
- Fast page mode cycle time
  35 ns (-50 version)
  40 ns (-60 version)
  45 ns (-70 version)
- Single + 5 V (± 10 %) supply with a built-in V_{bb} generator
- Low power dissipation
  max. 660 mW active (-50 version)
  max. 605 mW active (-60 version)
  max. 550 mW active (-70 version)
- Standby power dissipation:
  11 mW max. standby (TTL)
  5.5 mW max.standby (CMOS)
  1.1 mW max.standby (CMOS) for Low Power Version
- Output unlatched at cycle end allows two-dimensional chip selection
- Read, write, read-modify write, $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, hidden refresh, fast page mode capability and test mode capability
- All inputs and outputs TTL-compatible
- 1024 refresh cycles / 16 ms
- 1024 refresh cycles / 128 ms Low Power Version only
- Plastic Packages: P-SOJ-26/20-5 and P-TSOPII-26/20-1 with 300 mil width

Ordering Information

Type	Ordering Code	Package	Descriptions
HYB 514100BJ-50	Q67100-Q971	P-SOJ-26/20-5	DRAM (access time 50ns)
HYB 514100BJ-60	Q67100-Q759	P-SOJ-26/20-5	DRAM (access time 60 ns)
HYB 514100BJ-70	Q67100-Q760	P-SOJ-26/20-5	DRAM (access time 70 ns)
HYB 514100BJL-50	on request	P-SOJ-26/20-5	Low Power DRAM (access time 50 ns)
HYB 514100BJL-60	Q67100-Q1029	P-SOJ-26/20-5	Low Power DRAM (access time 60 ns)
HYB 514100BJL-70	Q67100-Q763	P-SOJ-26/20-5	Low Power DRAM (access time 70 ns)
HYB 514100BT-50	Q67100-Q2011	P-TSOPII-26/20-1	DRAM (access time 50 ns)
HYB 514100BT-60	Q67100-Q746	P-TSOPII-26/20-1	DRAM (access time 60 ns)
HYB 514100BT-70	Q67100-Q747	P-TSOPII-26/20-1	DRAM (access time 70 ns)
HYB 514100BTL-50	on request	P-TSOPII-26/20-1	Low Power DRAM (access time 50 ns)
HYB 514100BTL-60	on request	P-TSOPII-26/20-1	Low Power DRAM (access time 60 ns)
HYB 514100BTL-70	on request	P-TSOPII-26/20-1	Low Power DRAM (access time 70 ns)

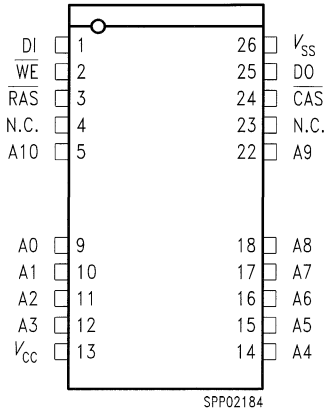
The HYB 514100BJ/BJL/BT/BTL is the new generation dynamic RAM organized as 4 194 304 words by 1-bit. The HYB 514100BJ/BJL/BT/BTL utilizes CMOS silicon gate process as well as advances circuit techniques to provide wide operation margins, both internally and for the system user. Multiplexed address inputs permit the HYB 514100BJ/BJL/BT/BTL to be packed in a standard plastic P-SOPJ-26/20 or P-TSOPII-26/20 package. This package size provides high system bit densities and is compatible with commonly used automatic testing and insertion equipment. System oriented feature include single + 5 V (± 10 %) power supply, direct interfacing with high performance logic device families such as Schottky TTL.

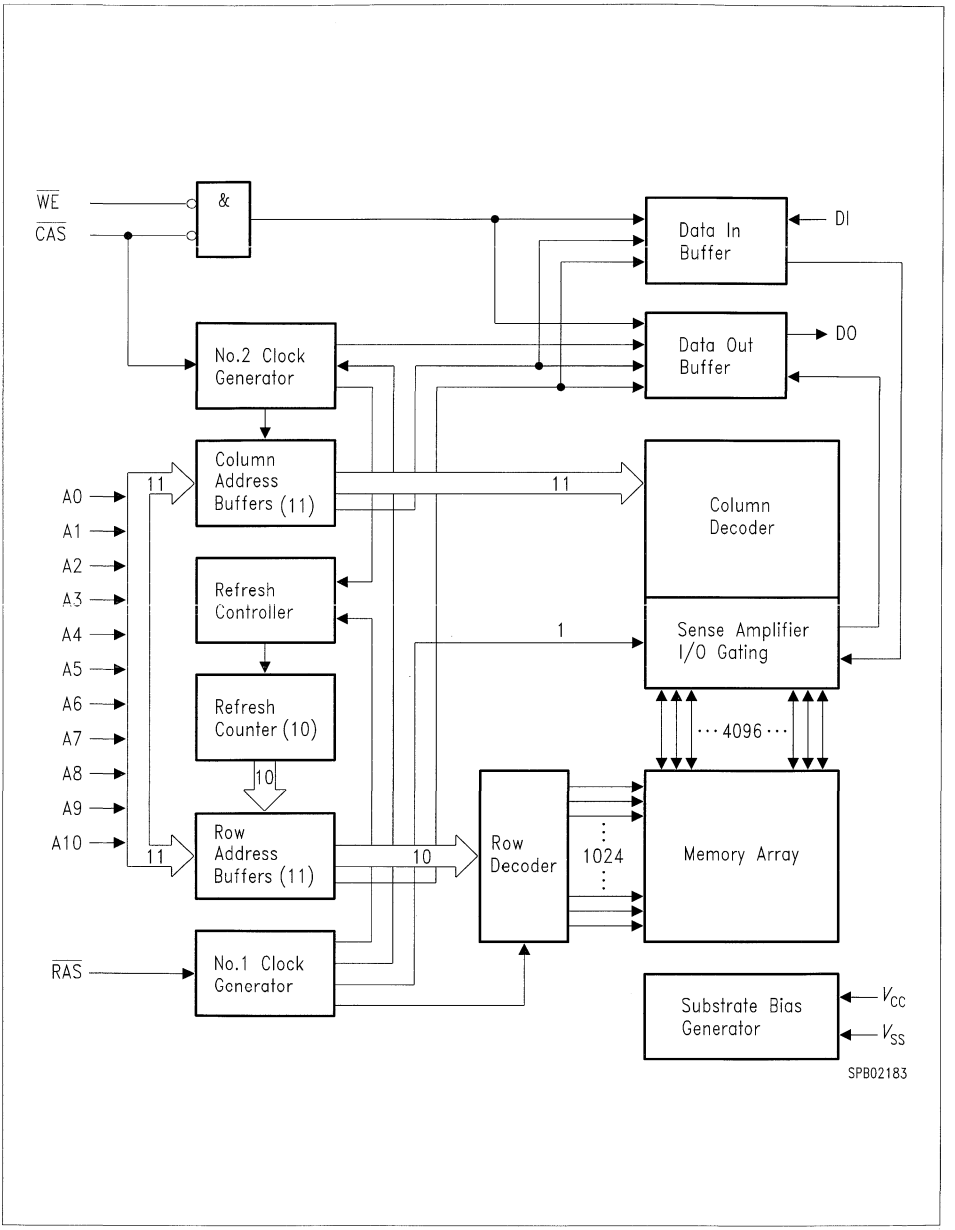
Pin Definitions and Functions

Pin No.	Function
A0-A10	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Input
DI	Data In
DO	Data Out
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground (0 V)
N.C.	No Connection

Pin Configuration
(top view)

P-SOJ-26/20-5
P-TSOPII-26/20-1





Block Diagram

Absolute Maximum Ratings

Operating temperature range ..... 0 to 70 °C
Storage temperature range ..... – 55 to + 150 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 1 to + 7 V
Power Supply voltage ..... – 1 to + 7 V
Data out current (short circuit) ..... 50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{ih}	2.4	6.5	V	1)
Input low voltage	V_{il}	– 1.0	0.8	V	1)
Output high voltage (I_{OUT} = – 5 mA)	V_{oh}	2.4	–	V	1)
Output low voltage (I_{OUT} = 4.2 mA)	V_{ol}	–	0.4	V	1)
Input leakage current, any input (0 V < V_{in} < 7, all other input = 0 V)	$I_{I(L)}$	– 10	10	µA	1)
Output leakage current (DO is disabled, 0 < V_{OUT} < V_{CC})	$I_{o(L)}$	– 10	10	µA	1)
Average V_{CC} supply current	I_{CC1}			mA	2) 3)
-50 version		–	120		
-60 version		–	110		
-70 version		–	100		
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = $\overline{WE}$ = V_{ih})	I_{CC2}	–	2	mA	–
Average V_{CC} supply current during $\overline{RAS}$-only refresh cycles	I_{CC3}			mA	2)
-50 version		–	120		
-60 version		–	110		
-70 version		–	100		
Average V_{CC} supply current during fast page mode operation	I_{CC4}			mA	2) 3)
-50 version		–	80		
-60 version		–	70		
-70 version		–	60		

DC Characteristics (cont'd)

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = $\overline{WE}$ = V_{CC} – 0.2 V)	I_{CC5}	–	1	mA	1)
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = $\overline{WE}$ = V_{CC} – 0.2 V) for Low Power Version	I_{CC5}	–	200	µA	–
Average V_{CC} supply current during $\overline{CAS}$ before $\overline{RAS}$ refresh mode	I_{CC6}			mA	2)
-50 version		–	120		
-60 version		–	110		
-70 version		–	100		
For Low Power Version only: Battery backup current (average power supply current in battery backup mode): ($\overline{CAS}$ = $\overline{CAS}$ before $\overline{RAS}$ cycling or 0.2 V, $\overline{WE}$ = V_{CC} – 0.2 V or 0.2 V, A0 to A10 = V_{CC} – 0.2 V or 0.2 V; DI = V_{CC} – 0.2 V or 0.2 V or open, t_{RC} = 125 µs, t_{RAS} = t_{RAS} min = 1 µs)	I_{CC7}	–	300	µA	–

AC Characteristics [4)13)]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		-50		-60		-70		
		min.	max.	min.	max.	min.	max.	
Random read or write time	t_{RC}	95	–	110	–	130	–	ns
Read-write cycle time	t_{RWC}	115	–	130	–	155	–	ns
Fast page mode cycle time	t_{PC}	35	–	40	–	45	–	ns
Fast page mode read/write cycle time	t_{PRWC}	55	–	60	–	70	–	ns
Access time from $\overline{RAS}$ [6) 11)]	t_{RAC}	–	50	–	60	–	70	ns
Access time from $\overline{CAS}$ [6) 11)]	t_{CAC}	–	15	–	15	–	20	ns
Access time from column address [6) 12)]	t_{AA}	–	25	–	30	–	35	ns
Access time from $\overline{CAS}$ precharge [6)]	t_{CPA}	–	30	–	35	–	40	ns
$\overline{CAS}$ to output in low-Z [6)]	t_{CLZ}	0	–	0	–	0	–	ns
Output buffer turn-off delay from $\overline{CAS}$ [7)]	t_{OFF}	0	15	0	20	0	20	ns
Transition time (rise and fall) [5)]	t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	35	–	40	–	50	–	ns
$\overline{RAS}$ pulse width	t_{RAS}	50	10000	60	10000	70	10000	ns
$\overline{RAS}$ pulse width in fast page mode	t_{RASP}	50	200000	60	200000	70	200000	ns
$\overline{RAS}$ hold time	t_{RSH}	15	–	15	–	20	–	ns
$\overline{CAS}$ hold time	t_{CSH}	50	–	60	–	70	–	ns
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge (Fast page mode)	t_{RHCP}	30	–	35	–	45	–	ns
$\overline{CAS}$ precharge to $\overline{WE}$ delay time (FPM read-modify-write)	t_{CPWD}	30	–	35	–	40	–	ns
$\overline{CAS}$ pulse width	t_{CAS}	15	10000	15	10000	20	10000	ns

AC Characteristics (cont'd)[4)13)]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		-50		-60		-70		
		min.	max.	min.	max.	min.	max.	
$\overline{RAS}$ to $\overline{CAS}$ delay time [11)]	t_{RCD}	20	35	20	45	20	50	ns
$\overline{RAS}$ to column address delay time [12)]	t_{RAD}	15	25	15	30	15	35	ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	5	–	ns
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns
Row address hold time	t_{RAH}	10	–	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns
Column address hold time	t_{CAH}	10	–	15	–	15	–	ns
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	–	30	–	35	–	ns
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns
Read command hold time [8)]	t_{RCH}	0	–	0	–	0	–	ns
Read command hold time ref. to $\overline{RAS}$ [8)]	t_{RRH}	0	–	0	–	0	–	ns
Write command hold time	t_{WCH}	10	–	10	–	15	–	ns
Write command pulse width	t_{WP}	10	–	10	–	15	–	ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	–	15	–	20	–	ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	–	15	–	20	–	ns
Data setup time [9)]	t_{DS}	0	–	0	–	0	–	ns
Data hold time [9)]	t_{DH}	10	–	15	–	15	–	ns

AC Characteristics (cont'd)[4)13)]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		-50		-60		-70		
		min.	max.	min.	max.	min.	max.	
Refresh period	t_{REF}	–	16	–	16	–	16	ms
Refresh period Low Power Version	t_{REF}	–	128	–	128	–	128	ms
Write command setup time [10)]	t_{WCS}	0	–	0	–	0	–	ns
$\overline{CAS}$ to $\overline{WE}$ delay time [10)]	t_{CWD}	15	–	15	–	20	–	ns
$\overline{RAS}$ to $\overline{WE}$ delay time [10)]	t_{RWD}	50	–	60	–	70	–	ns
Column address to $\overline{WE}$ delay time [10)]	t_{AWD}	25	–	30	–	35	–	ns
$\overline{CAS}$ setup time (CBR cycle)	t_{CSR}	5	–	5	–	5	–	ns
$\overline{CAS}$ hold time (CBR cycle)	t_{CHR}	10	–	15	–	15	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	0	–	0	–	0	–	ns
$\overline{CAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$ counter test cycle)	t_{CPT}	25	–	30	–	40	–	ns
Write command setup time (test mode entry)	t_{WTS}	10	–	10	–	10	–	ns
Write command hold time (in test mode entry cycle)	t_{WTH}	10	–	10	–	10	–	ns
Write to $\overline{RAS}$ precharge time (CBR cycle)	t_{WRP}	10	–	10	–	10	–	ns
Write to $\overline{RAS}$ hold time (CBR cycle)	t_{WRH}	10	–	10	–	10	–	ns

Capacitance

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A10, DI)	C_{i1}	–	5	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{i2}	–	7	pF
Output capacitance (DO)	C_{io}	–	7	pF

Notes:

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1}, I_{CC4} depend on output loading.

4) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using the internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

5) V_{ih} (min.) and V_{il} (max.) are reference levels for measuring timing of input signals. Transition times are also measured between V_{ih} and V_{il}.

6) Measured with a load equivalent to 2 TTL loads and 100 pF.

7) t_{off} (max.) defines the time at which the output achieves the open-circuit conditions and are not referenced to output voltage levels.

8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

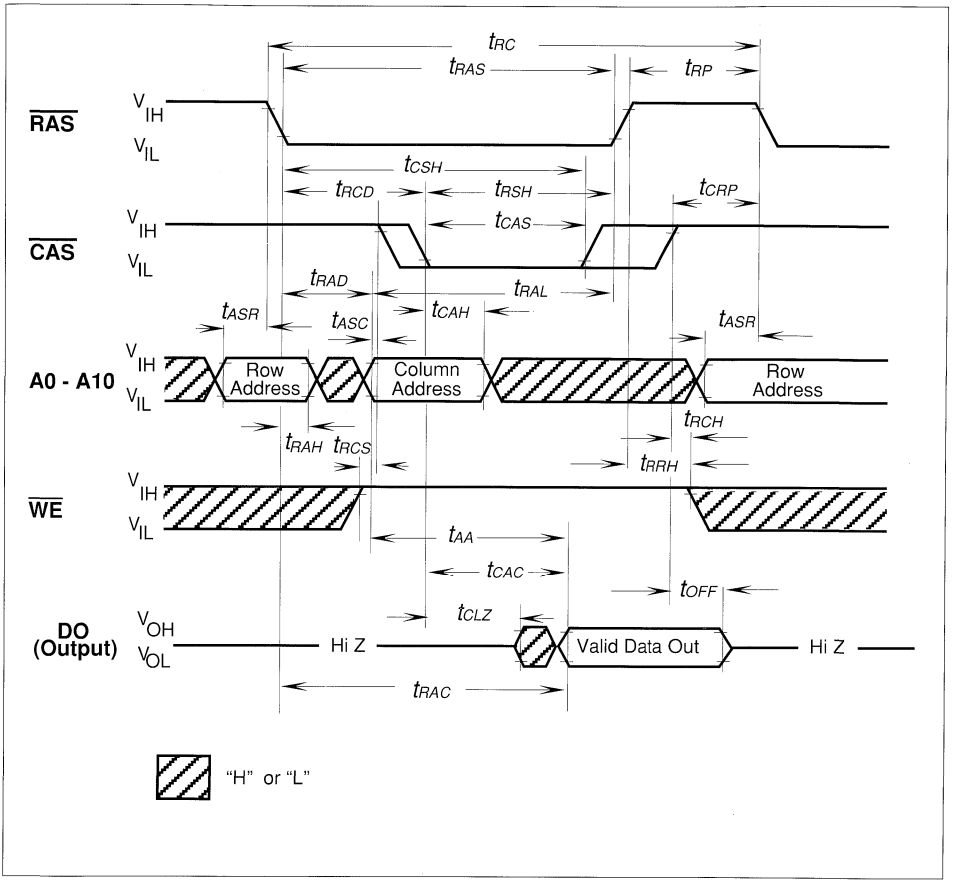
9) These parameters are references to the $\overline{CAS}$ leading edge in early write and to the $\overline{WE}$ leading edge in read-write cycles.

10) t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only.
If $t_{WCS} > t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} > t_{RWD}$ (min.), $t_{CWD} > t_{CWD}$ (min.) and $t_{AWD} > t_{AWD}$ (min.), the cycle is a read-write cycle and DO will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of D/O (at access time) is indeterminate.

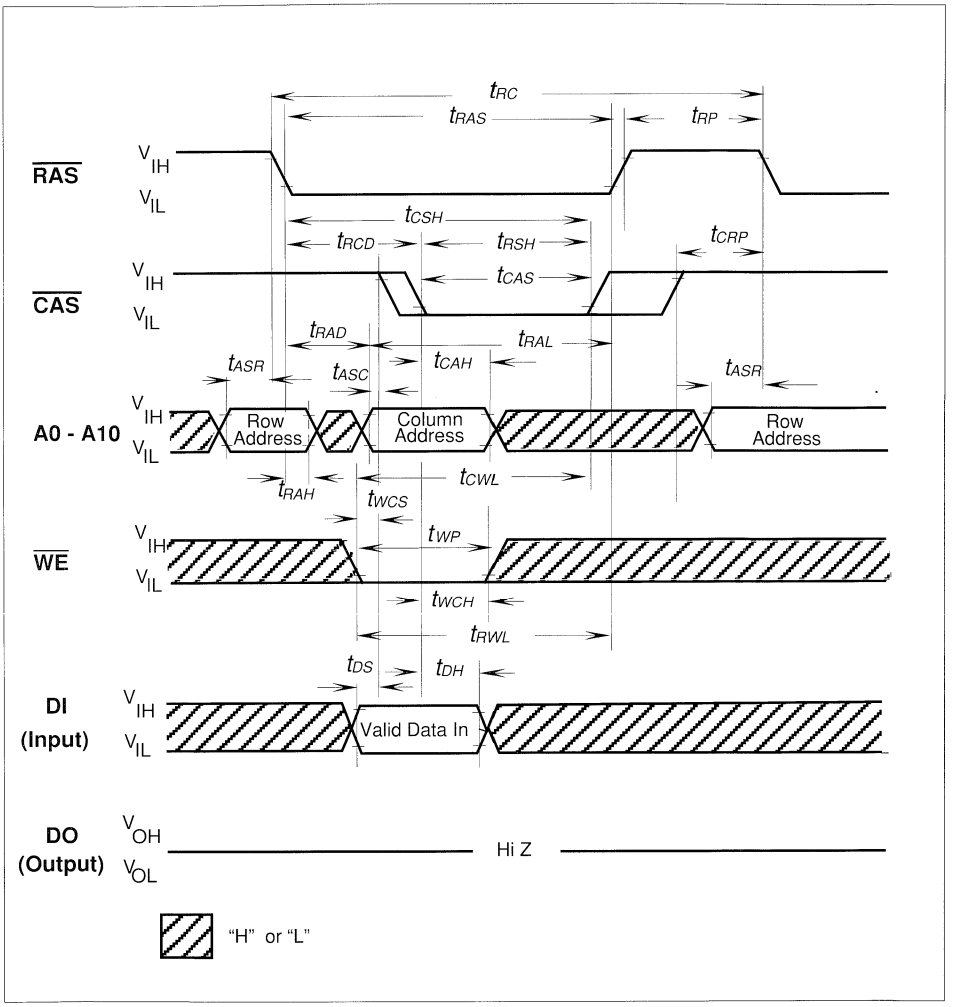
11) Operation within the t_{RCD} (max.) limit ensure that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

12) Operation within the t_{RAD} (max.) limit ensured that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

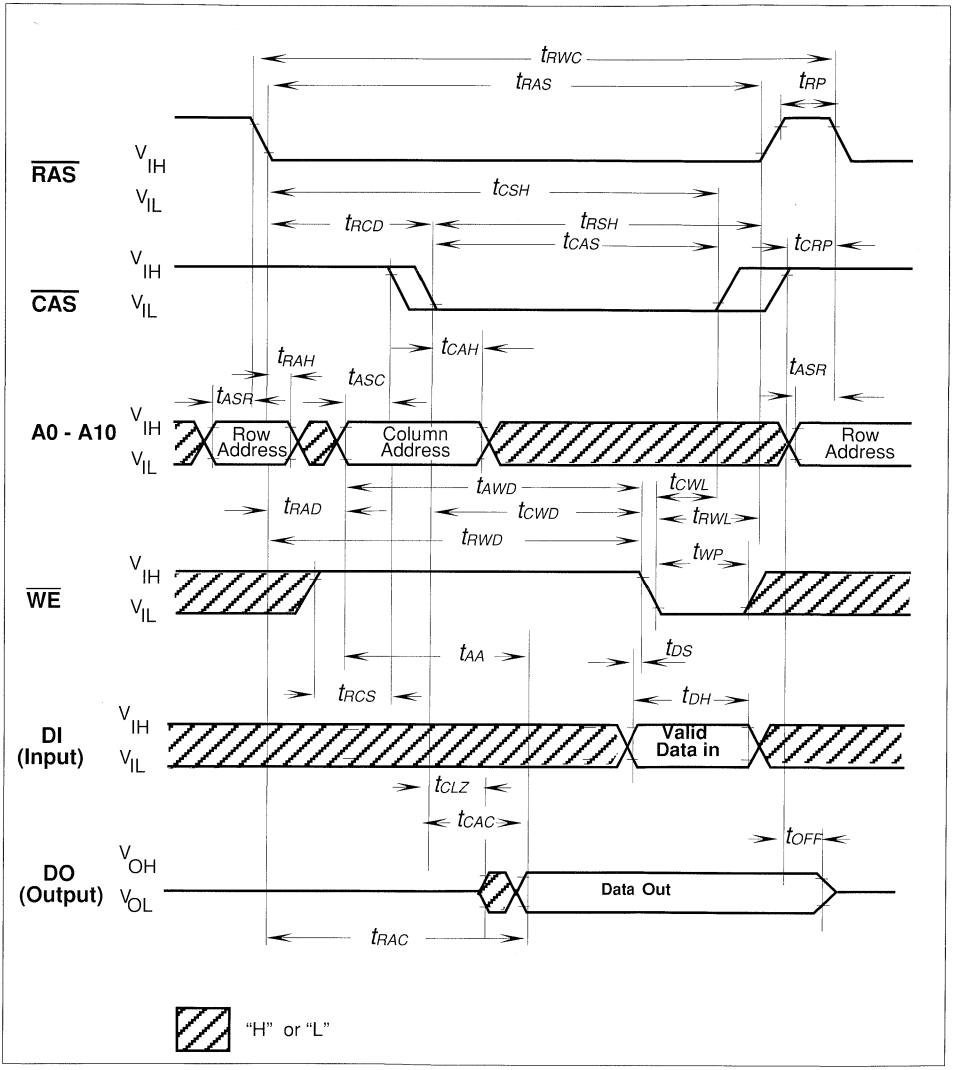
13) AC measurements assume t_T = 5 ns.


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tASR
tASC
tCAH
A0 - A10
Row Address
Column Address
Row Address
tRCH
tRAH
tRCS
tRRH
WE
tAA
tCAC
tOFF
tCLZ
DO (Output)
VOH
VOL
Hi Z
Valid Data Out
Hi Z
tRAC
"H" or "L"

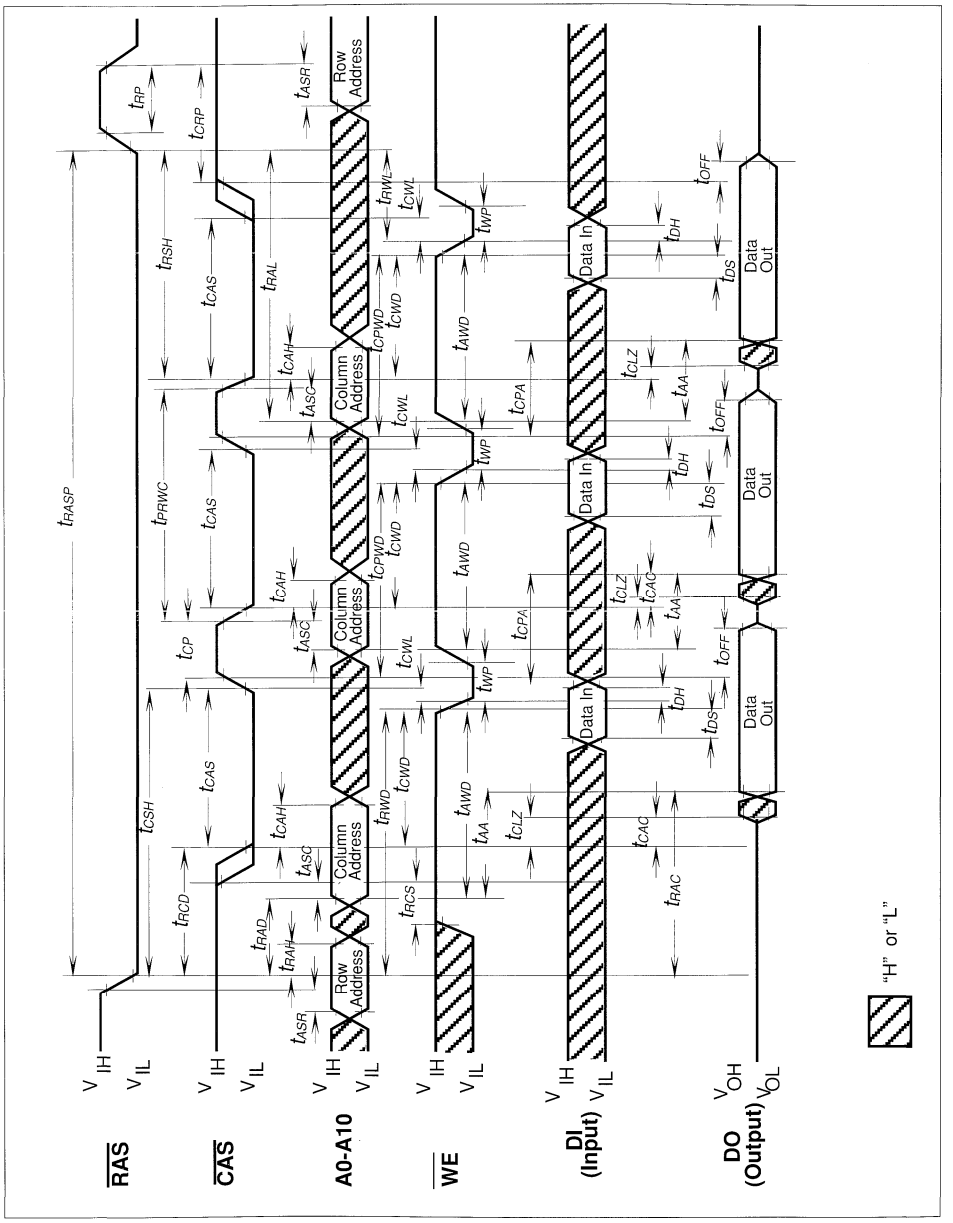
Read Cycle



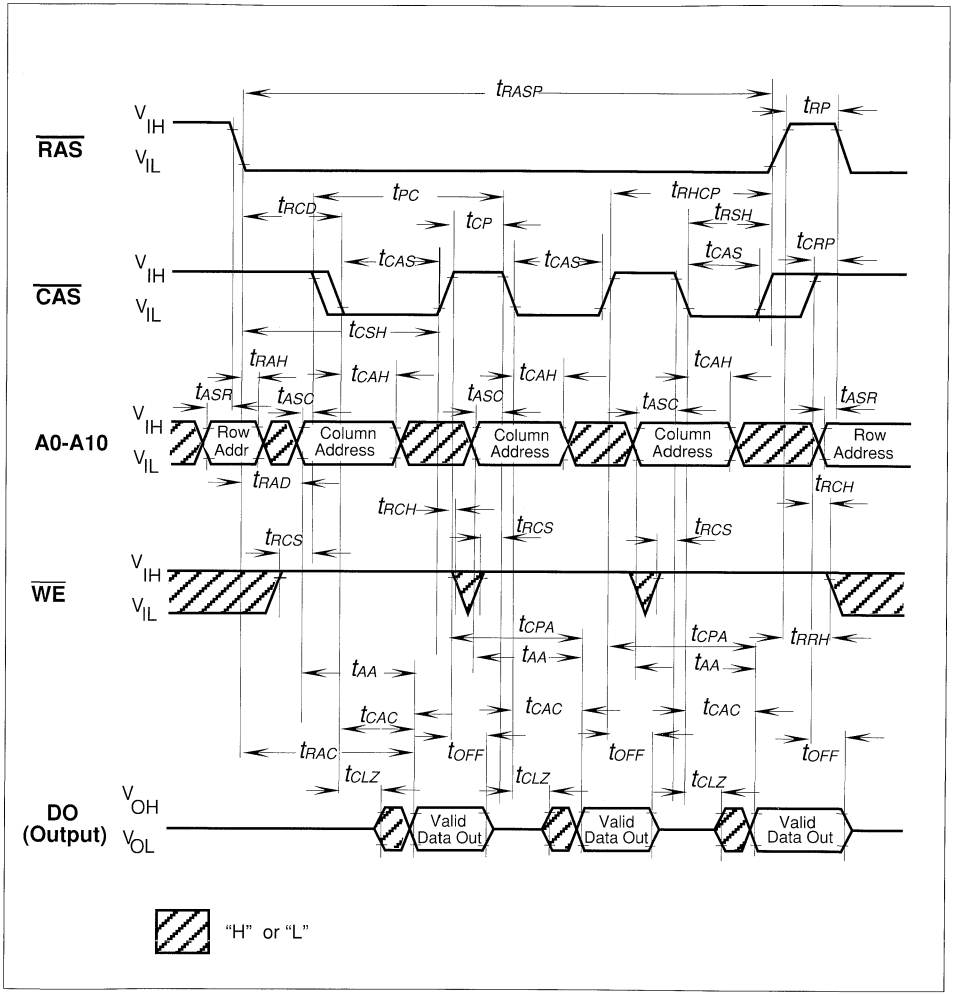
Write Cycle (Early Write)



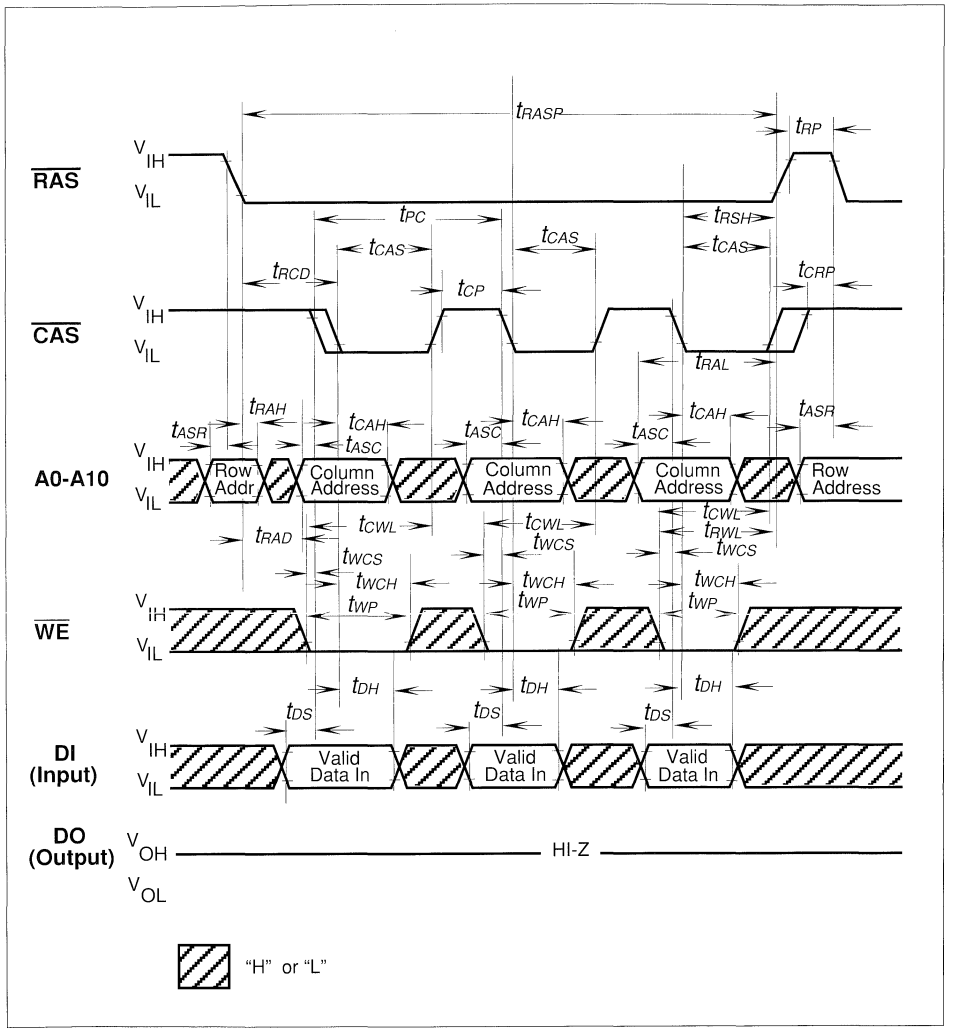
Read-Write (Read-Modify-Write) Cycle



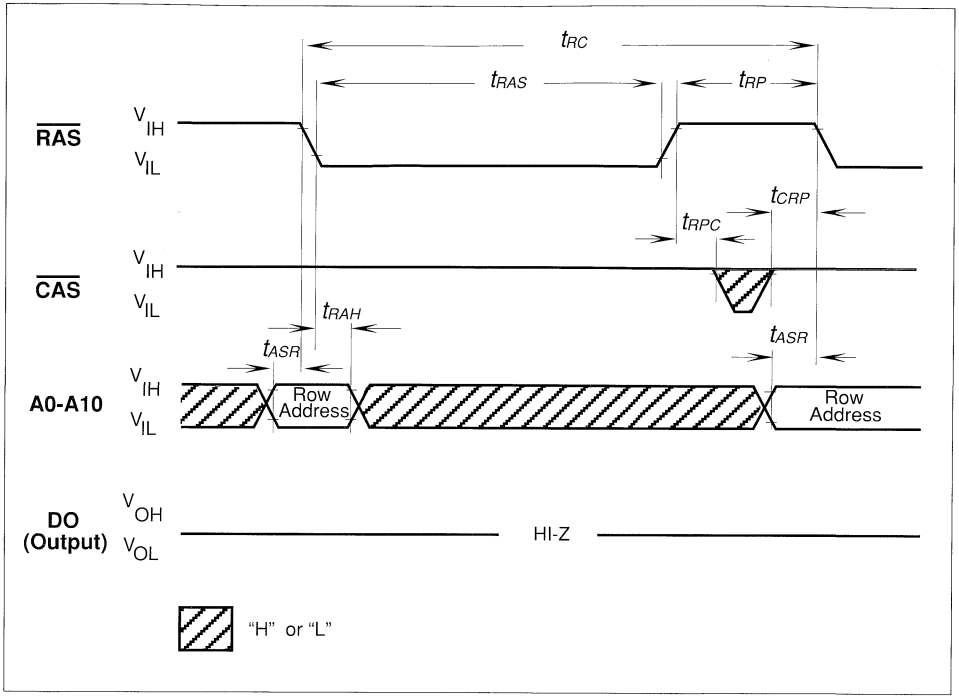
Fast Page Mode Read-Modify-Write Cycle



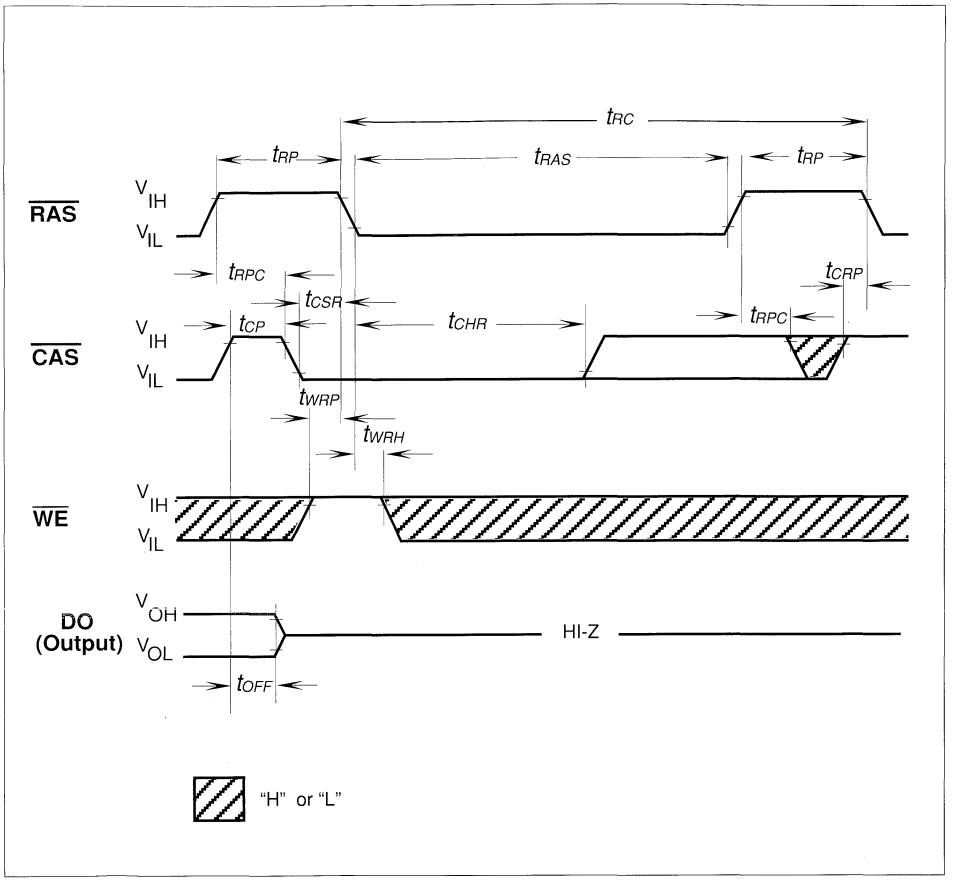
Fast Page Mode Read Cycle



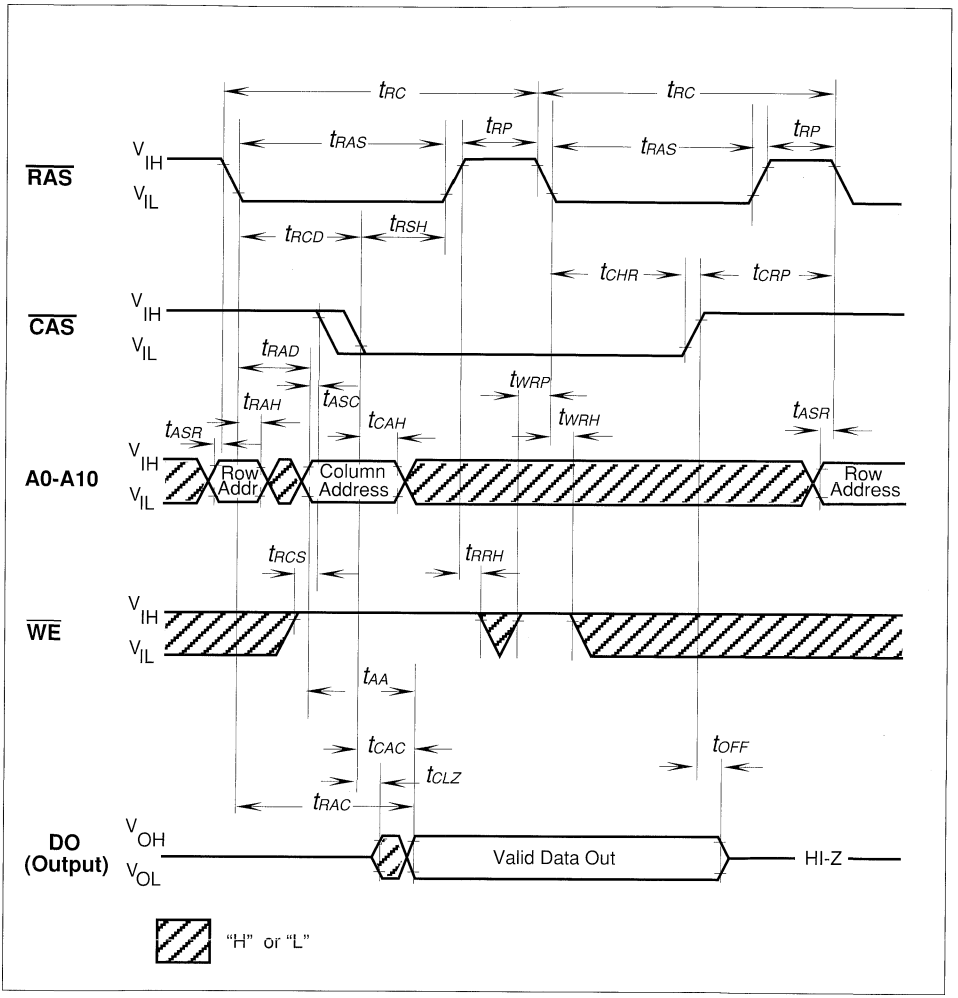
Fast Page Mode Early Write Cycle



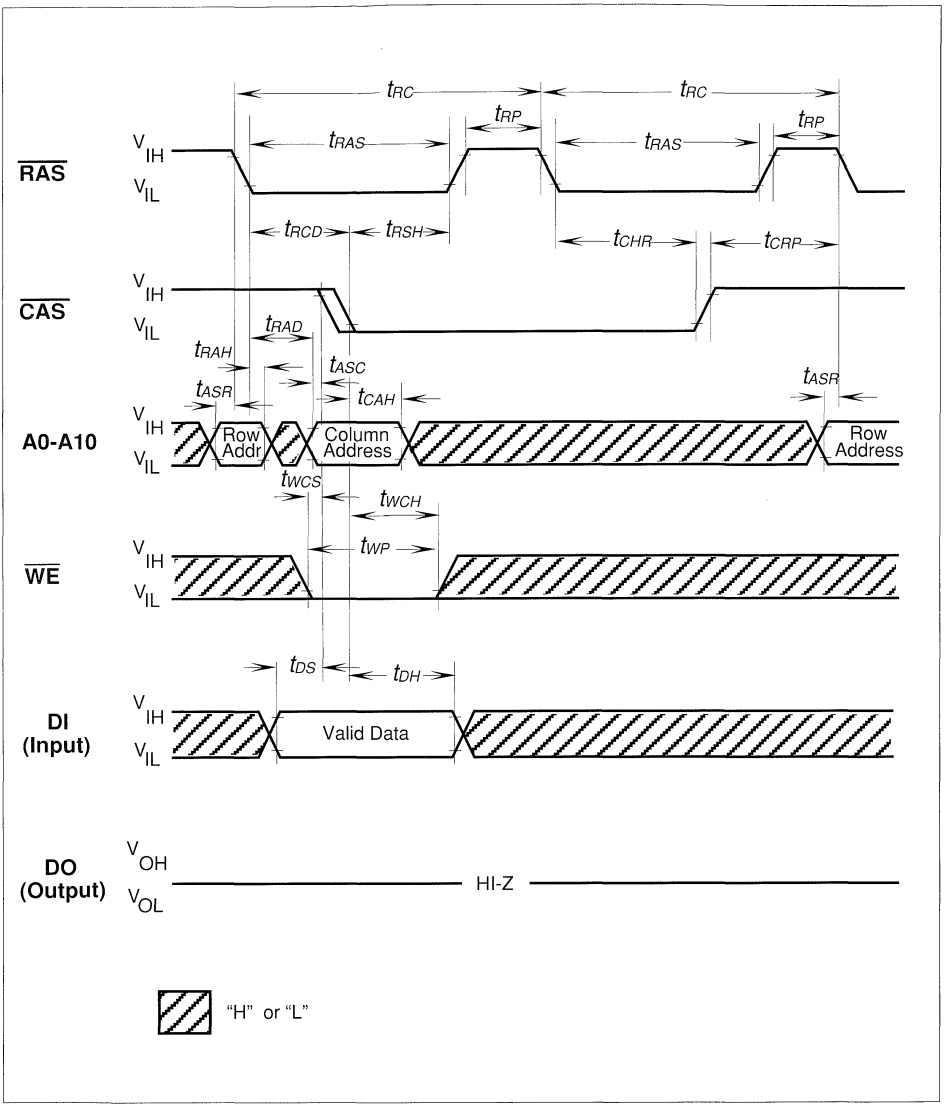
RAS-Only Refresh Cycle



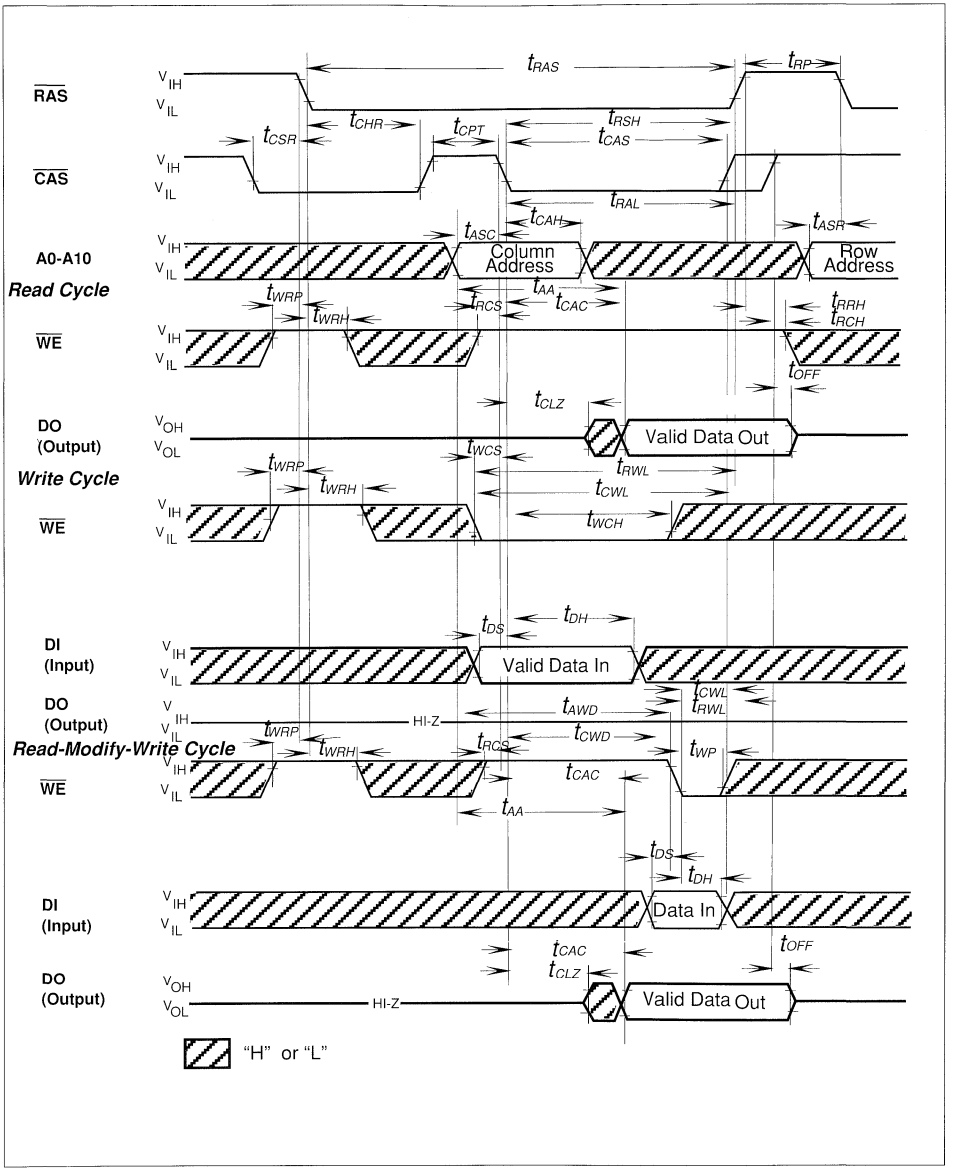
CAS-Before-RAS Refresh Cycle



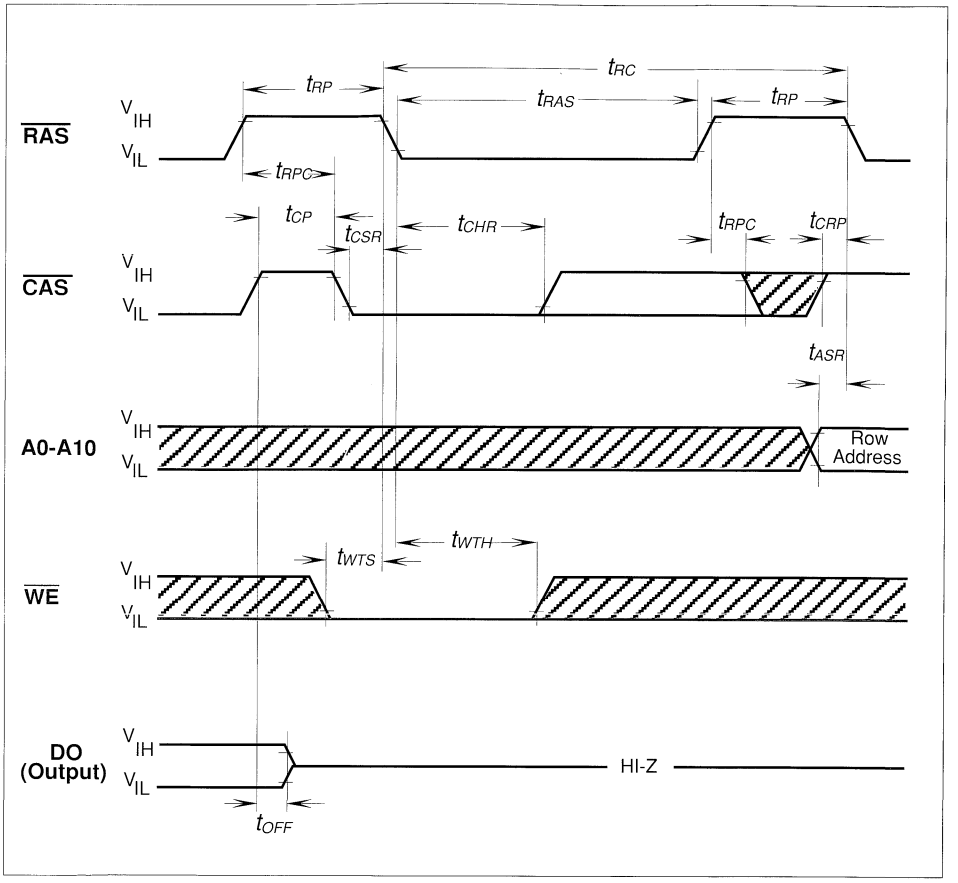
Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Early Write)



CAS-Before-RAS Refresh Counter Test Cycle



Test Mode Entry

Test Mode

The HYB514100BJ/BT/BJL/BTL is organized 4 194 304 words by 1- bit but can internally be configured as 524 288 words by 8-bits. A $\overline{WE}$, $\overline{CAS}$-before-$\overline{RAS}$ cycle puts the device into Test Mode.

In Test Mode, data is written into 8 sectors in parallel and retrieved the same way. If, upon reading, all bits are equal, the data output pin indicates a "1". If any of the bits differ, the data output pin indicates a "0". In Test Mode the 4M DRAM can be tested as if it were a 512K DRAM. Test Mode is exited by any refresh operation which is not a $\overline{WE}$, $\overline{CAS}$- before-$\overline{RAS}$ cycle. Addresses A10R, A10C and A0C do not care during Test Mode.

SIEMENS

1M x 4-Bit Dynamic RAM
Low Power 1M x 4-Bit Dynamic RAM

HYB 514400BJ/BT -50/-60/-70
HYB 514400BJL/BTL -50/-60/-70

Advanced Information

- 1 048 576 words by 4-bit organization
- 0 to 70 °C operating temperature
- Fast access and cycle time
  $\overline{RAS}$ access time:
  50 ns (-50 version)
  60 ns (-60 version)
  70 ns (-70 version)
  CAS access time:
  15 ns (-50,-60 version)
  20 ns (-70 version)
  Cycle time:
  95 ns (-50 version)
  110 ns (-60 version)
  130 ns (-70 version)
- Fast page mode cycle time
  35 ns (-50 version)
  40 ns (-60 version)
  45 ns (-70 version)
- Single + 5 V (± 10 %) supply with a built-in V_{bb} generator
- Low power dissipation
  max. 660 mW active (-50 version)
  max. 605 mW active (-60 version)
  max. 550 mW active (-70 version)
- Standby power dissipation:
  11 mW max. standby (TTL)
  5.5 mW max. standby (CMOS)
  1.1 mW max. standby (CMOS) for Low Power Version
- Output unlatched at cycle end allows two-dimensional chip selection
- Read, write, read-modify write, CAS-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, hidden refresh, fast page mode capability and test mode capability
- All inputs and outputs TTL-compatible
- 1024 refresh cycles / 16 ms
- 1024 refresh cycles / 128 ms Low Power Version only
- Plastic Packages: P-SOJ-26/20-5 and P-TSOPII-26/20-1 with 300 mil width

Ordering Information

Type	Ordering Code	Package	Descriptions
HYB 514400BJ-50	Q67100-Q973	P-SOJ-26/20-5	DRAM (access time 50 ns)
HYB 514400BJ-60	Q67100-Q756	P-SOJ-26/20-5	DRAM (access time 60 ns)
HYB 514400BJ-70	Q67100-Q757	P-SOJ-26/20-5	DRAM (access time 70 ns)
HYB 514400BJL-50	Q67100-Q2012	P-SOJ-26/20-5	Low Power DRAM (access time 50 ns)
HYB 514400BJL-60	Q67100-Q1030	P-SOJ-26/20-5	Low Power DRAM (access time 60 ns)
HYB 514400BJL-70	Q67100-Q762	P-SOJ-26/20-5	Low Power DRAM (access time 70 ns)
HYB 514400BT-50	Q67100-Q2013	P-TSOPII-26/20-1	DRAM (access time 50 ns)
HYB 514400BT-60	Q67100-Q749	P-TSOPII-26/20-1	DRAM (access time 60 ns)
HYB 514400BT-70	Q67100-Q750	P-TSOPII-26/20-1	DRAM (access time 70 ns)
HYB 514400BTL-50	on request	P-TSOPII-26/20-1	Low Power DRAM (access time 80 ns)
HYB 514400BTL-60	on request	P-TSOPII-26/20-1	Low Power DRAM (access time 60 ns)
HYB 514400BTL-70	on request	P-TSOPII-26/20-1	Low Power DRAM (access time 70 ns)

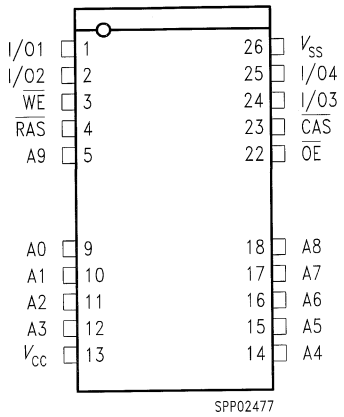
The HYB 514400BJ/BJL/BT/BTL is the new generation dynamic RAM organized as 1 048 576 words by 4-bit. The HYB 514400BJ/BJL/BT/BTL utilizes CMOS silicon gate process as well as advances circuit techniques to provide wide operation margins, both internally and for the system user. Multiplexed address inputs permit the HYB 514400BJ/BJL/BT/BTL to be packed in a standard plastic P-SOPJ-26/20 or P-TSOPII-26/20 package. This package size provides high system bit densities and is compatible with commonly used automatic testing and insertion equipment. System oriented feature include single + 5 V (± 10 %) power supply, direct interfacing with high performance logic device families such as Schottky TTL

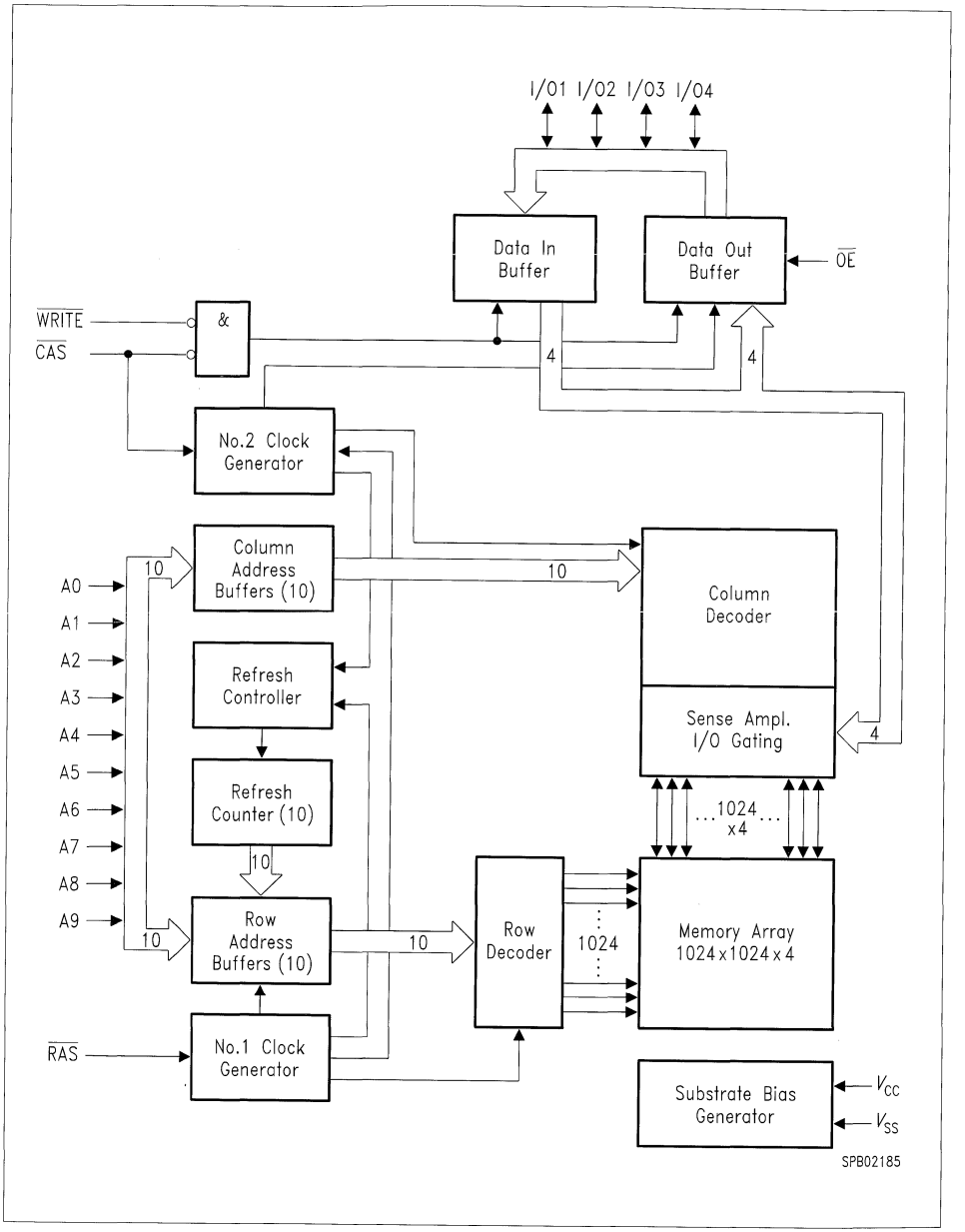
Pin Definitions and Functions

Pin No.	Function
A0-A9	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1 - I/O4	Data Input/Output
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground (0 V)
N.C.	No Connection

Pin Configuration
(top view)

P-SOJ-26/20-5
P-TSOPII-26/20-1





Block Diagram

Absolute Maximum Ratings

Operating temperature range ..... 0 to 70 °C
Storage temperature range ..... – 55 to + 150 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 1 to + 7 V
Power Supply voltage ..... – 1 to + 7 V
Data out current (short circuit) ..... 50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{ih}	2.4	6.5	V	1)
Input low voltage	V_{il}	– 1.0	0.8	V	1)
Output high voltage (I_{OUT} = – 5 mA)	V_{oh}	2.4	–	V	1)
Output low voltage (I_{OUT} = 4.2 mA)	V_{ol}	–	0.4	V	1)
Input leakage current, any input (0 V < V_{in} < 7, all other input = 0 V)	$I_{I(L)}$	– 10	10	µA	1)
Output leakage current (DO is disabled, 0 < V_{OUT} < V_{CC})	$I_{O(L)}$	– 10	10	µA	1)
Average V_{CC} supply current	I_{CC1}			mA	2) 3)
-50 version		–	120		
-60 version		–	110		
-70 version		–	100		
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = $\overline{WE}$ = V_{ih})	I_{CC2}	–	2	mA	–
Average V_{CC} supply current during $\overline{RAS}$-only refresh cycles	I_{CC3}			mA	2)
-50 version		–	120		
-60 version		–	110		
-70 version		–	100		
Average V_{CC} supply current during fast page mode operation	I_{CC4}			mA	2) 3)
-50 version		–	80		
-60 version		–	70		
-70 version		–	60		

DC Characteristics (cont'd)

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = $\overline{WE}$ = V_{CC} – 0.2 V)	I_{CC5}	–	1	mA	1)
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = $\overline{WE}$ = V_{CC} – 0.2 V) for Low Power Version	I_{CC5}	–	200	µA	–
Average V_{CC} supply current during $\overline{CAS}$ before $\overline{RAS}$ refresh mode	I_{CC6}			mA	2)
-50 version		–	120		
-60 version		–	110		
-70 version		–	100		
For Low Power Version only: Battery backup current (average power supply current in battery backup mode): ($\overline{CAS}$ = $\overline{CAS}$ before $\overline{RAS}$ cycling or 0.2 V, $\overline{WE}$ = V_{CC} – 0.2 V or 0.2 V, A0 to A10 = V_{CC} – 0.2 V or 0.2 V; DI = V_{CC} – 0.2 V or 0.2 V or open, t_{RC} = 125 µs, t_{RAS} = t_{RAS} min = 1 µs)	I_{CC7}	–	300	µA	–

AC Characteristics [4)13)]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		-50		-60		-70		
		min.	max.	min.	max.	min.	max.	
Random read or write time	t_{RC}	95	–	110	–	130	–	ns
Read-write cycle time	t_{RWC}	140	–	160	–	185	–	ns
Fast page mode cycle time	t_{PC}	35	–	40	–	45	–	ns
Fast page mode read/write cycle time	t_{PRWC}	80	–	90	–	100	–	ns
Access time from $\overline{RAS}$ [6) 11)]	t_{RAC}	–	50	–	60	–	70	ns
Access time from $\overline{CAS}$ [6) 11)]	t_{CAC}	–	15	–	15	–	20	ns
Access time from column address [6) 12)]	t_{AA}	–	25	–	30	–	35	ns
Access time from CAS precharge [6)]	t_{CPA}	–	30	–	35	–	40	ns
CAS to output in low-Z [6)]	t_{CLZ}	0	–	0	–	0	–	ns
Output buffer turn-off delay from CAS [7)]	t_{OFF}	0	15	0	20	0	20	ns
Transition time (rise and fall) [5)]	t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	35	–	40	–	50	–	ns
$\overline{RAS}$ pulse width	t_{RAS}	50	10000	60	10000	70	10000	ns
$\overline{RAS}$ pulse width in fast page mode	t_{RASP}	50	200000	60	200000	70	200000	ns
$\overline{RAS}$ hold time	t_{RSH}	15	–	15	–	20	–	ns
$\overline{CAS}$ hold time	t_{CSH}	50	–	60	–	70	–	ns
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge (Fast page mode)	t_{RHCP}	30	–	35	–	45	–	ns
$\overline{CAS}$ precharge to $\overline{WE}$ delay time (FPM read-modify-write)	t_{CPWD}	55	–	60	–	65	–	ns
$\overline{CAS}$ pulse width	t_{CAS}	15	10000	15	10000	20	10000	ns

AC Characteristics (cont'd)[4)13)]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		-50		-60		-70		
		min.	max.	min.	max.	min.	max.	
$\overline{RAS}$ to $\overline{CAS}$ delay time [11)]	t_{RCD}	20	35	20	45	20	50	ns
$\overline{RAS}$ to column address delay time [12)]	t_{RAD}	15	25	15	30	15	35	ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	5	–	ns
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns
Row address hold time	t_{RAH}	10	–	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns
Column address hold time	t_{CAH}	10	–	15	–	15	–	ns
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	–	30	–	35	–	ns
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns
Read command hold time [8)]	t_{RCH}	0	–	0	–	0	–	ns
Read command hold time ref. to $\overline{RAS}$ [8)]	t_{RRH}	0	–	0	–	0	–	ns
Write command hold time	t_{WCH}	10	–	10	–	15	–	ns
Write command pulse width	t_{WP}	10	–	10	–	15	–	ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	–	15	–	20	–	ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	–	15	–	20	–	ns
Data setup time [9)]	t_{DS}	0	–	0	–	0	–	ns
Data hold time [9)]	t_{DH}	10	–	15	–	15	–	ns

AC Characteristics (cont'd)[4)13)]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		-50		-60		-70		
		min.	max.	min.	max.	min.	max.	
Refresh period	t_{REF}	–	16	–	16	–	16	ms
Refresh period Low Power Version	t_{REF}	–	128	–	128	–	128	ms
Write command setup time [10)]	t_{WCS}	0	–	0	–	0	–	ns
$\overline{CAS}$ to $\overline{WE}$ delay time [10)]	t_{CWD}	40	–	45	–	50	–	ns
$\overline{RAS}$ to $\overline{WE}$ delay time [10)]	t_{RWD}	75	–	90	–	100	–	ns
Column address to $\overline{WE}$ delay time [10)]	t_{AWD}	50	–	60	–	65	–	ns
$\overline{CAS}$ setup time (CBR cycle)	t_{CSR}	5	–	5	–	5	–	ns
$\overline{CAS}$ hold time (CBR cycle)	t_{CHR}	10	–	15	–	15	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	0	–	0	–	0	–	ns
$\overline{CAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$ counter test cycle)	t_{CPT}	25	–	30	–	40	–	ns
Write command setup time (test mode entry)	t_{WTS}	10	–	10	–	10	–	ns
Write command hold time (in test mode entry cycle)	t_{WTH}	10	–	10	–	10	–	ns
Write to $\overline{RAS}$ precharge time (CBS cycle)	t_{WRP}	10	–	10	–	10	–	ns
Write to $\overline{RAS}$ hold time (CBR cycle)	t_{WRH}	10	–	10	–	10	–	ns
OE command hold time	t_{OEH}	15	–	20	–	20	–	ns
OE acces time	t_{OEA}	–	15	–	15	–	20	ns

AC Characteristics (cont'd)[4)13)]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		-50		-60		-70		
		min.	max.	min.	max.	min.	max.	
$\overline{RAS}$ hold time referenced to OE	t_{ROH}	10	–	10	–	10	–	ns
Output buffer turn-off delay from OE	t_{OEZ}	0	15	0	20	0	20	ns
Data to $\overline{CAS}$ low delay [14)]	t_{DZC}	0	–	0	–	0	–	ns
Data to OE low delay [14)]	t_{DZO}	0	–	0	–	0	–	ns
$\overline{CAS}$ high to data delay [15)]	t_{CDD}	15	–	20	–	20	–	ns
OE high to data delay [15)]	t_{ODD}	15	–	20	–	20	–	ns

Capacitance

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A9)	C_{i1}	–	5	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$,$\overline{OE}$)	C_{i2}	–	7	pF
Output capacitance (IO1 to IO4)	C_{io}	–	7	pF

Notes:

1) All voltages are referenced to V_{SS}

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1}, I_{CC4} depend on output loading.

4) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using the internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

5) V_{ih} (min.) and V_{il} (max.) are reference levels for measuring timing of input signals. Transition times are also measured between V_{ih} and V_{il}.

6) Measured with a load equivalent to 2 TTL loads and 100 pF.

7) t_{off} (max.), t_{OEZ} (max.) defines the time at which the output achieves the open-circuit conditions and are not referenced to output voltage levels.

8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9) These parameters are references to the $\overline{CAS}$ leading edge in early write and to the $\overline{WE}$ leading edge in read-write cycles.

10) t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only.
If $t_{WCS} > t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} > t_{RWD}$ (min.), $t_{CWD} > t_{CWD}$ (min.) and $t_{AWD} > t_{AWD}$ (min.), the cycle is a read-write cycle and I/O will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of I/O (at access time) is indeterminate.

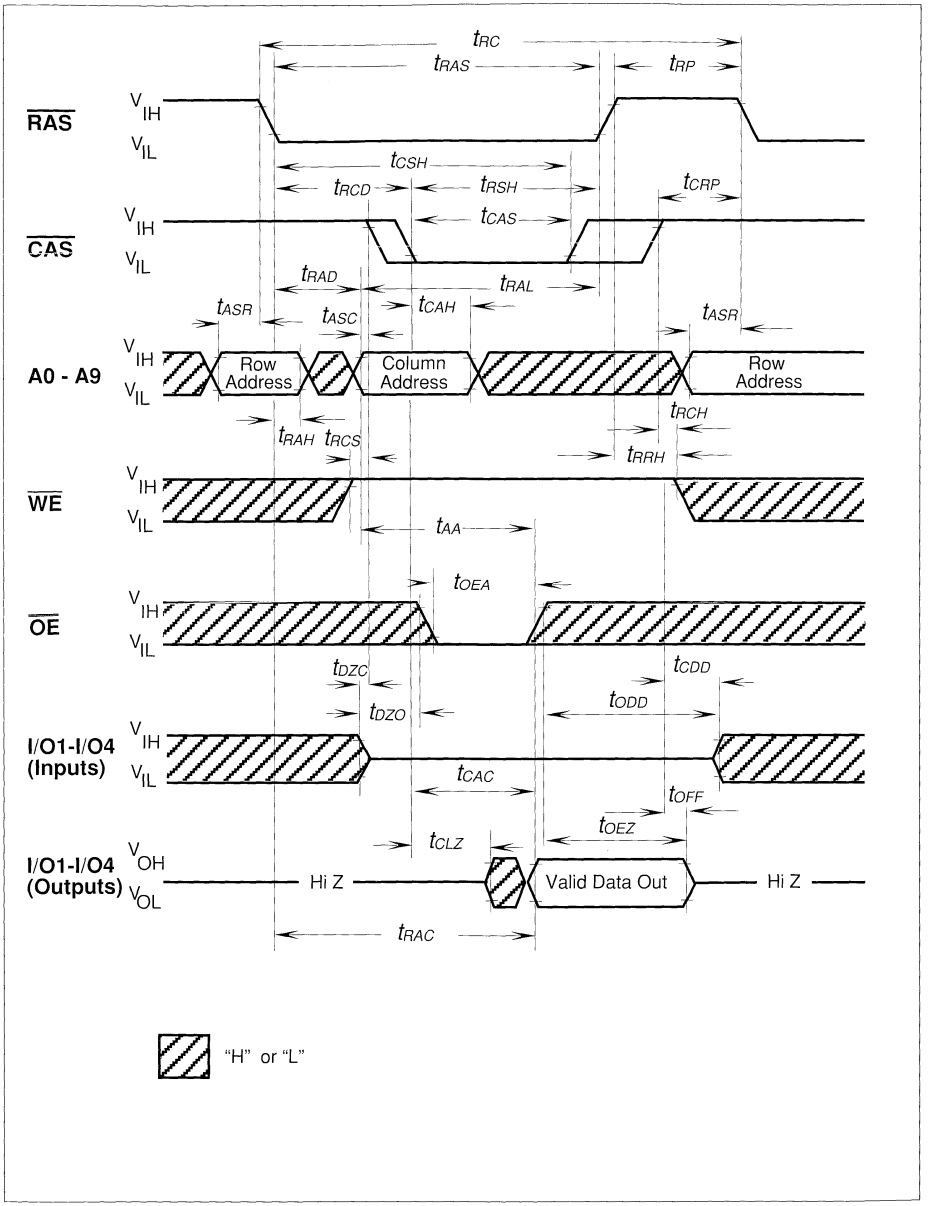
11) Operation within the t_{RCD} (max.) limit ensure that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

12) Operation within the t_{RAD} (max.) limit ensured that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

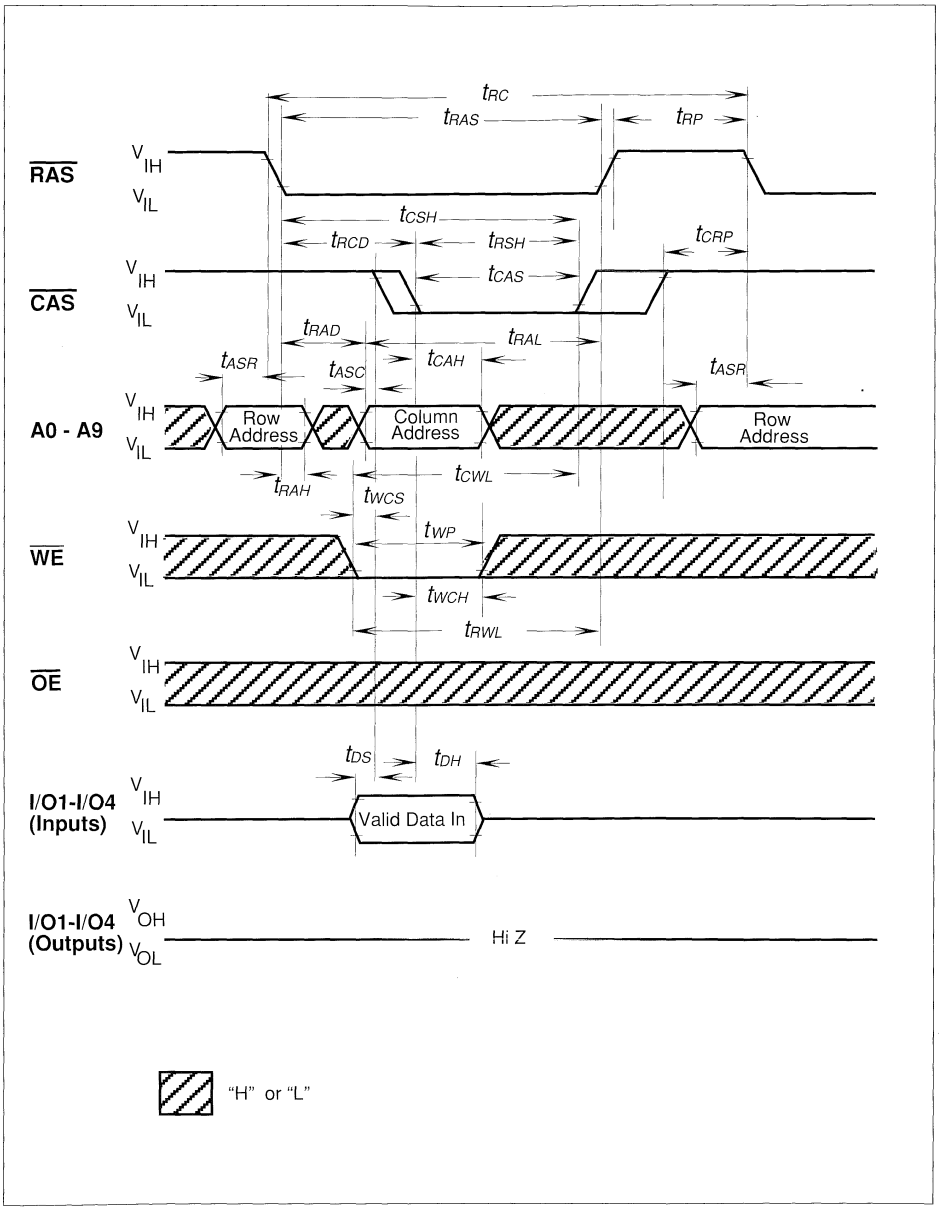
13) AC measurements assume t_T = 5 ns

14) Either t_{DZC} or t_{DZO} must be satisfied.

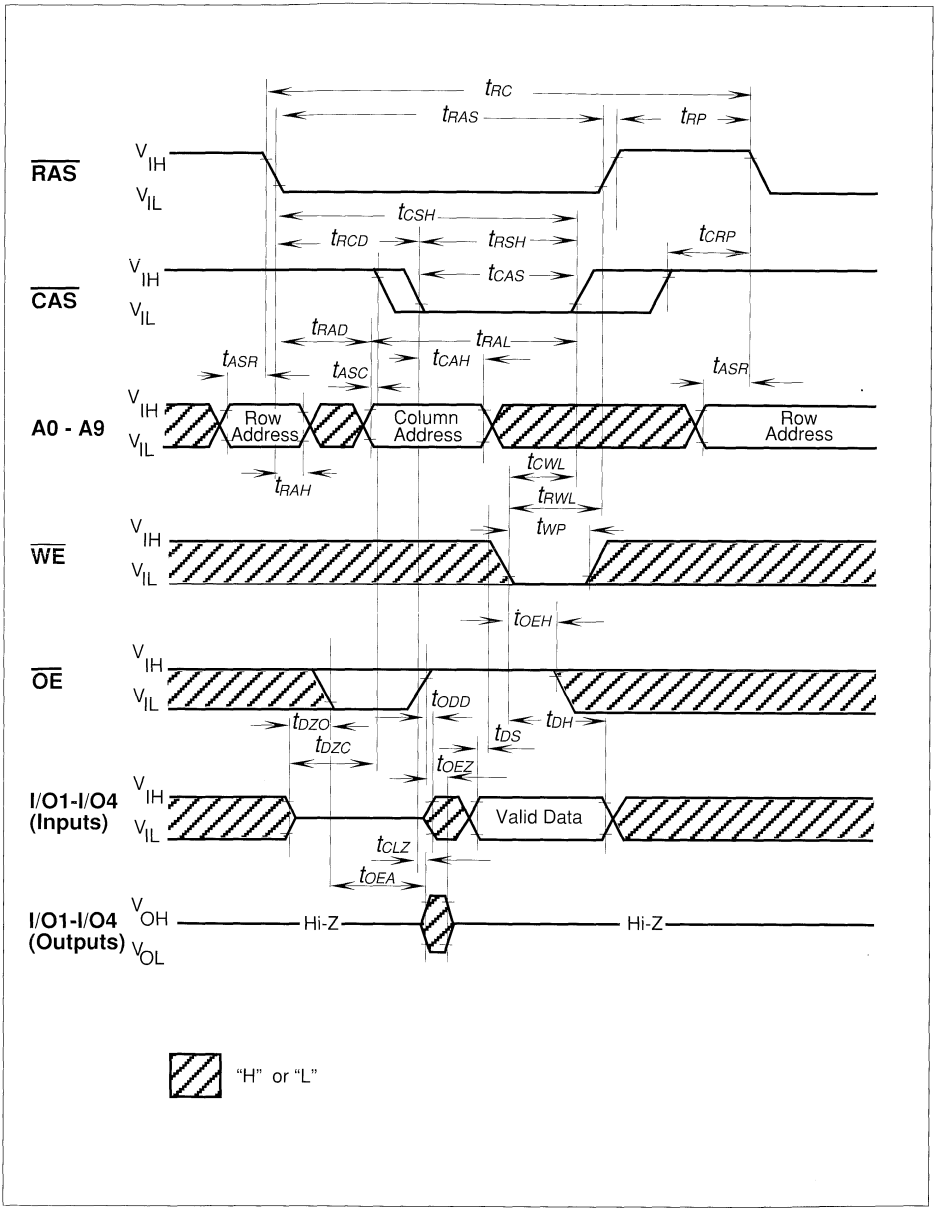
15) Either t_{CDD} or t_{ODD} must be satisfied.


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tASR
tASC
tCAH
A0 - A9
Row Address
Column Address
Row Address
tRCH
tRAH
tRCS
tRRH
WE
tAA
tOEA
OE
tDZC
tCDD
tDZO
tODD
I/O1-I/O4 (Inputs)
tCAC
tOFF
tOEZ
tCLZ
I/O1-I/O4 (Outputs)
VOH
VOL
Hi Z
Valid Data Out
Hi Z
tRAC
"H" or "L"

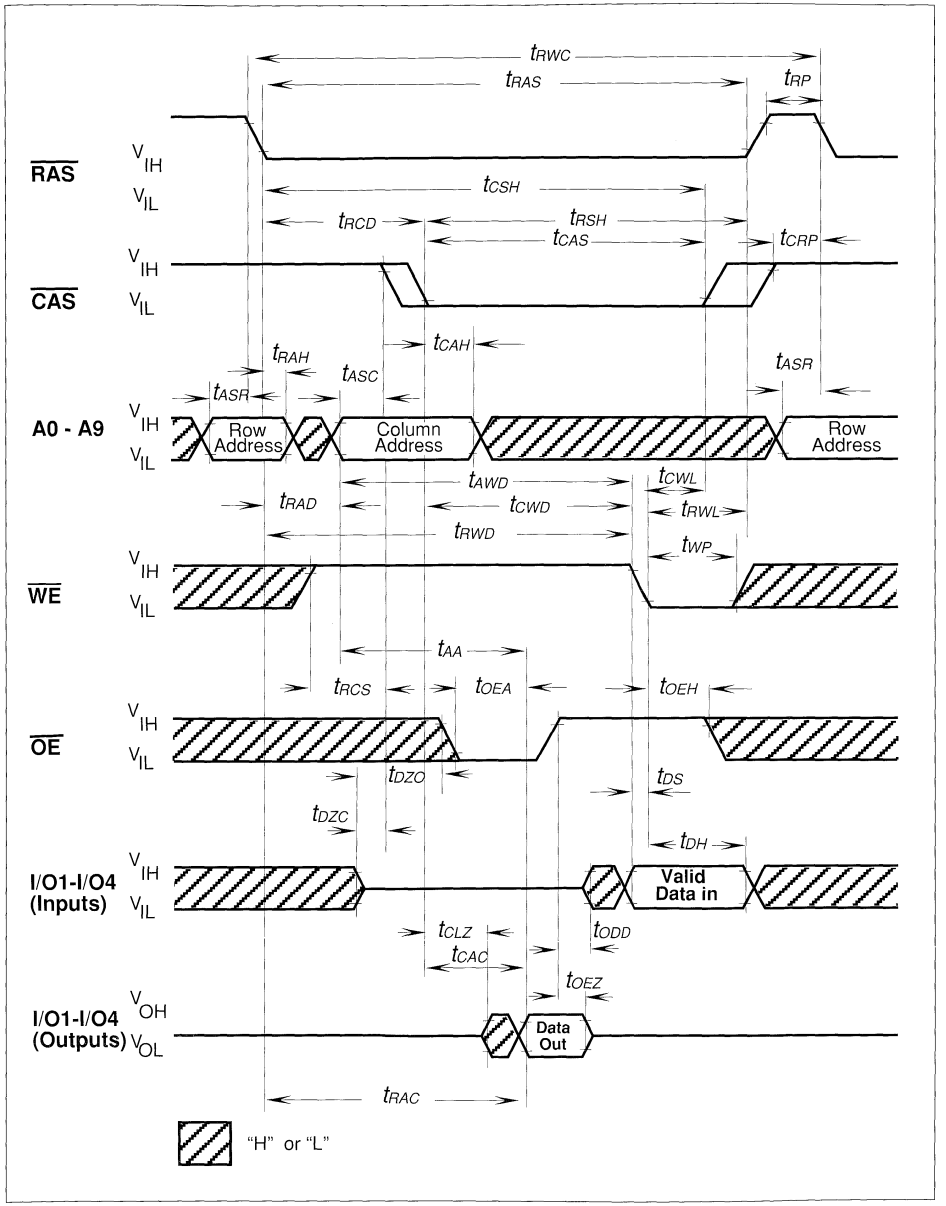
Read Cycle



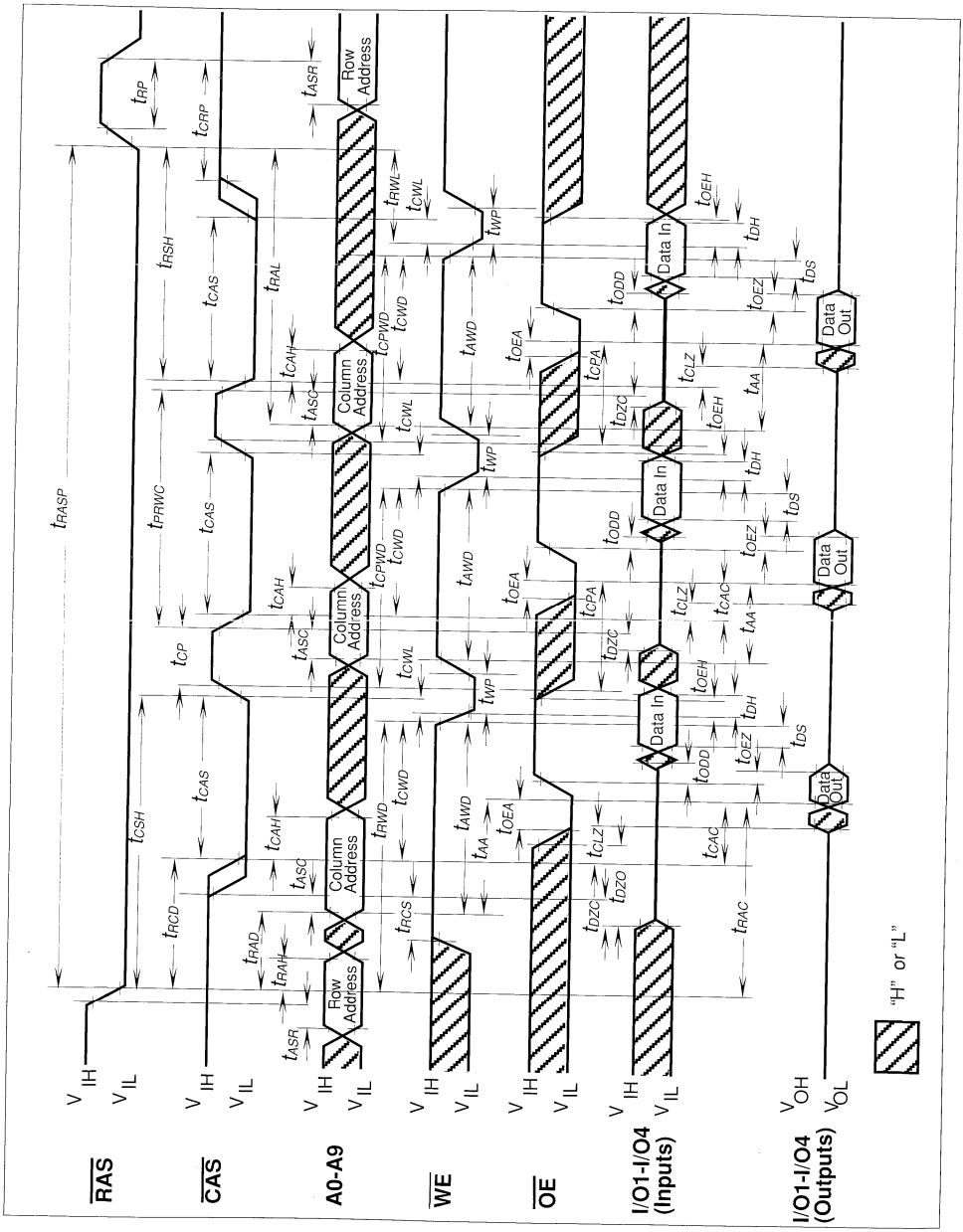
Write Cycle (Early Write)



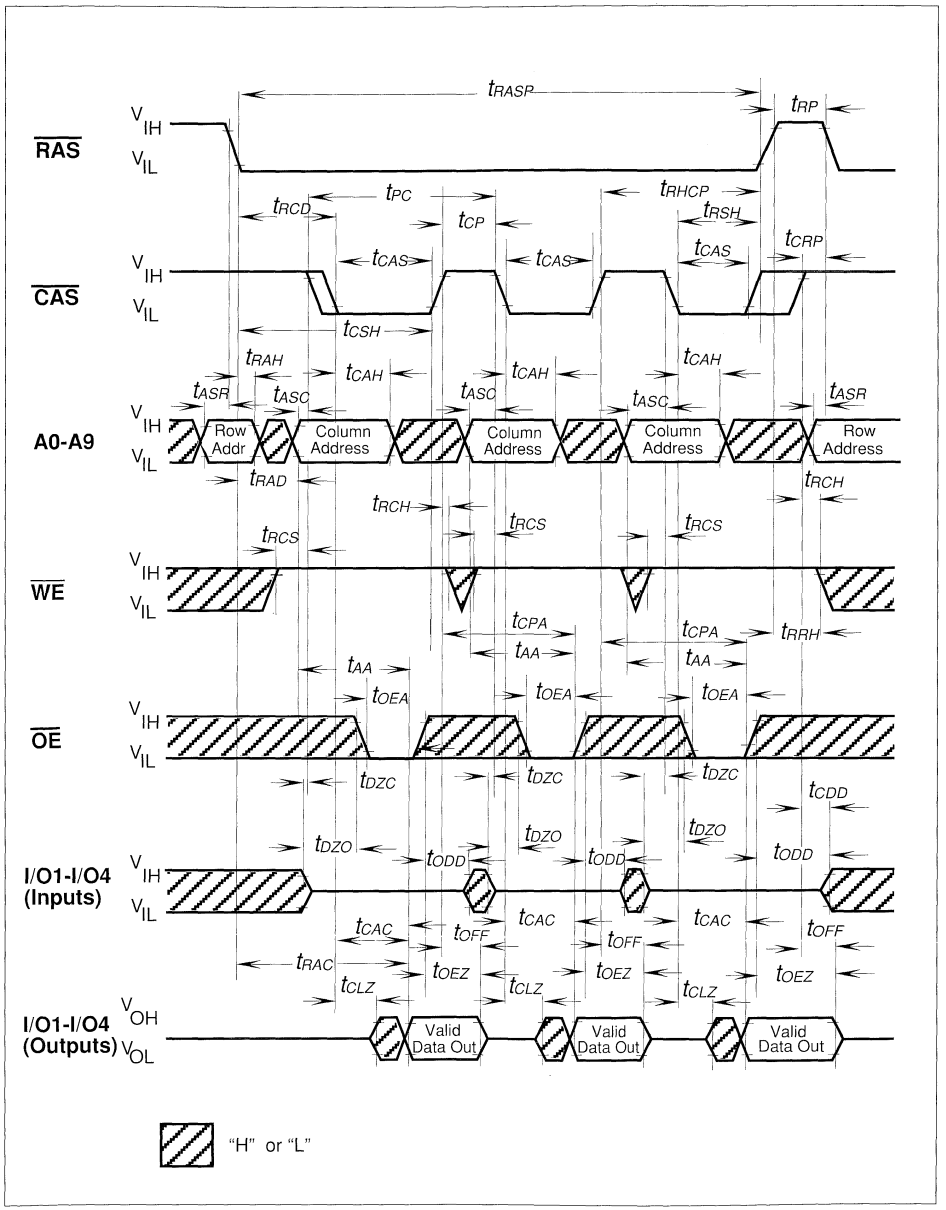
Write Cycle ($\overline{OE}$ Controlled Write)



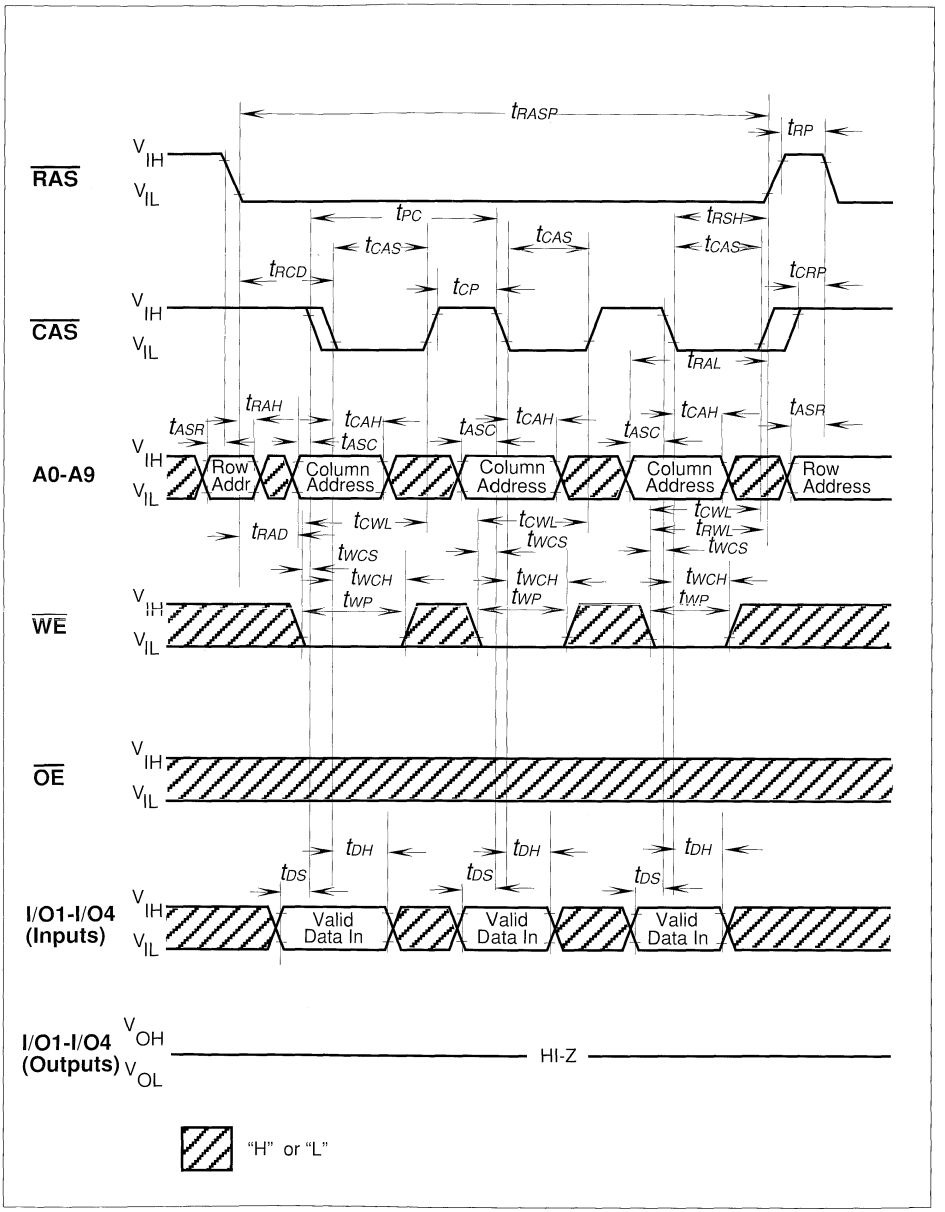
Read-Write (Read-Modify-Write) Cycle



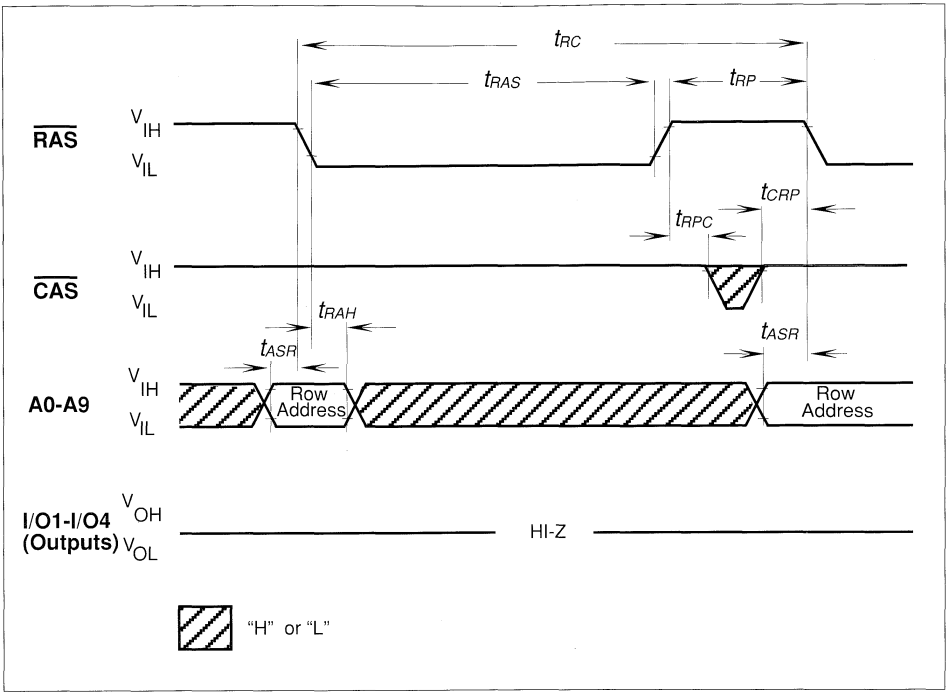
Fast Page Mode Read-Modify-Write Cycle



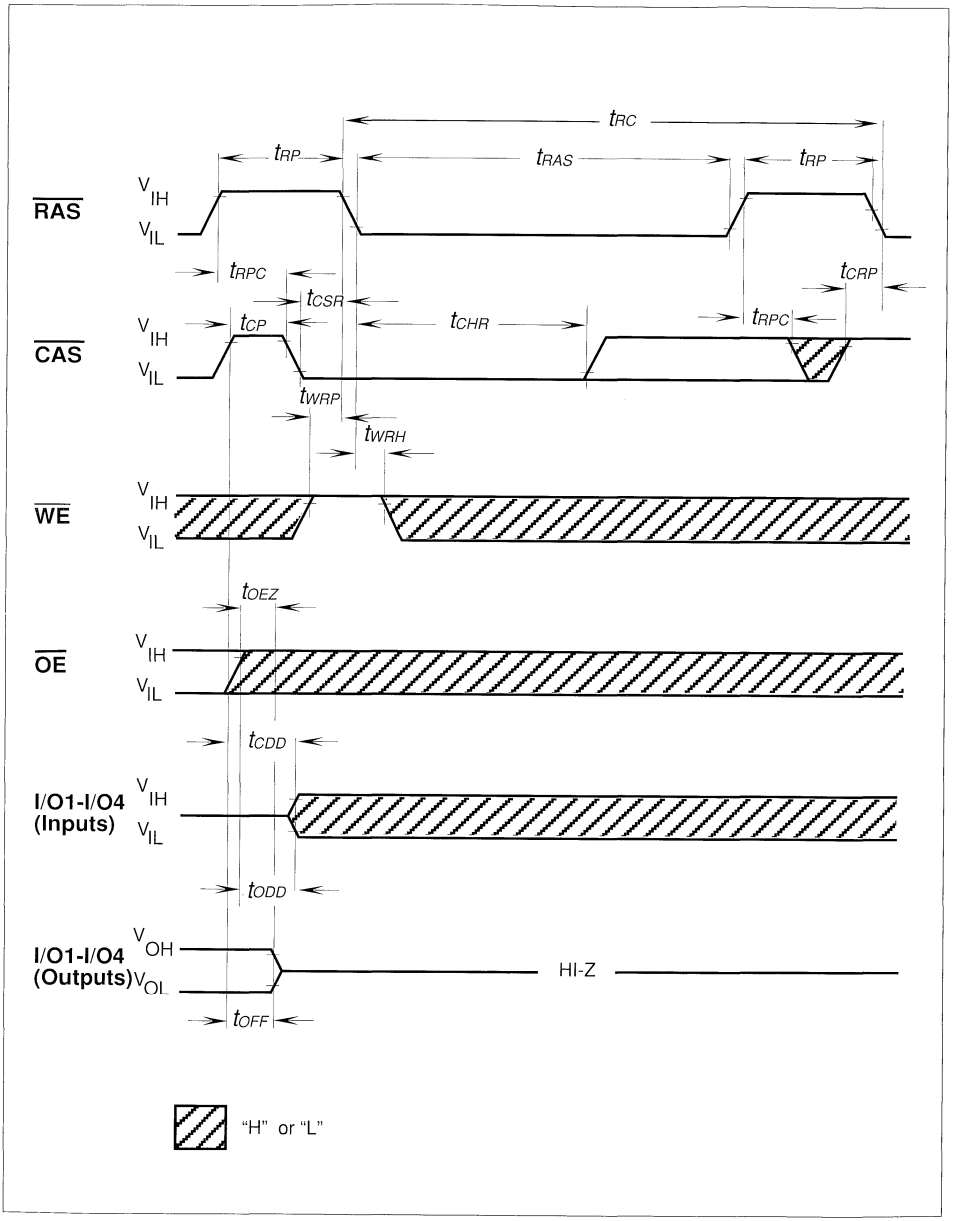
Fast Page Mode Read Cycle



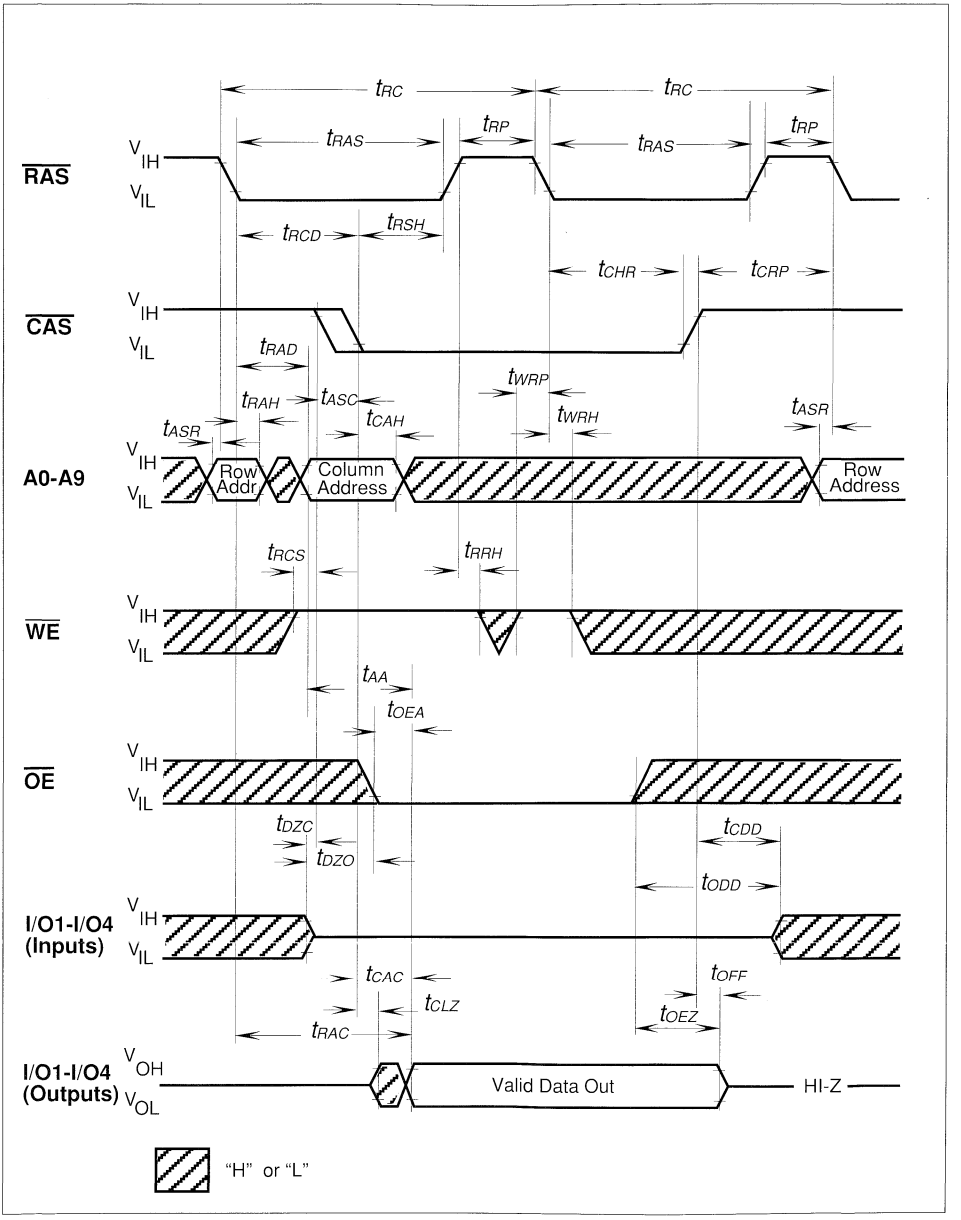
Fast Page Mode Early Write Cycle



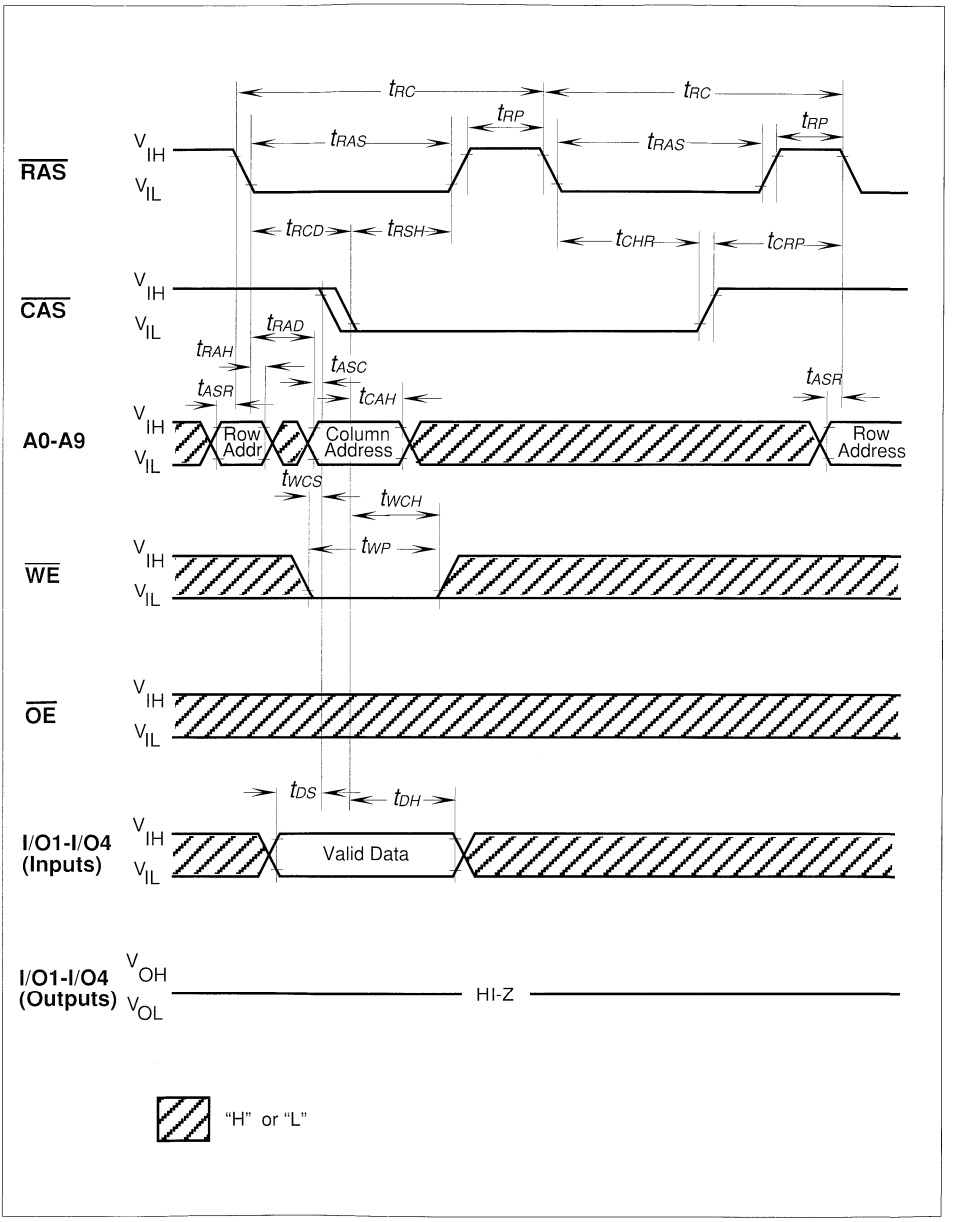
$\overline{RAS}$-Only Refresh Cycle



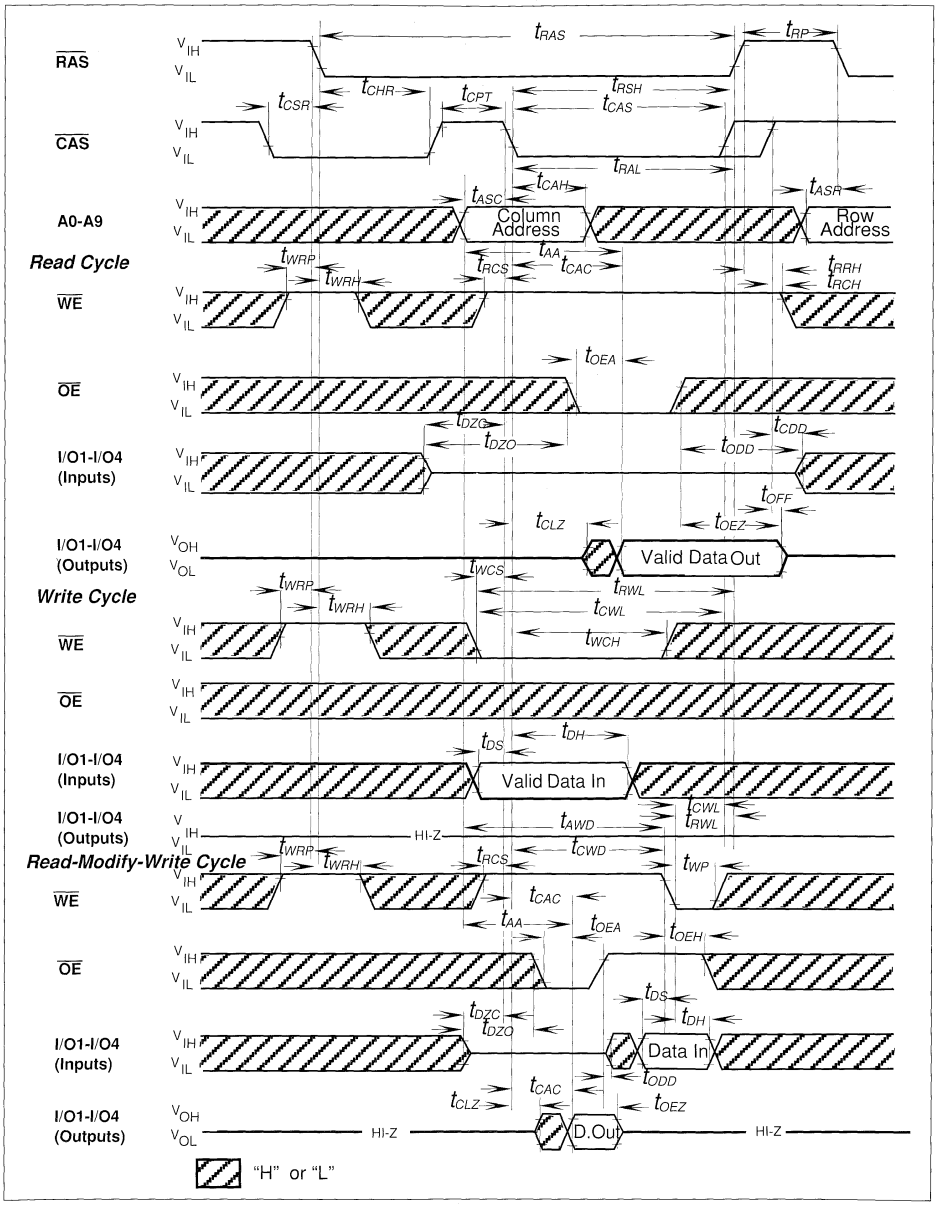
CAS-Before-RAS Refresh Cycle



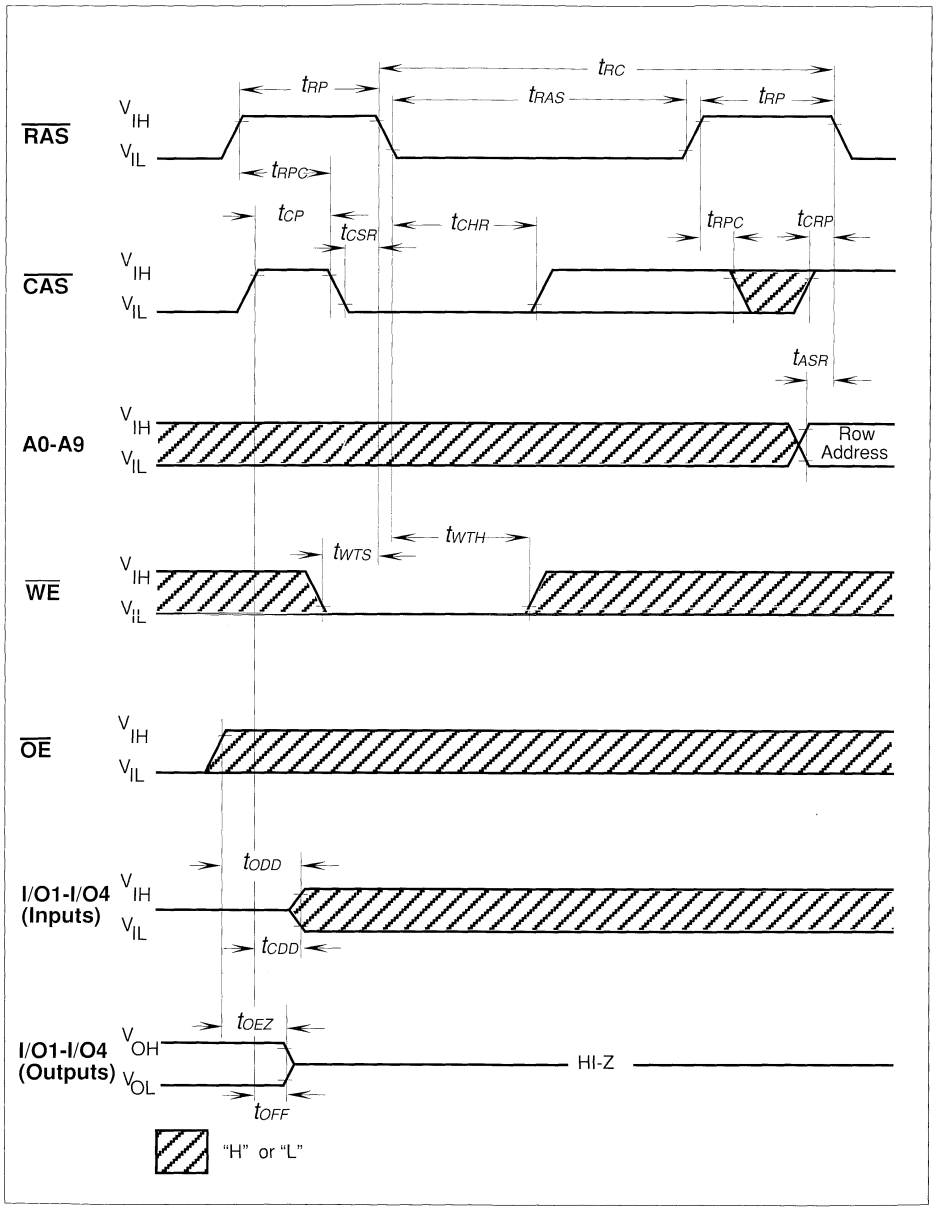
Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Early Write)



CAS-Before-RAS Refresh Counter Test Cycle



Test Mode Entry

Test Mode

As the HYB 514400BJ/BJL/BT/BTL is organized internally as 512K x 8-bits, a test mode cycle using 8:1 compression can be used to improve test time. Note that in the 1M x 4 version the test time is reduced by 1/2 for a linear test pattern.

In a test mode "write" the data from each I/O1 pin is written into eight bits simultaneously (all "1" s or all "0" s).The I/O2-I/O4 inputs are not used for writing in test mode. In test mode "read" each I/O output is used for indicating the test mode result. If the internal eight bits are equal, the I/O would indicate a "1". If they were not equal, the I/O would indicate a "0".Note that in test mode „read" I/O1-I/O3 are always driven to „ones" ,i.e. all outputs will be „1"s for a test mode „pass". The WCBR cycle ($\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$) puts the device into test mode. To exit from test mode, a "$\overline{CAS}$ before $\overline{RAS}$ refresh", "$\overline{RAS}$ only refresh" or "Hidden refresh" can be used.

Addresses A10R, A10C and A0C are don't care during test mode.

512kx8-Bit Dynamic RAM

HYB 514800BJ -60/-70/-80

Advanced Information

- 512 288 words by 8-bit organization
- 0 to 70 °C operating temperature
- Fast access and cycle time
  RAS access time:
  60 ns (-60 version)
  70 ns (-70 version)
  80 ns (-80 version)
  CAS access time:
  20 ns
  Cycle time:
  110 ns (-60 version)
  130 ns (-70 version)
  150 ns (-80 version)
- Fast page mode cycle time
  45 ns (-60 version)
  45 ns (-70 version)
  50 ns (-80 version)
- Single + 5 V (± 10 %) supply with a built-in V_{bb} generator
- Low power dissipation
  max. 605 mW active (-60 version)
  max. 550 mW active (-70 version)
  max. 468 mW active (-80 version)
- Standby power dissipation:
  11 mW standby standby (TTL)
  5.5 mW max.standby (CMOS)
- Output unlatched at cycle end allows two-dimensional chip selection
- Read, write, read-modify write, CAS-before-RAS refresh, RAS-only refresh, hidden refresh, fast page mode capability
- All inputs and outputs TTL-compatible
- 1024 refresh cycles / 16 ms
- Plastic Packages: P-SOJ-28-2 400 mil width

Ordering Information

Type	Ordering Code	Package	Descriptions
HYB 514800BJ-60	Q67100-Q849	P-SOJ-28-2	DRAM (access time 60 ns)
HYB 514800BJ-70	Q67100-Q850	P-SOJ-28-2	DRAM (access time 70 ns)
HYB 514800BJ-80	Q67100-Q851	P-SOJ-28-2	DRAM (access time 80 ns)

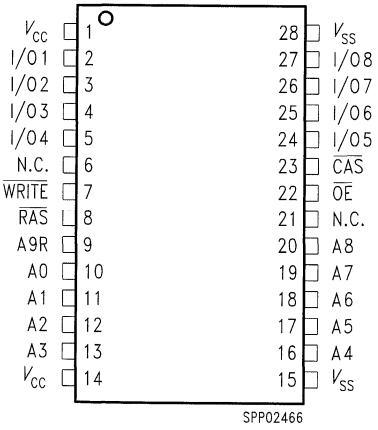
The HYB 514800BJ is the new generation dynamic RAM organized as 512 288 words by 8-bit. The HYB 514800BJ utilizes CMOS silicon gate process as well as advances circuit techniques to provide wide operation margins, both internally and for the system user. Multiplexed address inputs permit the HYB 514800BJ to be packed in a standard plastic 400mil wide P-SOPJ-28 package. This package size provides high system bit densities and is compatible with commonly used automatic testing and insertion equipment. System oriented feature include single + 5 V (± 10 %) power supply, direct interfacing with high performance logic device families such as Schottky TTL.

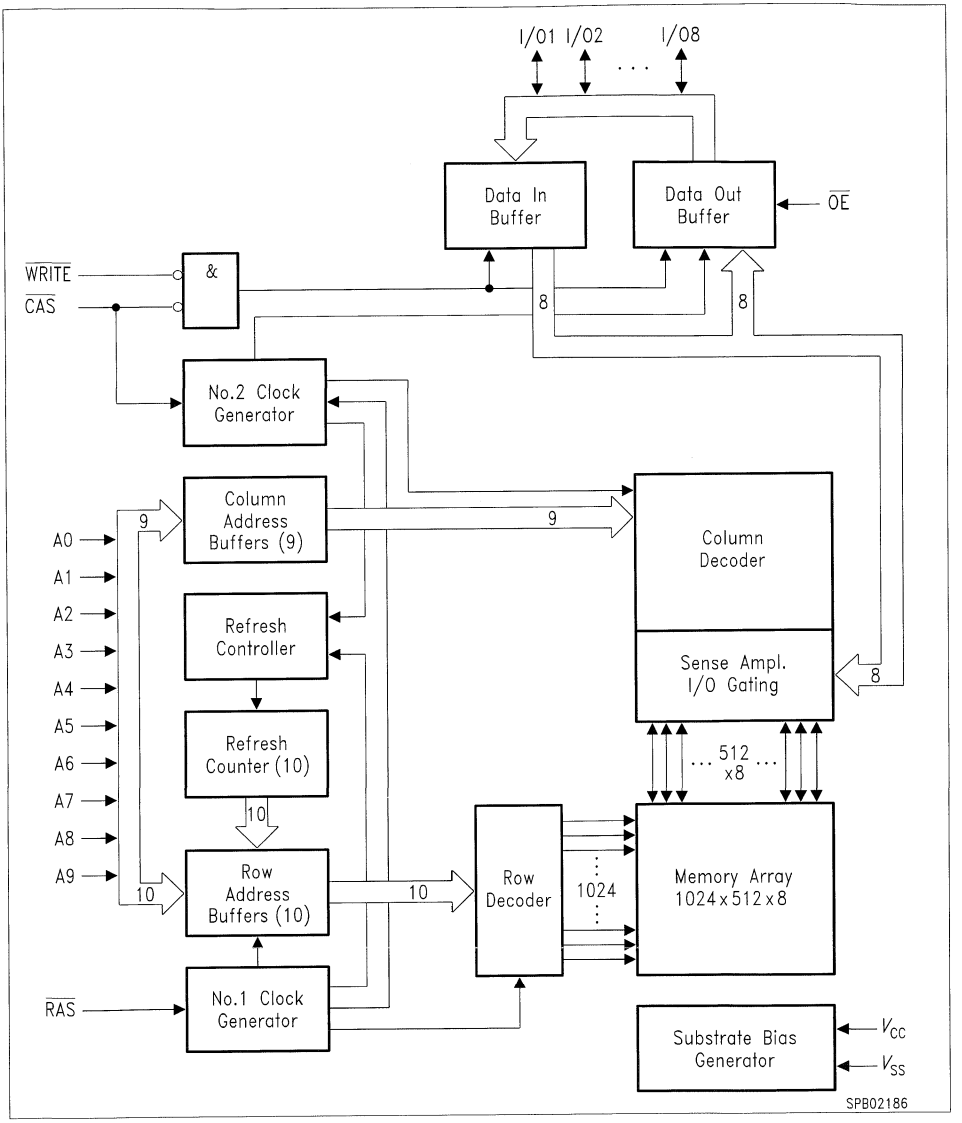
Pin Definitions and Functions

A0-A8,A9R	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
IO1 - IO8	Data Input/Output
N.C.	No Connection
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground (0 V)

Pin Configuration
(top view)

P-SOJ-28-2 (400 mil width)





Block Diagram

Absolute Maximum Ratings

Operating temperature range ..... 0 to 70 °C
Storage temperature range ..... – 55 to + 150 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 1 to + 7 V
Power Supply voltage ..... – 1 to + 7 V
Data out current (short circuit) ..... 50 mA

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC Characteristics

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{ih}	2.4	6.5	V	1)
Input low voltage	V_{il}	– 1.0	0.8	V	1)
Output high voltage (I_{OUT} = – 5 mA)	V_{oh}	2.4	–	V	1)
Output low voltage (I_{OUT} = 4.2 mA)	V_{ol}	–	0.4	V	1)
Input leakage current, any input (0 V < V_{in} < 7, all other input = 0 V)	$I_{I(L)}$	– 10	10	µA	1)
Output leakage current (DO is disabled, 0 < V_{OUT} < V_{CC})	$I_{O(L)}$	– 10	10	µA	1)
Average V_{CC} supply current	I_{CC1}			mA	2) 3)
-60 version		–	110		
-70 version		–	100		
-80 version		–	90		
Standby V_{CC} supply current (RAS = CAS = V_{ih})	I_{CC2}	–	2	mA	–
Average V_{CC} supply current during RAS-only refresh cycles	I_{CC3}			mA	2)
-60 version		–	110		
-70 version		–	100		
-80 version		–	90		
Average V_{CC} supply current during fast page mode operation	I_{CC4}			mA	2) 3)
-60 version		–	70		
-70 version		–	60		
-80 version		–	50		

DC Characteristics (cont'd)

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Standby V_{CC} supply current (RAS = CAS = V_{CC} – 0.2 V)	I_{CC5}	–	1	mA	1)
Average V_{CC} supply current during CAS before RAS refresh mode	I_{CC6}			mA	2)
-60 version		–	110		
-70 version		–	100		
-80 version		–	90		

AC Characteristics [4]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		-60		-70		-80		
		min.	max.	min.	max.	min.	max.	
Random read or write time	t_{RC}	110	–	130	–	150	–	ns
Read-write cycle time	t_{RWC}	165	–	185	–	205	–	ns
Fast page mode cycle time	t_{PC}	45	–	45	–	50	–	ns
Fast page mode read/write cycle time	t_{PRWC}	100	–	100	–	105	–	ns
Access time from RAS [6) 11)]	t_{RAC}	–	60	–	70	–	80	ns
Access time from CAS [6) 11)]	t_{CAC}	–	20	–	20	–	20	ns
Access time from column address [6) 12)]	t_{AA}	–	30	–	35	–	40	ns
Access time from CAS precharge [6)]	t_{CPA}	–	40	–	40	–	45	ns
CAS to output in low-Z [6)]	t_{CLZ}	0	–	0	–	0	–	ns
Output buffer turn-off delay from CAS [7)]	t_{OFF}	0	20	0	20	0	20	ns
Transition time (rise and fall) [5)]	t_T	3	50	3	50	3	50	ns
RAS precharge time	t_{RP}	40	–	50	–	60	–	ns
RAS pulse width	t_{RAS}	60	10000	70	10000	80	10000	ns
RAS pulse width in fast page mode	t_{RASP}	60	200000	70	200000	80	200000	ns
CAS pulse width	t_{CAS}	20	10000	20	10000	20	10000	ns
RAS hold time	t_{RSH}	20	–	20	–	20	–	ns
CAS hold time	t_{CSH}	60	–	70	–	80	–	ns
RAS hold time from CAS precharge (Fast page mode)	t_{RHCP}	40	–	45	–	50	–	ns
CAS precharge to WRITE delay time (FPM read-modify-write)	t_{CPWD}	60	–	65	–	70	–	ns

AC Characteristics (cont'd)[4]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		-60		-70		-80		
		min.	max.	min.	max.	min.	max.	
RAS to CAS delay time [11]	t_{RCD}	20	40	20	50	20	60	ns
RAS to column address delay time [12]	t_{RAD}	15	30	15	35	15	40	ns
CAS to RAS precharge time	t_{CRP}	5	–	5	–	10	–	ns
CAS precharge time	t_{CP}	10	–	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns
Row address hold time	t_{RAH}	10	–	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns
Column address hold time	t_{CAH}	15	–	15	–	15	–	ns
Column address to RAS lead time	t_{RAL}	30	–	35	–	40	–	ns
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns
Read command hold time [8]	t_{RCH}	0	–	0	–	0	–	ns
Read command hold time ref. to RAS [8]	t_{RRH}	0	–	0	–	0	–	ns
Write command hold time	t_{WCH}	10	–	15	–	15	–	ns
Write command hold time ref. to RAS	t_{WCR}	50	–	55	–	60	–	ns
Write command pulse width	t_{WP}	10	–	15	–	15	–	ns
Write command to RAS lead time	t_{RWL}	20	–	20	–	20	–	ns
Write command to CAS lead time	t_{CWL}	20	–	20	–	20	–	ns
Data setup time [9]	t_{DS}	0	–	0	–	0	–	ns

AC Characteristics (cont'd)[4]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		-60		-70		-80		
		min.	max.	min.	max.	min.	max.	
Data hold time [9]	t_{DH}	15	–	15	–	15	–	ns
Refresh period	t_{REF}	–	16	–	16	–	16	ms
Write command setup time [10]	t_{WCS}	0	–	0	–	0	–	ns
CAS to WRITE delay time [10]	t_{CWD}	50	–	50	–	50	–	ns
RAS to WRITE delay time [10]	t_{RWD}	90	–	100	–	110	–	ns
Column address to WRITE delay time [10]	t_{AWD}	60	–	65	–	70	–	ns
CAS setup time (CBR cycle)	t_{CSR}	5	–	5	–	5	–	ns
CAS hold time (CBR cycle)	t_{CHR}	15	–	15	–	15	–	ns
RAS to CAS precharge time	t_{RPC}	0	–	0	–	0	–	ns
CAS precharge time (CAS before RAS counter test cycle)	t_{CPT}	30	–	40	–	40	–	ns
Write to RAS precharge time (CBR cycle)	t_{WRP}	10	–	10	–	10	–	ns
Write to RAS hold time (CBR cycle)	t_{WRH}	10	–	10	–	10	–	ns
OE command hold time	t_{OEH}	20	–	20	–	20	–	ns
OE acces time	t_{OEA}	–	20	–	20	–	20	ns
RAS hold time referenced to OE	t_{ROH}	10	–	10	–	10	–	ns
Output buffer turn-off delay from OE	t_{OEZ}	0	20	0	20	0	20	ns
Data to CAS low delay [14]	t_{DZC}	0	–	0	–	0	–	ns

AC Characteristics (cont'd)[4)]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		-60		-70		-80		
		min.	max.	min.	max.	min.	max.	
Data to OE low delay [14)]	t_{DZO}	0	–	0	–	0	–	ns
CAS high to data delay [15)]	t_{CDD}	20	–	20	–	20	–	ns
OE high to data delay [15)]	t_{ODD}	20	–	20	–	20	–	ns
CAS hold time after OE low	t_{OECH}	20	–	20	–	20	–	ns

Capacitance

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A9)	C_{i1}	–	5	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{i2}	–	7	pF
Output capacitance (IO1 to IO8)	C_{io}	–	7	pF

Notes:

1) All voltages are referenced to V_{SS}

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1}, I_{CC4} depend on output loading.

4) An initial pause of 200 µs is required after power-up followed by 8 RAS cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using the internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS cycles are required.

5) V_{ih} (min.) and V_{il} (max.) are reference levels for measuring timing of input signals. Transition times are also measured between V_{ih} and V_{il}.

6) Measured with a load equivalent to 2 TTL loads and 100 pF.

7) t_{off} (max.), t_{OEZ} (max.) defines the time at which the output achieves the open-circuit conditions and are not referenced to output voltage levels.

8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9) These parameters are references to the CAS leading edge in early write and to the WRITE leading edge in read-write cycles.

10) t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only.
If $t_{WCS} > t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} > t_{RWD}$ (min.), $t_{CWD} > t_{CWD}$ (min.) and $t_{AWD} > t_{AWD}$ (min.), the cycle is a read-write cycle and I/O will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of I/O (at access time) is indeterminate.

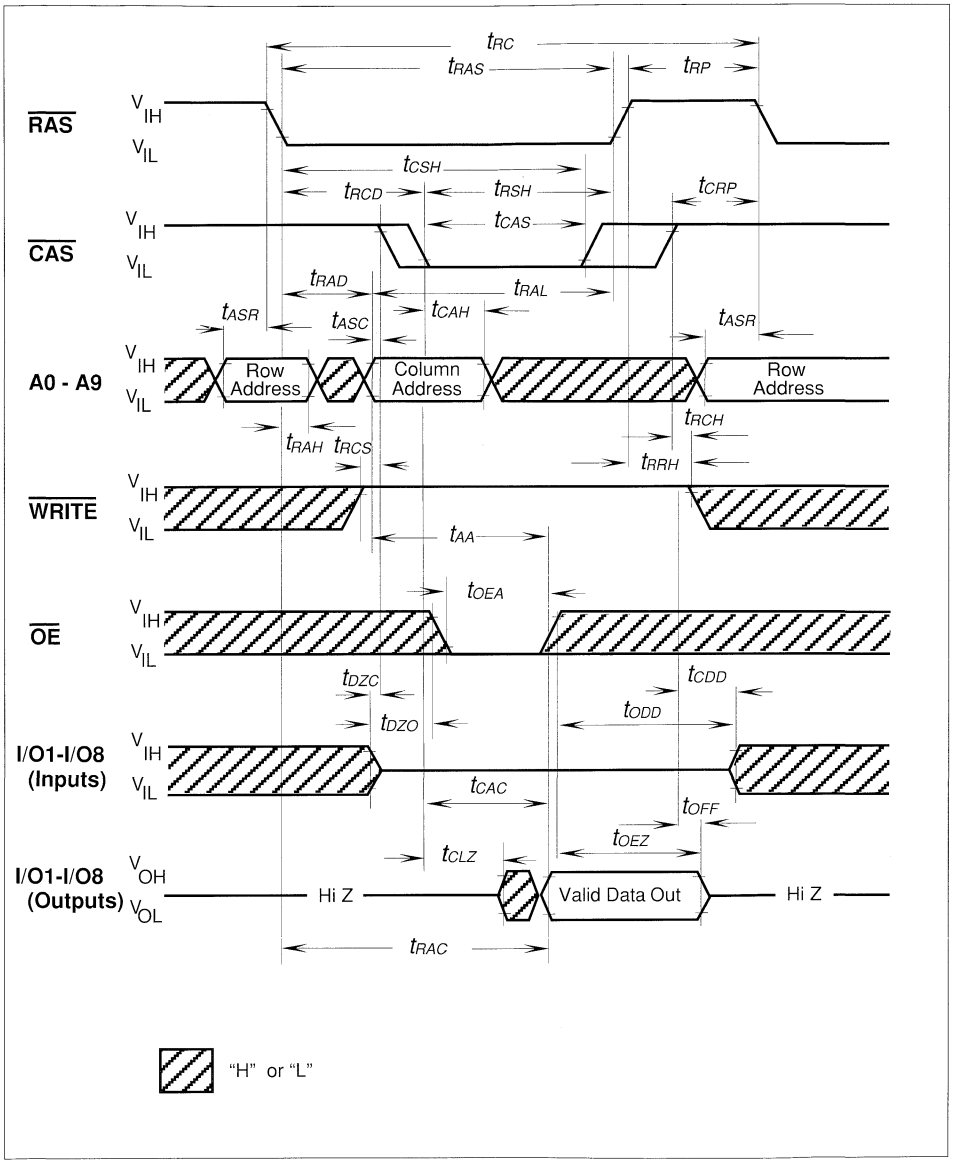
11) Operation within the t_{RCD} (max.) limit ensure that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

12) Operation within the t_{RAD} (max.) limit ensured that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

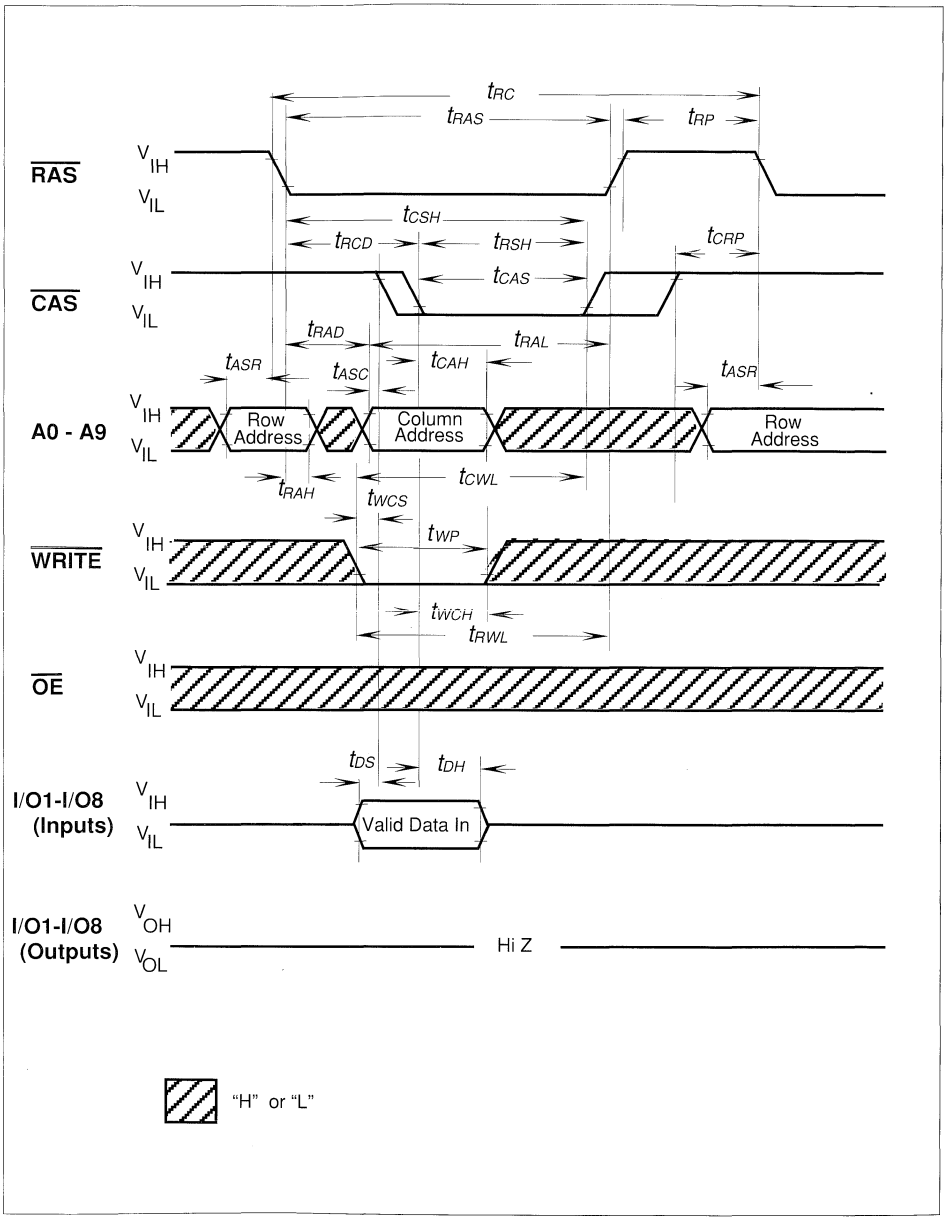
13) AC measurements assume t_T = 5 ns.

14) Either t_{DZC} or t_{DZO} must be satisfied.

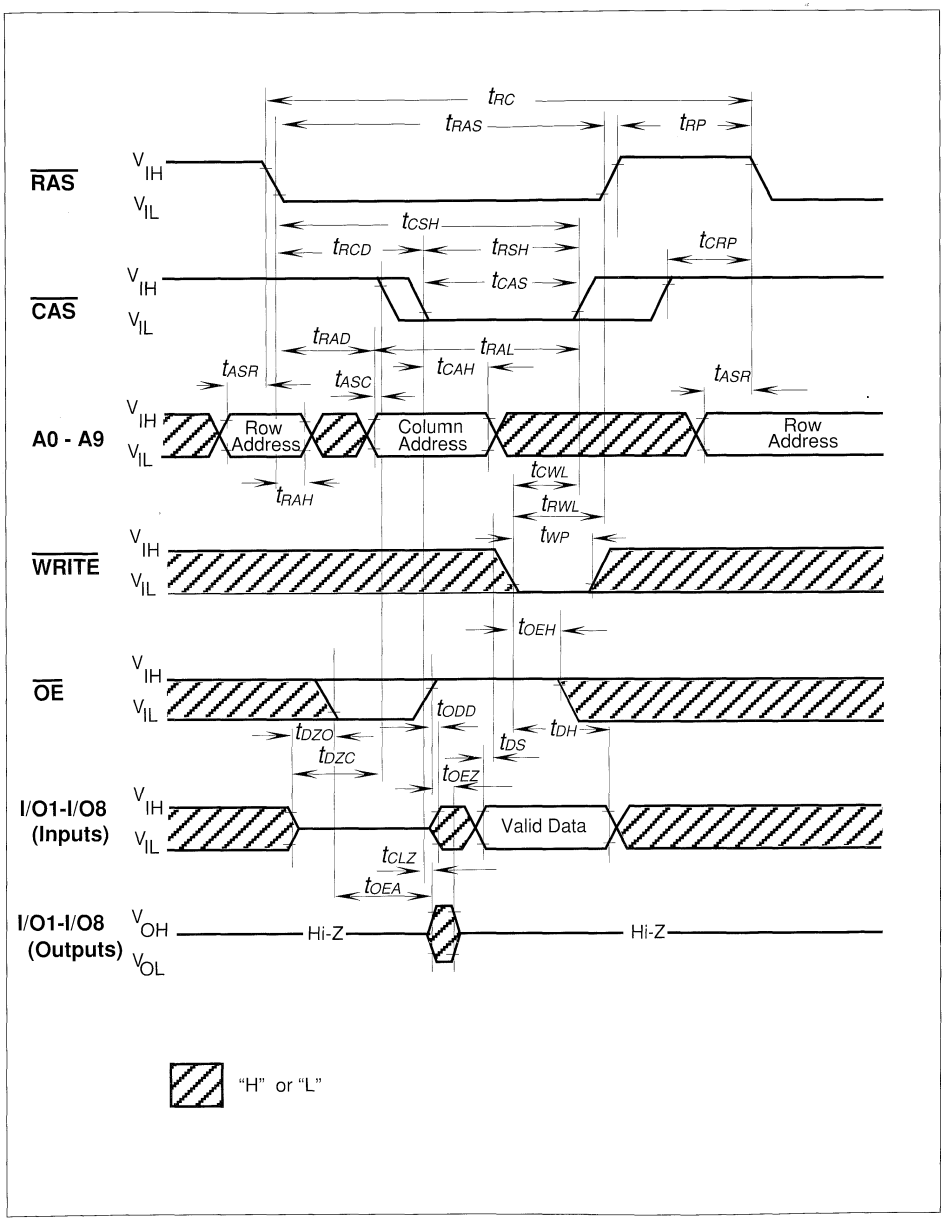
15) Either t_{CDD} or t_{ODD} must be satisfied.


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tASR
tASC
tCAH
tASR
A0 - A9
Row Address
Column Address
Row Address
tRCH
tRAH
tRCS
tRRH
WRITE
tAA
tOEA
OE
tDZC
tCDD
tDZO
tODD
I/O1-I/O8 (Inputs)
tCAC
tOFF
tOEZ
tCLZ
I/O1-I/O8 (Outputs)
VOH
VOL
Hi Z
Valid Data Out
Hi Z
tRAC
"H" or "L"

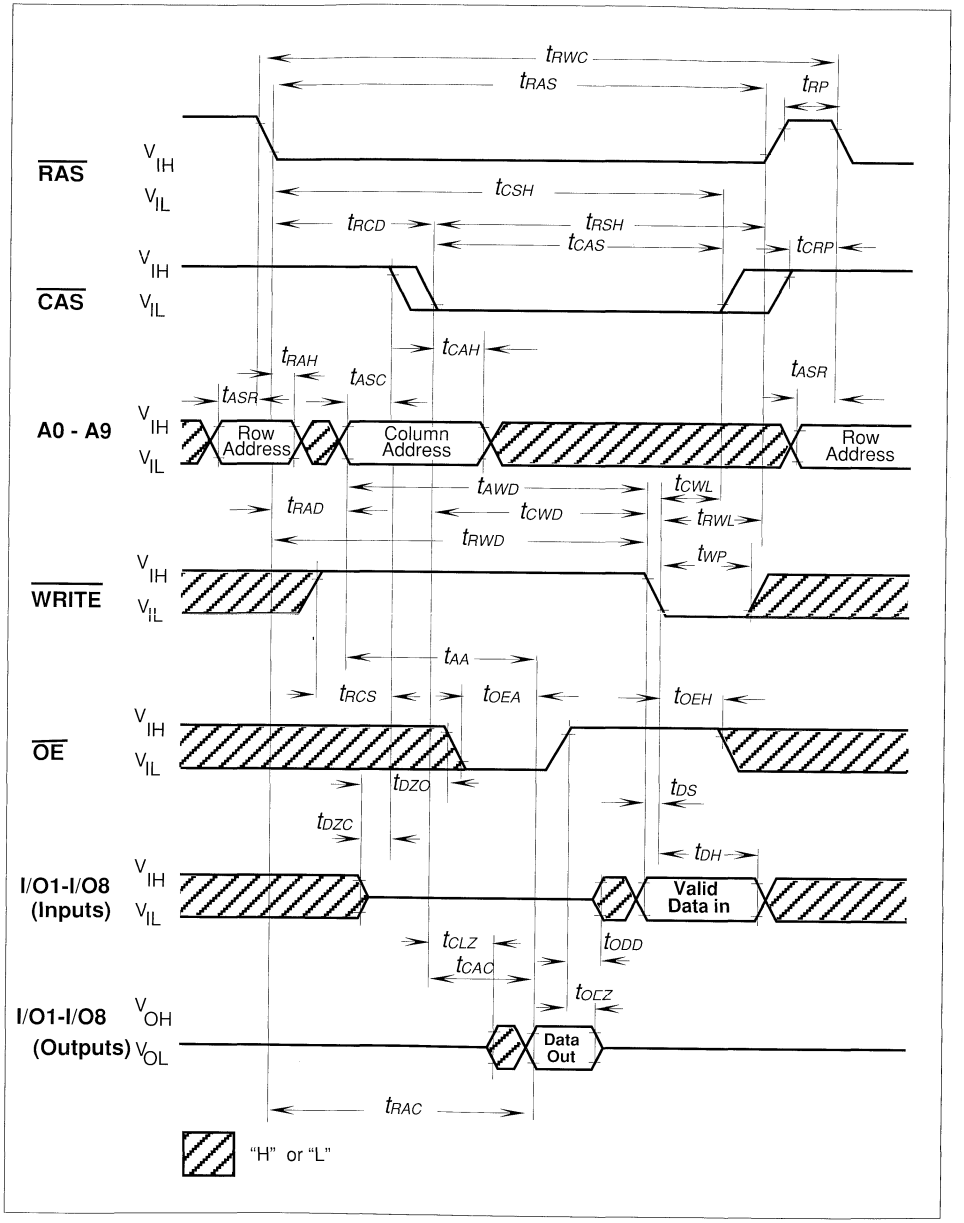
Read Cycle



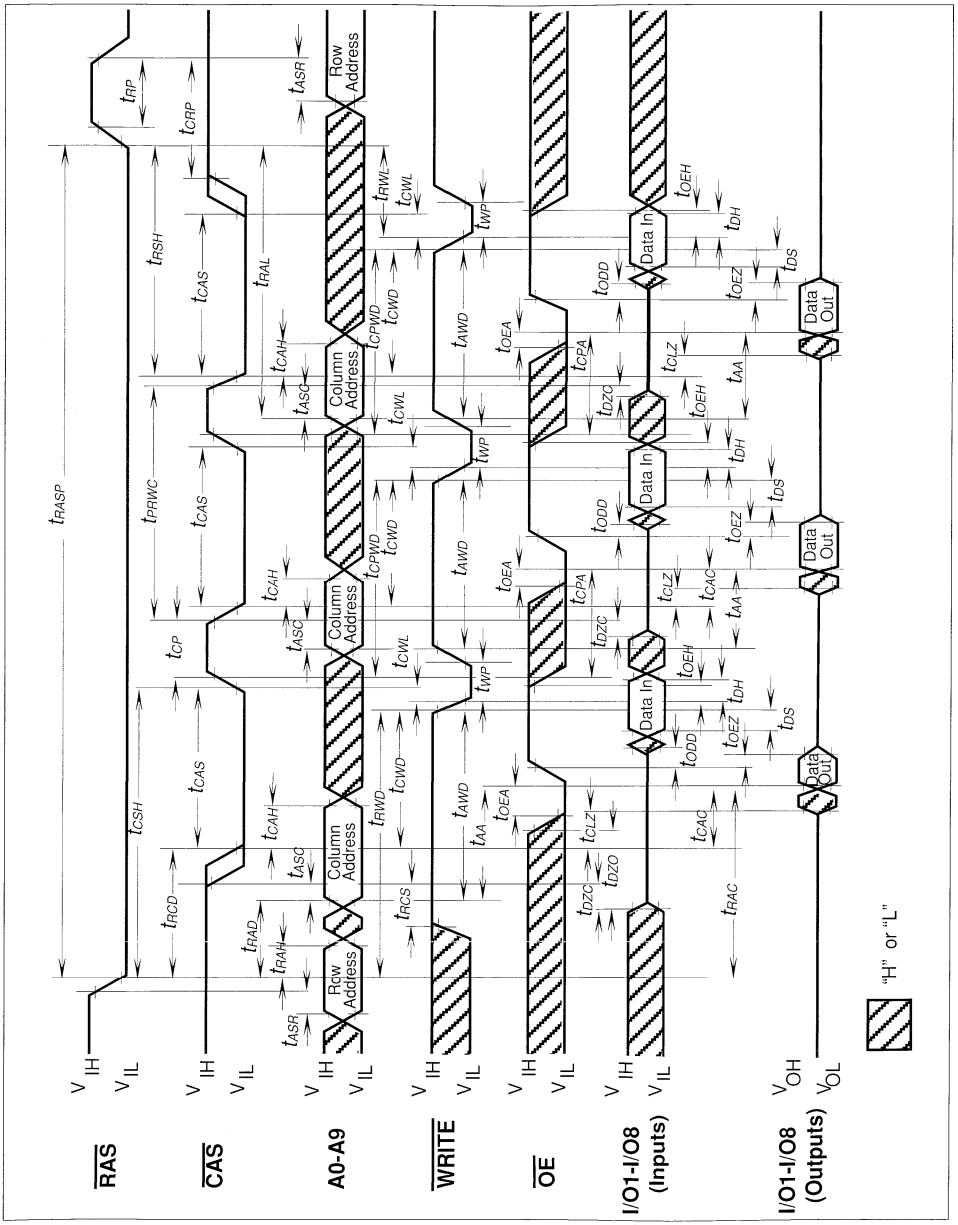
Write Cycle (Early Write)



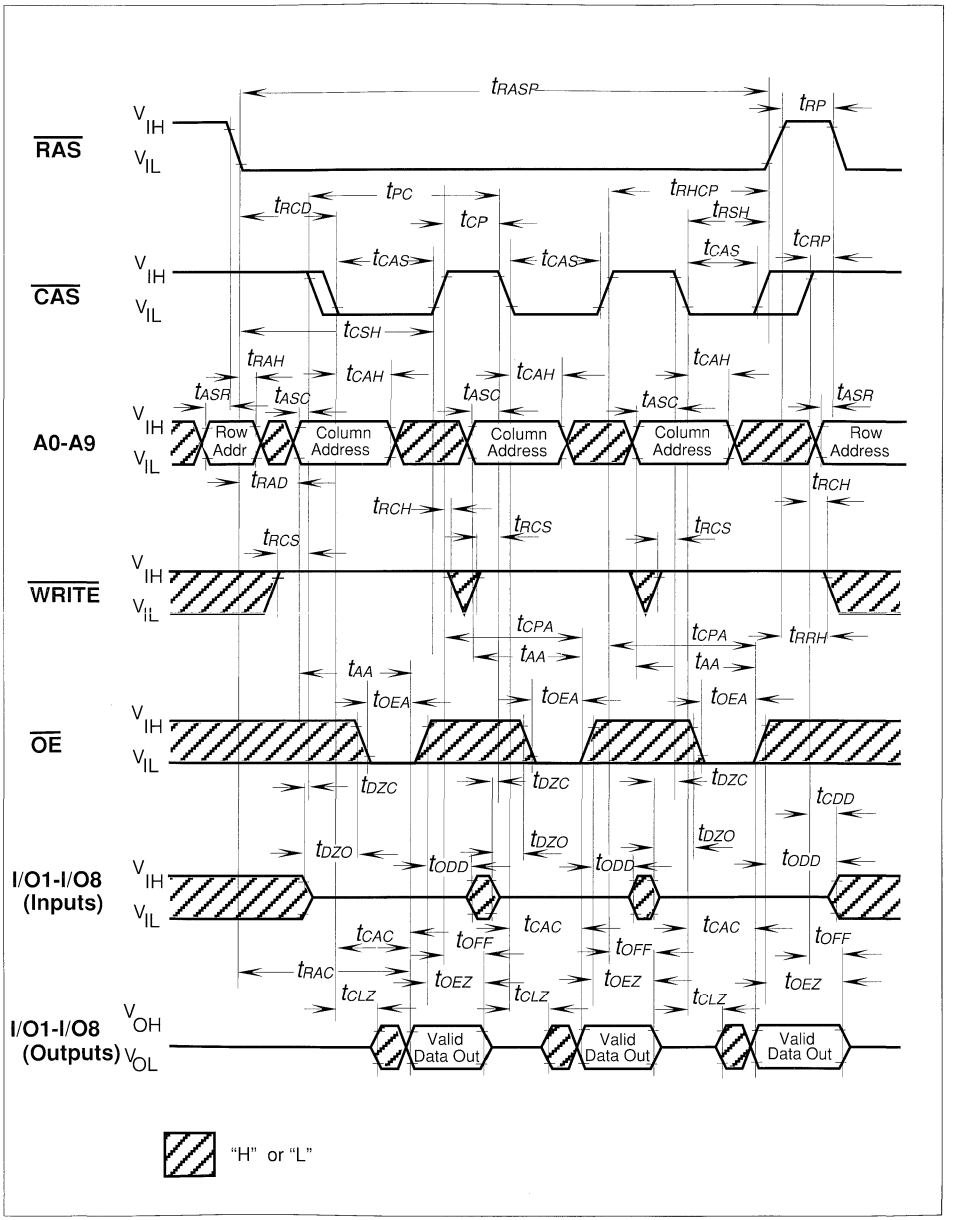
Write Cycle ($\overline{OE}$ Controlled Write)



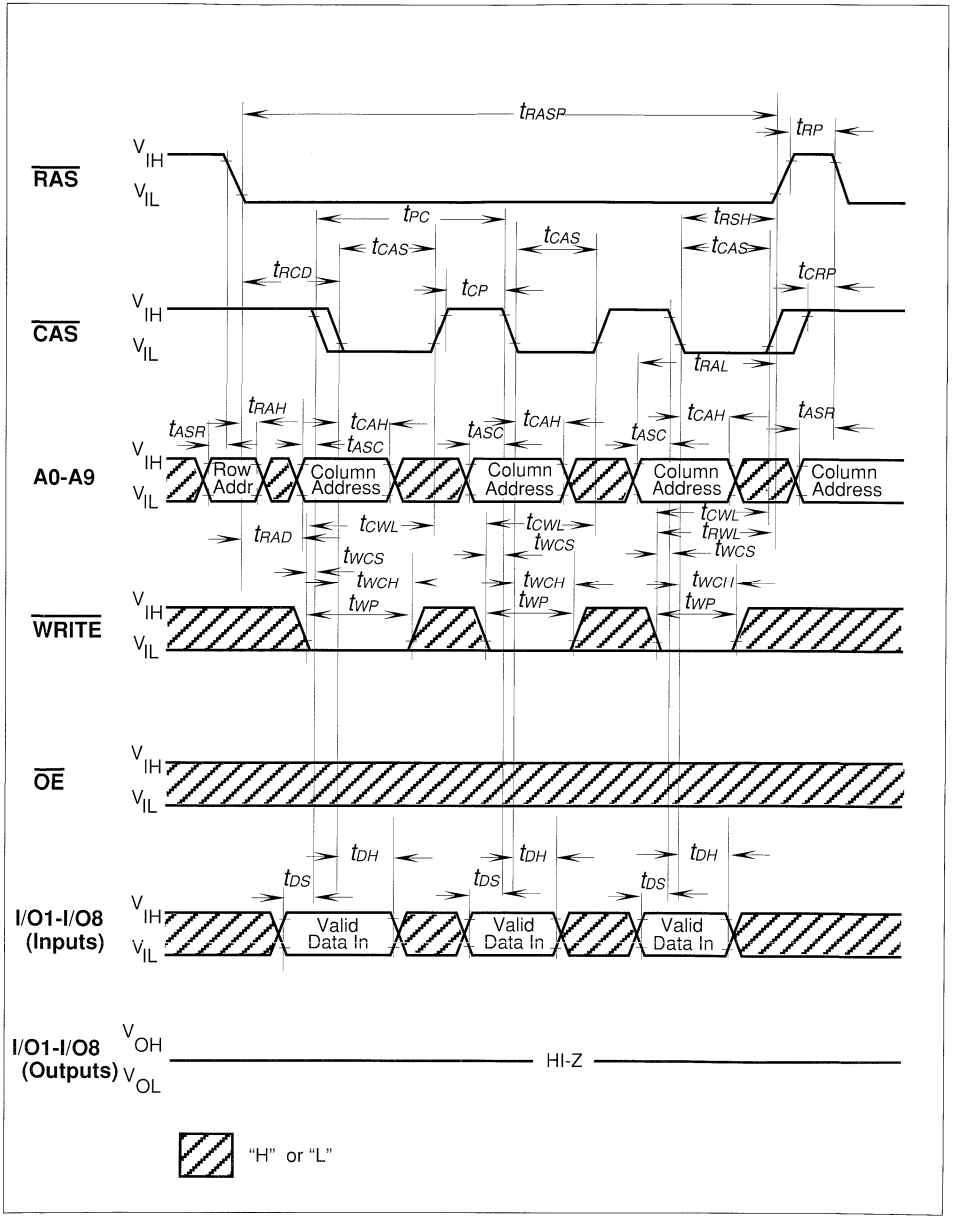
Read-Write (Read-Modify-Write) Cycle



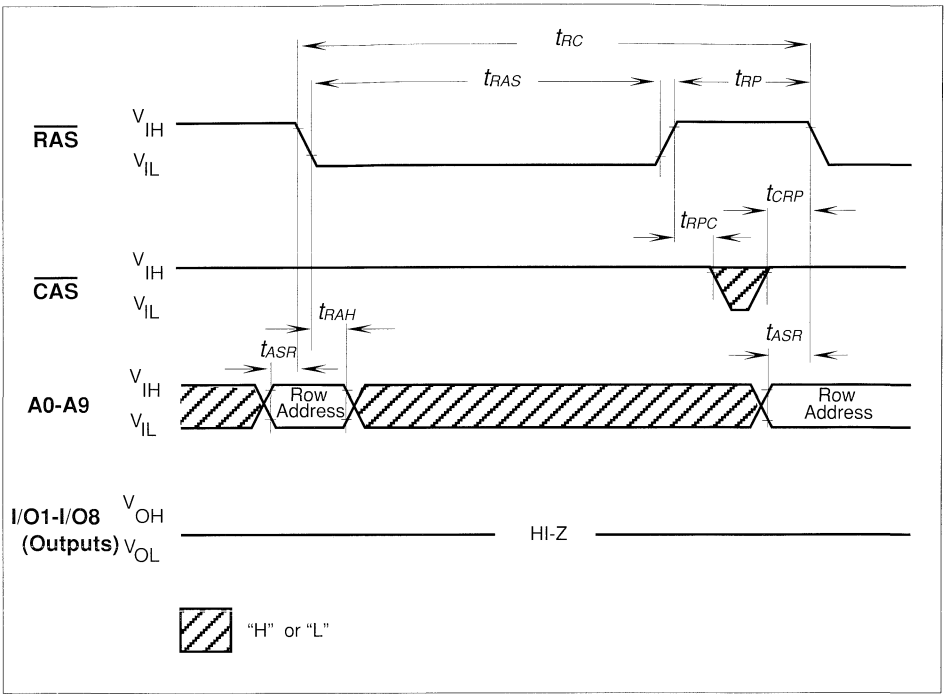
Fast Page Mode Read-Modify-Write Cycle



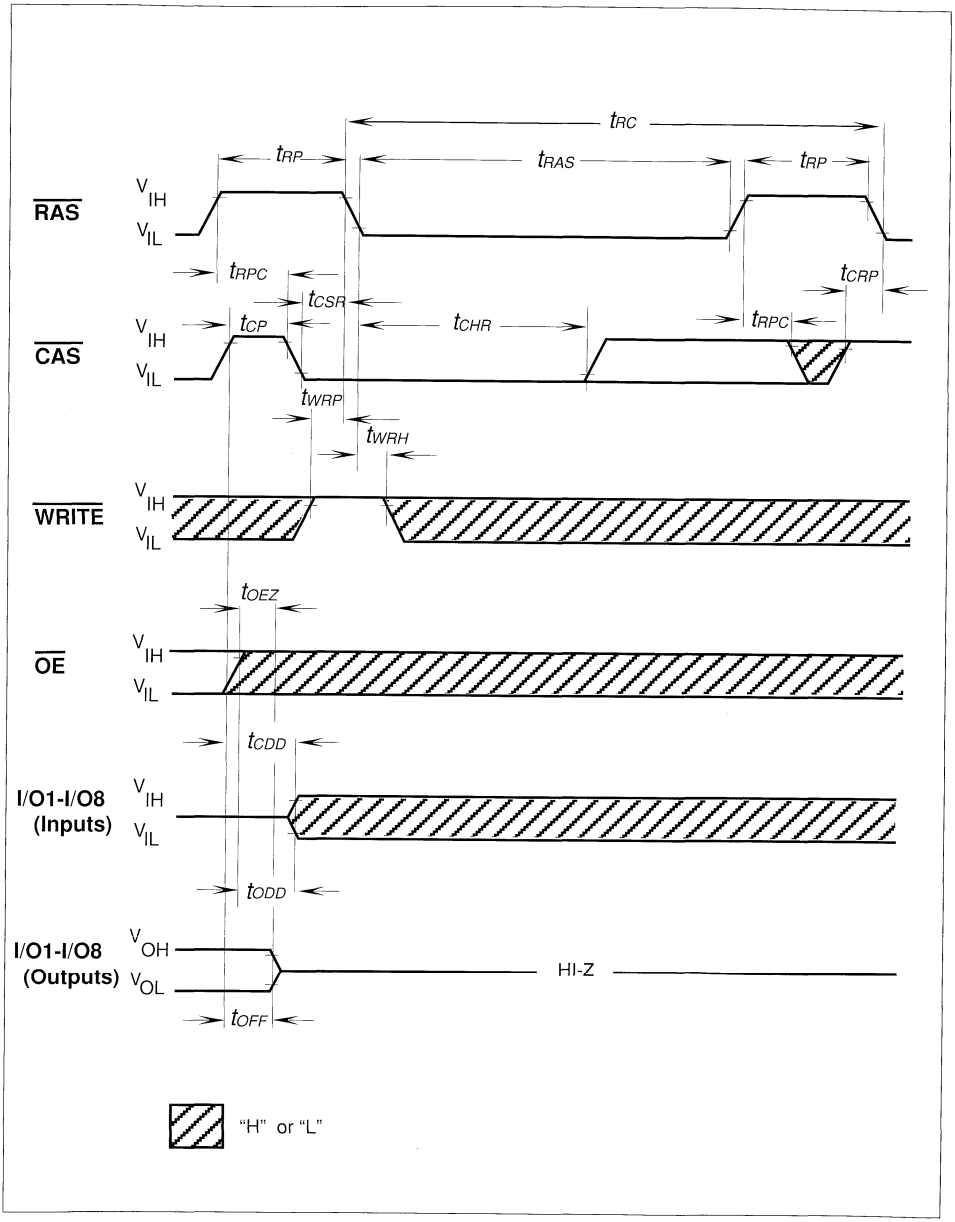
Fast Page Mode Read Cycle



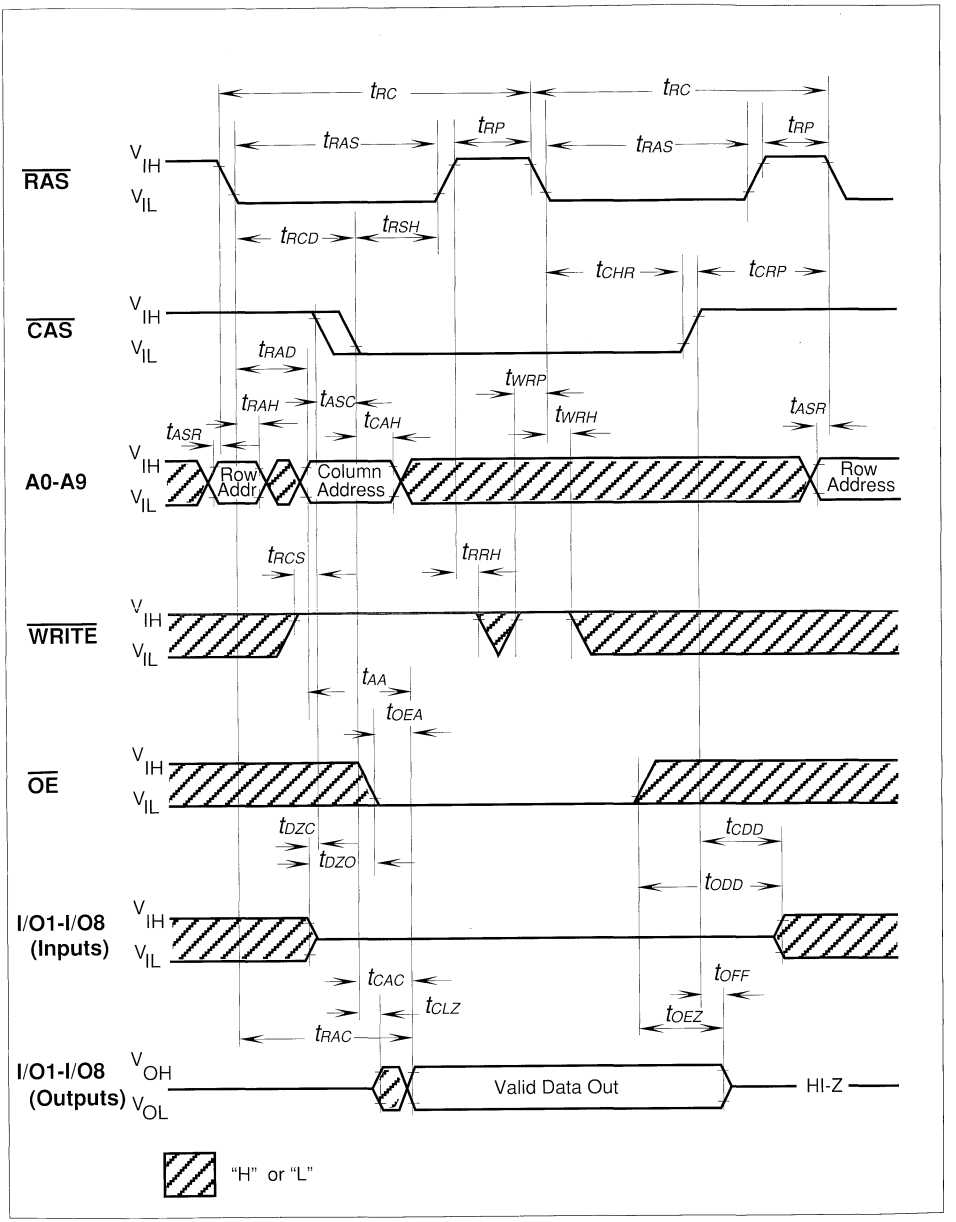
Fast Page Mode Early Write Cycle



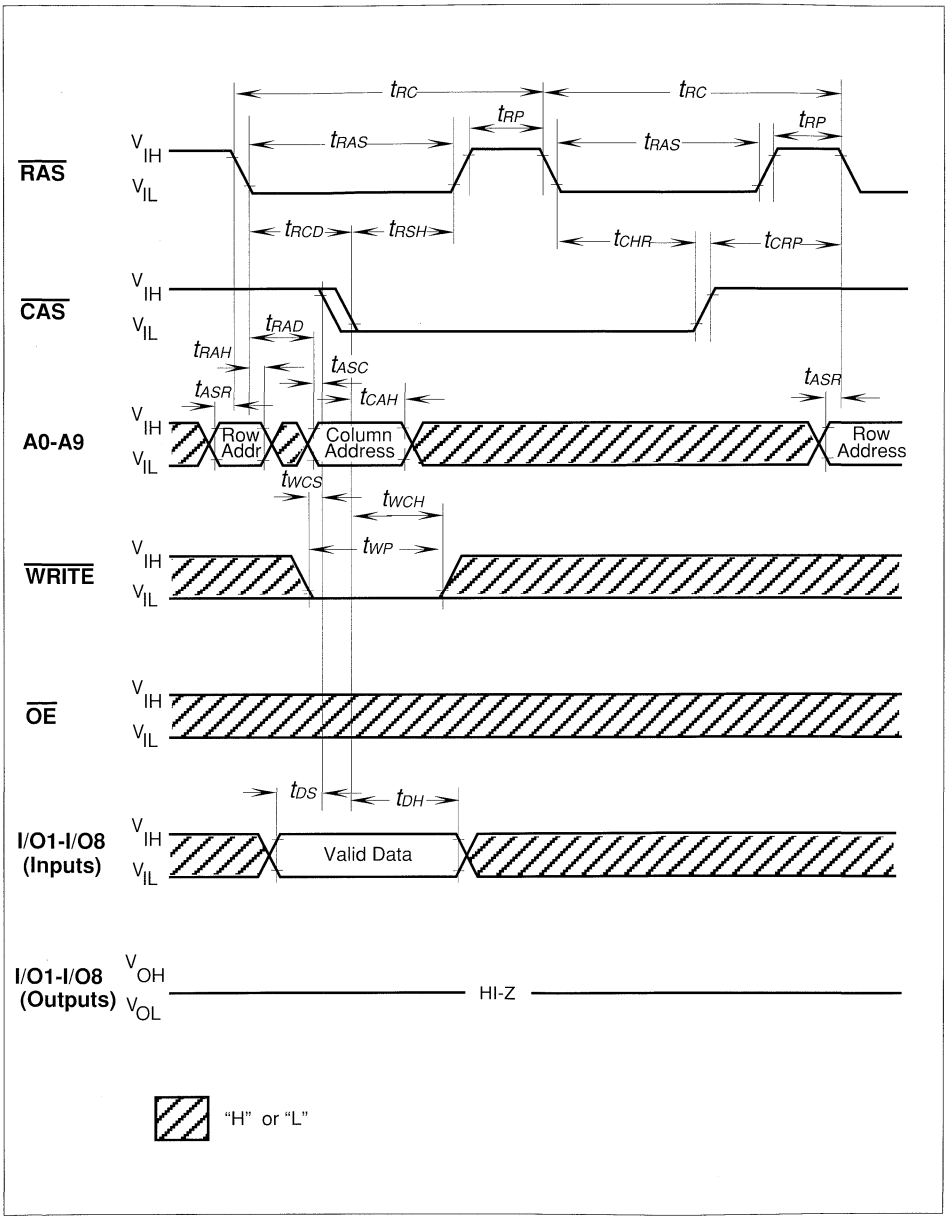
RAS-Only Refresh Cycle



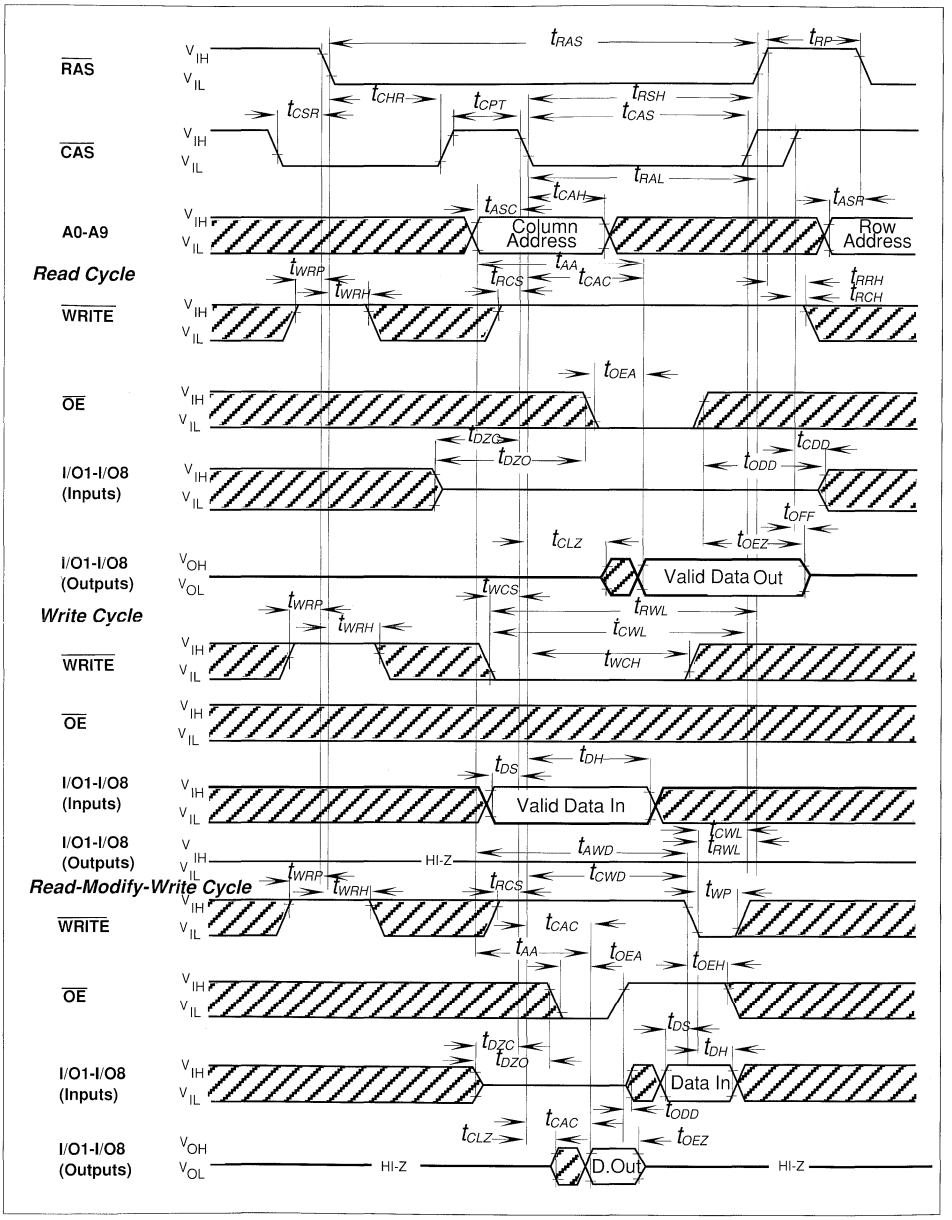
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Early Write)



CAS-Before-RAS Refresh Counter Test Cycle

256 K x 16-Bit Dynamic RAM

HYB 514171BJ-60/-70

Low Power 256 K x 16-Bit Dynamic RAM with Self Refresh

HYB 514171BJL-60/-70

Advanced Information

- 262 144 words by 16-bit organization
- 0 to 70 °C operating temperature
- Fast access and cycle time
- $\overline{RAS}$ access time:
  60 ns (-60 version)
  70 ns (-70 version)
- CAS access time:
  15ns (-60 version)
  20 ns (-70 version)
- Cycle time:
  110 ns (-60 version)
  130 ns (-70 version)
- Fast page mode cycle time
  40 ns (-60 version)
  45 ns (-70 version)
- Single + 5 V (± 10 %) supply with a built-in V_{BB} generator
- Low Power dissipation
  max. 1127.5 mW active (-60 version)
  max. 880 mW active (-70 version)
- Standby power dissipation
  11 mW standby (TLL)
  5.5 mW max. standby (CMOS)
  1.1 mW max. standby (CMOS) for Low Power Version
- Output unlatched at cycle end allows two-dimensional chip selection
- Read, write, read-modify write, CAS-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, hidden-refresh and fast page mode capability
- 2 $\overline{CAS}$ / 1 $\overline{WE}$ control
- Self Refresh (L-Version)
- All inputs and outputs TTL-compatible
- 512 refresh cycles / 16 ms
- 512 refresh cycles / 128 ms
  Low Power Version only
- Plastic Packages:
  P-SOJ-40-1 400mil width

Ordering Information

Type	Ordering Code	Package	Description
HYB 514171BJ-60	Q67100-Q727	P-SOJ-40-1	60 ns 256 K x 16 DRAM
HYB 514171BJ-70	Q67100-Q728	P-SOJ-40-1	70 ns 256 K x 16 DRAM
HYB 514171BJL-60	Q67100-Q932	P-SOJ-40-1	60 ns 256 K x 16 DRAM
HYB 514171BJL-70	Q67100-Q931	P-SOJ-40-1	70 ns 256 K x 16 DRAM

The HYB 514171BJ/BJL is the new generation dynamic RAM organized as 262 144 words by 16-bit. The HYB 514171BJ/BJL utilizes CMOS silicon gate process as well as advanced circuit techniques to provide wide operation margins, both internally and for the system user. Multiplexed address inputs permit the HYB 514171BJ/BJL to be packed in a standard plastic 400mil wide P-SOJ-40-1 package. This package size provides high system bit densities and is compatible with commonly used automatic testing and insertion equipment. System oriented features include Self Refresh (L-Version), single + 5 V (± 10 %) power supply, direct interfacing with high performance logic device families such as Schottky TTL.

Pin Definitions and Functions

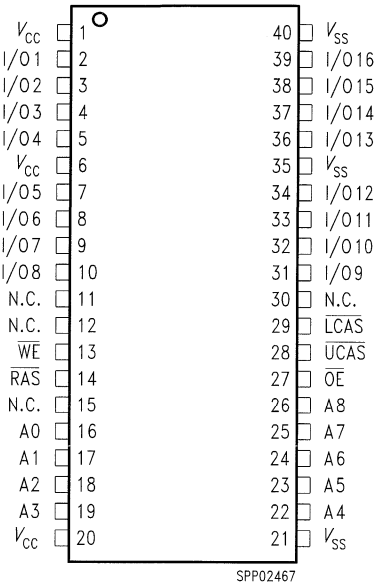
Pin No.	Function
A0-A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$, $\overline{LCAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1 – I/O16	Data Input/Output
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground (0 V)
N.C.	No Connection

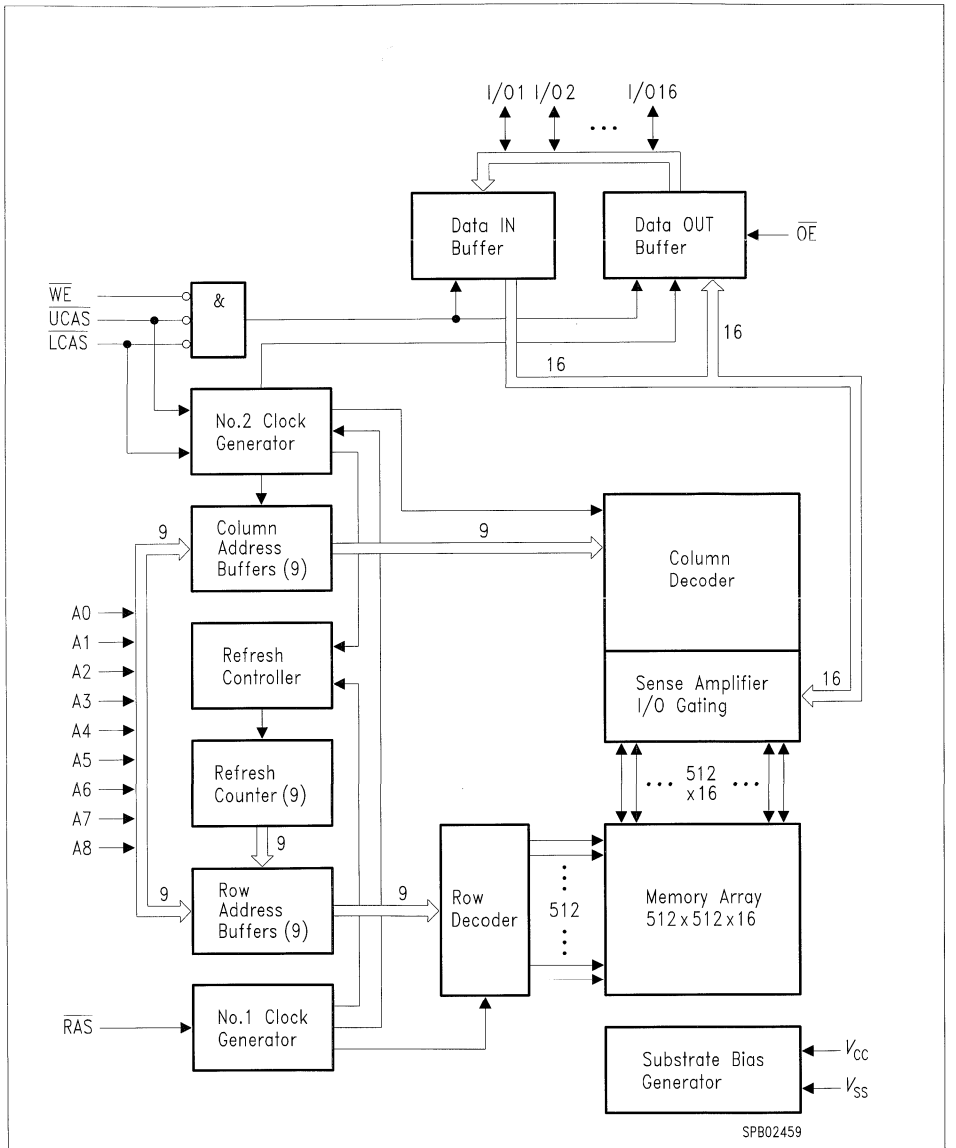
Truth Table

$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	I/O1-I/O8	I/O9-I/O16	Operation
H	H	H	H	H	High-Z	High-Z	Standby
L	H	H	H	H	High-Z	High-Z	Refresh
L	L	H	H	L	Dout	High-Z	Lower byte read
L	H	L	H	L	High-Z	Dout	Upper byte read
L	L	L	H	L	Dout	Dout	Word read
L	L	H	L	H	Din	Don't care	Lower byte write
L	H	L	L	H	Don't care	Din	Upper byte write
L	L	L	L	H	Din	Din	Word write
L	L	L	H	H	High-Z	High-Z	

Pin Configuration
(top view)

P-SOJ-40-1





Block Diagram

Absolute Maximum Ratings

Operating temperature range ..... 0 to + 70 °C
Storage temperature range ..... – 55 to + 150 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 1 to + 7 V
Power supply voltage ..... – 1 to + 7 V
Data out current (short circuit) ..... 50 mA

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC Characteristics

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	6.5	V	1)
Input low voltage	V_{IL}	– 1.0	0.8	V	1)
Output high voltage (I_{OUT} = – 5.0 mA)	V_{OH}	2.4	–	V	1)
Output low voltage (I_{OUT} = 4.2 mA)	V_{OL}	–	0.4	V	1)
Input leakage current, any input (0 V < V_{IN} < 7 V, all other inputs = 0 V)	$I_{I(L)}$	– 10	10	µA	1)
Output leakage current (DO is disabled, 0 V < V_{OUT} < V_{CC})	$I_{O(L)}$	– 10	10	µA	1)
Average V_{CC} supply current: -60 version -70 version	I_{CC1}		170 160	mA	2) 3)
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{LCAS}$ = $\overline{UCAS}$ = $\overline{WE}$ = V_{IH})	I_{CC2}		2	mA	–
Average V_{CC} supply current during $\overline{RAS}$-only refresh cycles: -60 version -70 version	I_{CC3}		170 160	mA	2)

DC Characteristics (cont'd)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current during fast page mode operation: -60 version -70 version	I_{CC4}		150 140	mA	2) 3)
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{LCAS}$ = $\overline{UCAS}$ = $\overline{WE}$ = V_{CC} – 0.2 V)	I_{CC5}		1	mA	1)
Average V_{CC} supply current during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode: -60 version -70 version	I_{CC6}		170 160	mA	2)
Standby V_{CC} current (L-version) ($\overline{RAS}$ = $\overline{LCAS}$ = $\overline{UCAS}$ = $\overline{WE}$= V_{CC} – 0.2 V)	I_{CC5}		200	µA	
Self Refresh Current (L-version) ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$ = 0.2V A0 – A8 = V_{CC} – 0.2 V or 0.2 V)	I_{CCS}		300	µA	

AC Characteristics [4]

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values				Unit
		-60		-70		
		min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	110	–	130	–	ns
Read-write cycle time	t_{RWC}	160	–	185	–	ns
Fast page mode cycle time	t_{PC}	40	–	45	–	ns
Fast page mode read/write cycle time	t_{PRWC}	90	–	100	–	ns
Access time from $\overline{RAS}$ [6) 11)]	t_{RAC}	–	60	–	70	ns
Access time from $\overline{CAS}$ [6) 11)]	t_{CAC}	–	15	–	20	ns
Access time from column address [6) 12)]	t_{AA}	–	30	–	35	ns
Access time from $\overline{CAS}$ precharge[6)]	t_{CPA}	–	35	–	40	ns
$\overline{CAS}$ to output in low-Z [6)]	t_{CLZ}	0	–	0	–	ns
Output buffer turn-off delay from $\overline{CAS}$ [7)]	t_{OFF}	0	20	0	20	ns
Transition time (rise and fall) [5)]	t_T	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	40	–	50	–	ns
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	ns
$\overline{RAS}$ pulse width in fast page mode	t_{RASP}	60	200000	70	200000	ns
$\overline{CAS}$ pulse width	t_{CAS}	15	10000	20	10000	ns
$\overline{RAS}$ hold time	t_{RSH}	15	–	20	–	ns
$\overline{CAS}$ hold time	t_{CSH}	50	–	60	–	ns
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge (Fast page mode)	t_{RHCP}	35	–	45	–	ns
$\overline{CAS}$ precharge to $\overline{WE}$ delay time (FPM read-modify-write)	t_{CPWD}	60	–	65	–	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time [11)]	t_{RCD}	20	45	20	50	ns
$\overline{RAS}$ to column address delay time [12)]	t_{RAD}	15	30	15	35	ns

Parameter	Symbol	Limit Values				Unit
		-60		-70		
		min.	max.	min.	max.	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	ns
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	ns
Row address hold time	t_{RAH}	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	ns
Column address hold time	t_{CAH}	15	–	15	–	ns
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	–	35	–	ns
Read command setup time	t_{RCS}	0	–	0	–	ns
Read command hold time[8)]	t_{RCH}	0	–	0	–	ns
Read command hold time ref. to $\overline{RAS}$ [8)]	t_{RRH}	0	–	0	–	ns
Write command hold time	t_{WCH}	10	–	15	–	ns
Write command pulse width	t_{WP}	10	–	15	–	ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	–	20	–	ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	–	20	–	ns
Data setup time [9)]	t_{DS}	0	–	0	–	ns
Data hold time [9)]	t_{DH}	15	–	15	–	ns
Refresh period	t_{REF}	–	16	–	16	ms
Refresh period (L-version)	t_{REF}	–	128	–	128	ms
Write command setup time[10)]	t_{WCS}	0	–	0	–	ns
$\overline{CAS}$ to $\overline{WE}$ delay time[10)]	t_{CWD}	45	–	50	–	ns
$\overline{RAS}$ to $\overline{WE}$ delay time[10)]	t_{RWD}	90	–	100	–	ns
Column address to $\overline{WE}$ delay time [10)]	t_{AWD}	60	–	65	–	ns
$\overline{CAS}$ setup time (CBR cycle)	t_{CSR}	5	–	5	–	ns
$\overline{CAS}$ hold time (CBR cycle)	t_{CHR}	10	–	10	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	0	–	0	–	ns
$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ counter test cycle)	t_{CPT}	30	–	40	–	ns

Parameter	Symbol	Limit Values				Unit
		-60		-70		
		min.	max.	min.	max.	
Write to $\overline{RAS}$ precharge time (CBR cycle)	t_{WRP}	10	–	10	–	ns
Write to $\overline{RAS}$ hold time (CBR cycle)	t_{WRH}	10	–	10	–	ns
$\overline{OE}$ command hold time	t_{OEH}	20	–	20	–	ns
$\overline{OE}$ access time	t_{OEA}	–	15	–	20	ns
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	10	–	10	–	ns
Output buffer turn-off delay from $\overline{OE}$	t_{OEZ}	0	20	0	20	ns
Data to $\overline{CAS}$ low delay [14]	t_{DZC}	0	–	0	–	ns
Data to $\overline{OE}$ low delay [14]	t_{DZO}	0	–	0	–	ns
$\overline{CAS}$ high to data delay [15]	t_{CDD}	20	–	20	–	ns
$\overline{OE}$ high to data delay [15]	t_{ODD}	20	–	20	–	ns
$\overline{RAS}$ pulse width Self Refresh (L-Version)	t_{RASS}	100	–	100	–	µs
$\overline{RAS}$ precharge time Self Refresh (L-Version)	t_{RPS}	110	–	130	–	ns
$\overline{CAS}$ hold time Self Refresh (L-Version)	t_{CHS}	40	–	50	–	ns

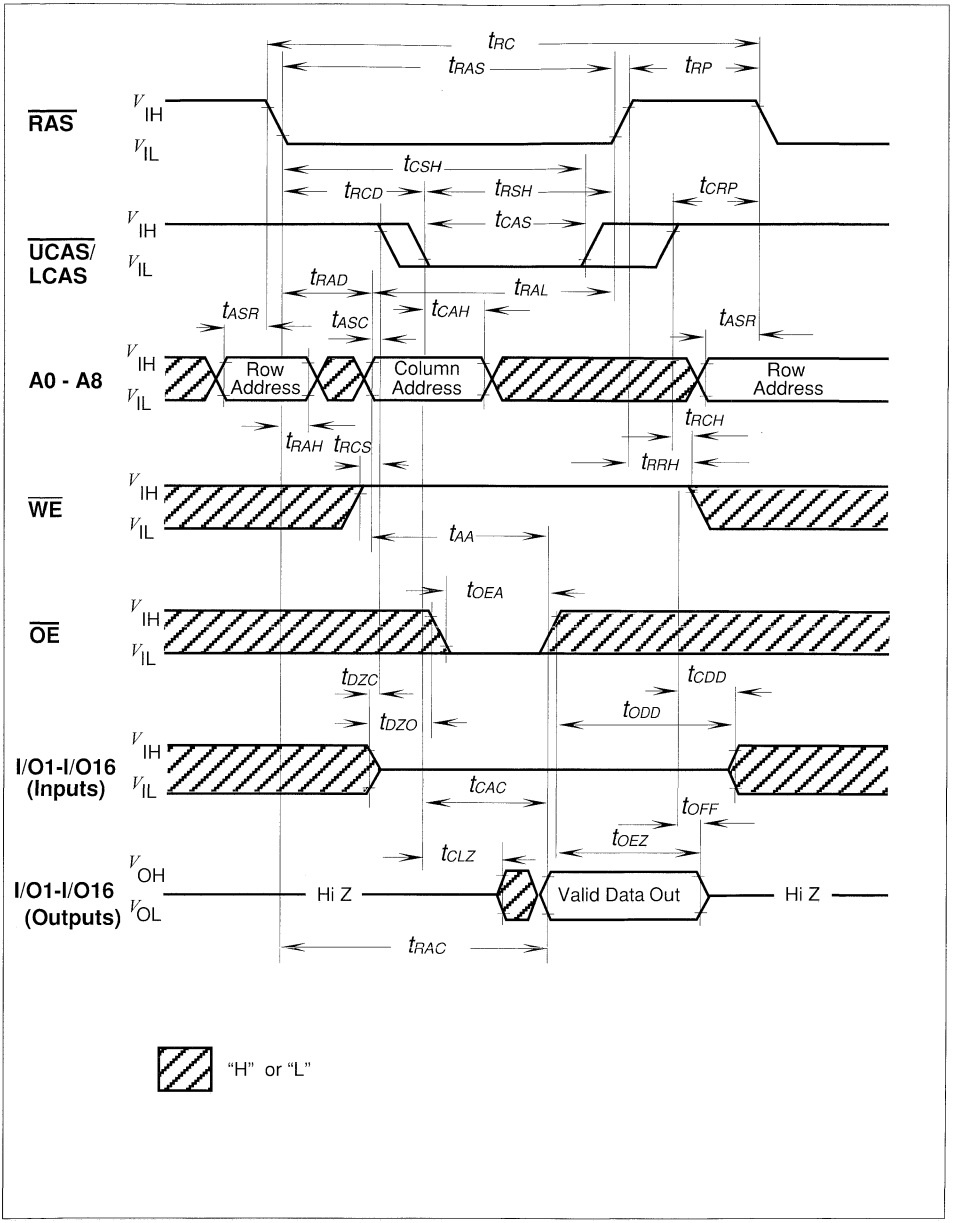
Capacitance

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %, f = 1 MHz

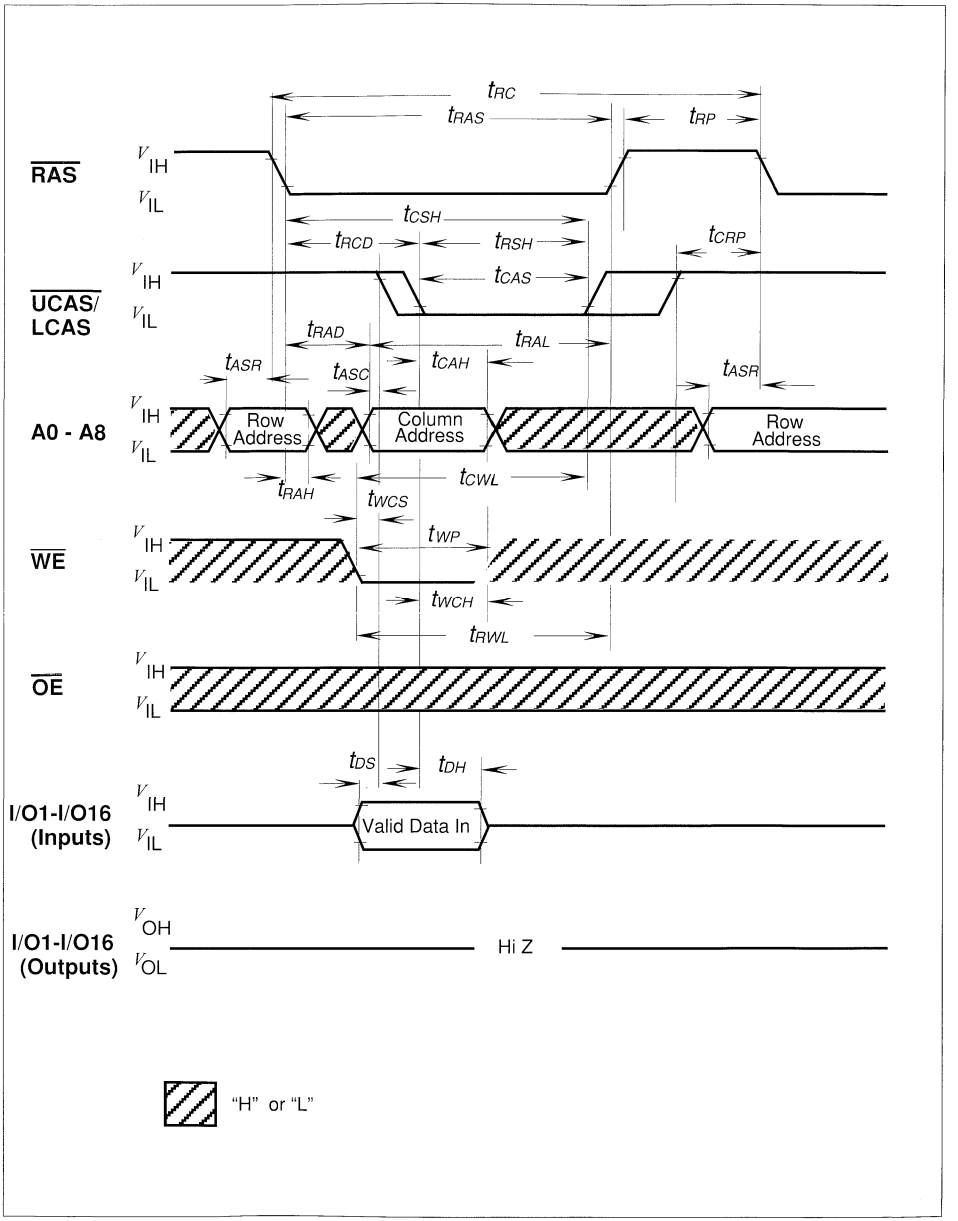
Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A8)	C_{I1}	–	6	pF
Input capacitance ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}	–	7	pF
Output capacitance (I/O1 to I/O16)	C_{IO}	–	7	pF

Notes:

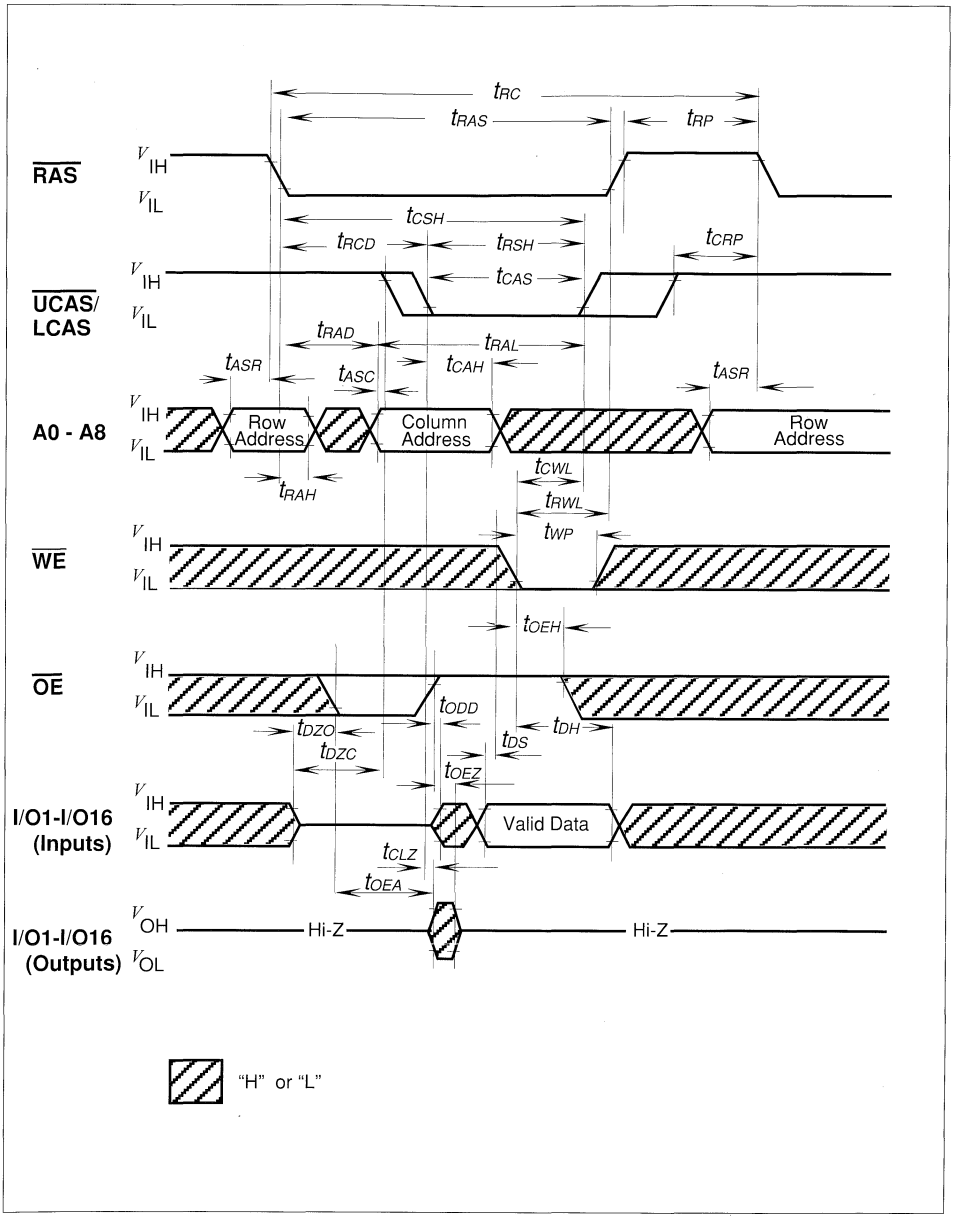
1) All voltages are referenced to V_{SS}.
2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
3) I_{CC1} and I_{CC4} depend on output loading.
4) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using the internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
5) $V_{IH\ (min.)}$ and $V_{IL\ (max.)}$ are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.
6) Measured with a load equivalent to 2 TTL loads and 100 pF.
7) $t_{OFF\ (max.)}$, $t_{OEZ\ (max.)}$ define the time at which the output achieves the open-circuit conditions and are not referenced to output voltage levels.
8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9) These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.
10) t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS\ (min.)}$, the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} > t_{RWD\ (min.)}$, $t_{CWD} > t_{CWD\ (min.)}$ and $t_{AWD} > t_{AWD\ (min.)}$, the cycle is a read-write cycle and I/O will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of I/O (at access time) is indeterminate.
11) Operation within the $t_{RCD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RCD\ (max.)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD\ (max.)}$ limit, then access time is controlled by t_{CAC}.
12) Operation within the $t_{RAD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RAD\ (max.)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD\ (max.)}$ limit, then access time is controlled by t_{AA}.
13) AC measurements assume t_T = 5 ns.
14) Either t_{DZC} or t_{DZO} must be satisfied.
15) Either t_{CDD} or t_{ODD} must be satisfied.


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
tCAS
UCAS/
LCAS
tRAD
tRAL
tASR
tASC
tCAH
tASR
A0 - A8
Row Address
Column Address
Row Address
tRCH
tRAH
tRCS
tRRH
WE
tAA
tOEA
OE
tDZC
tCDD
tDZO
tODD
I/O1-I/O16 (Inputs)
tCAC
tOFF
tOEZ
tCLZ
VOH
VOL
I/O1-I/O16 (Outputs)
Hi Z
Valid Data Out
Hi Z
tRAC
"H" or "L"

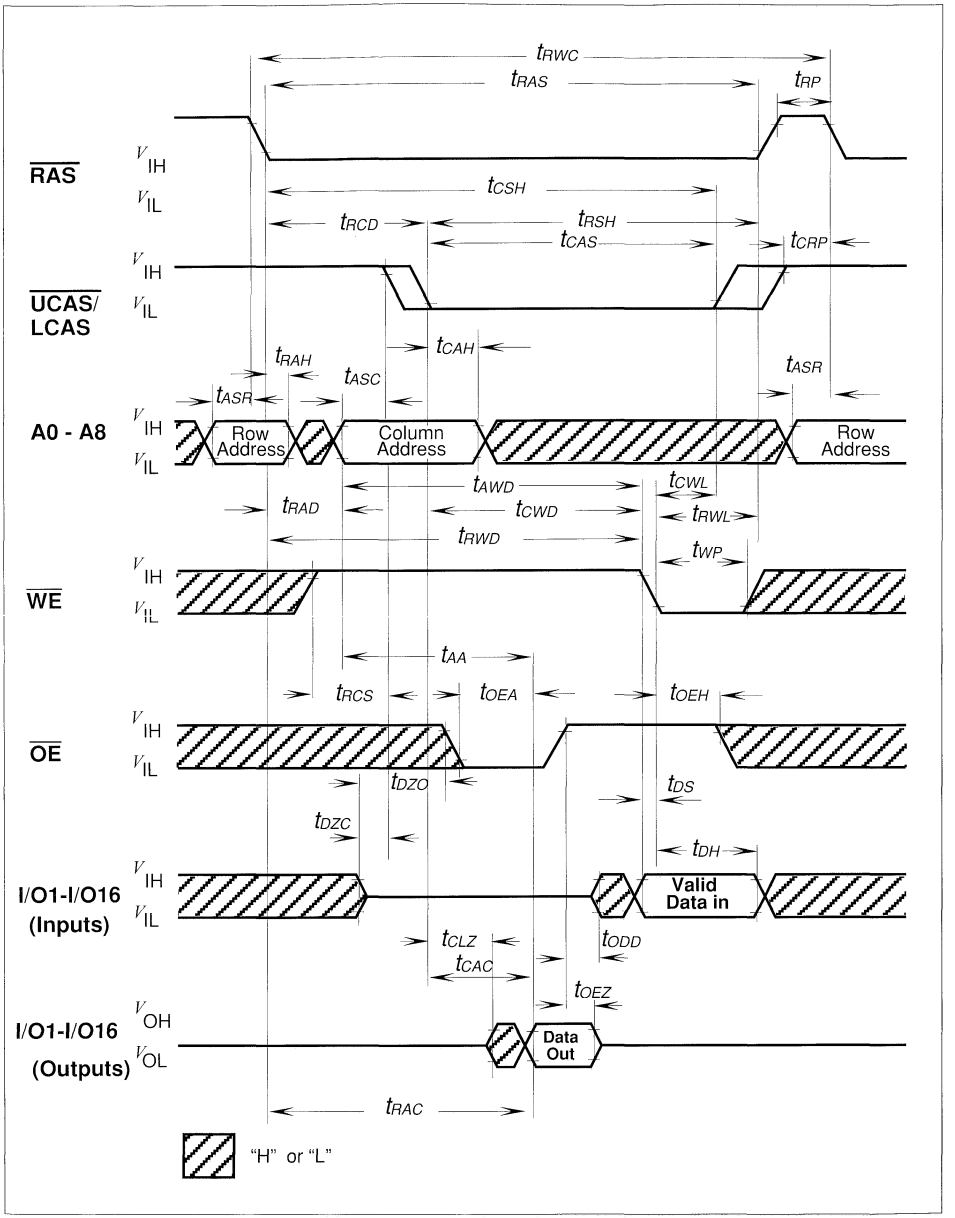
Read Cycle



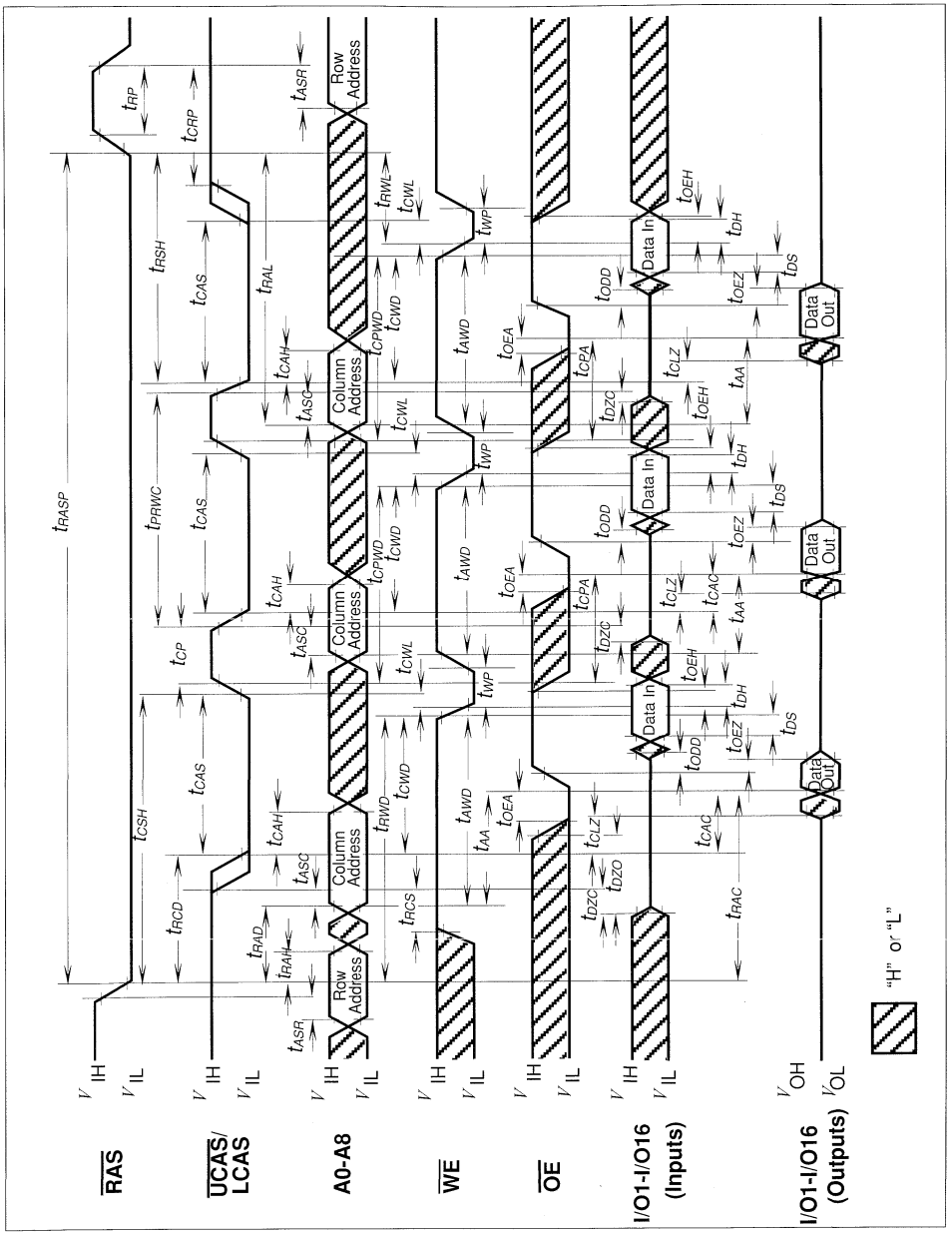
Write Cycle (Early Write)



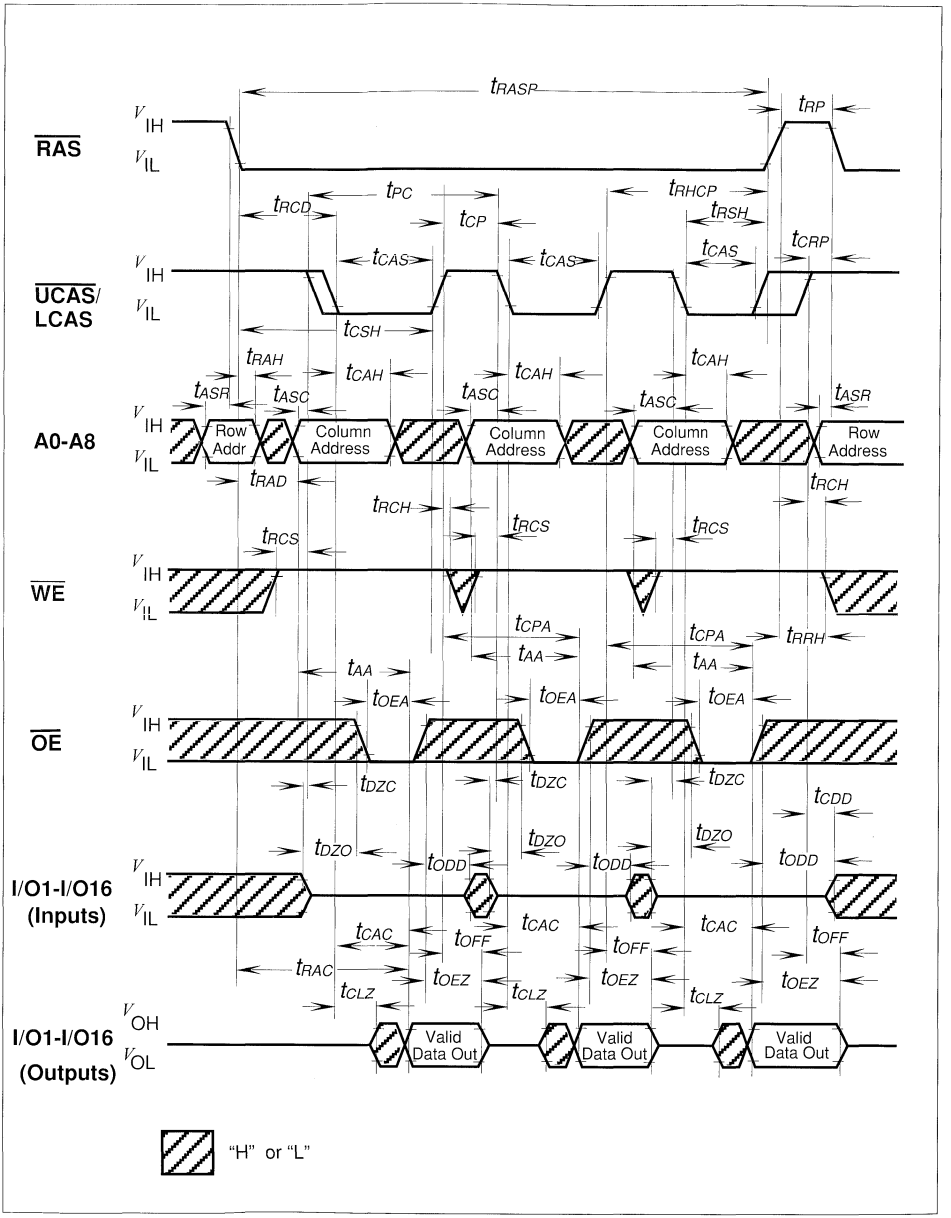
Write Cycle ($\overline{OE}$ Controlled Write)



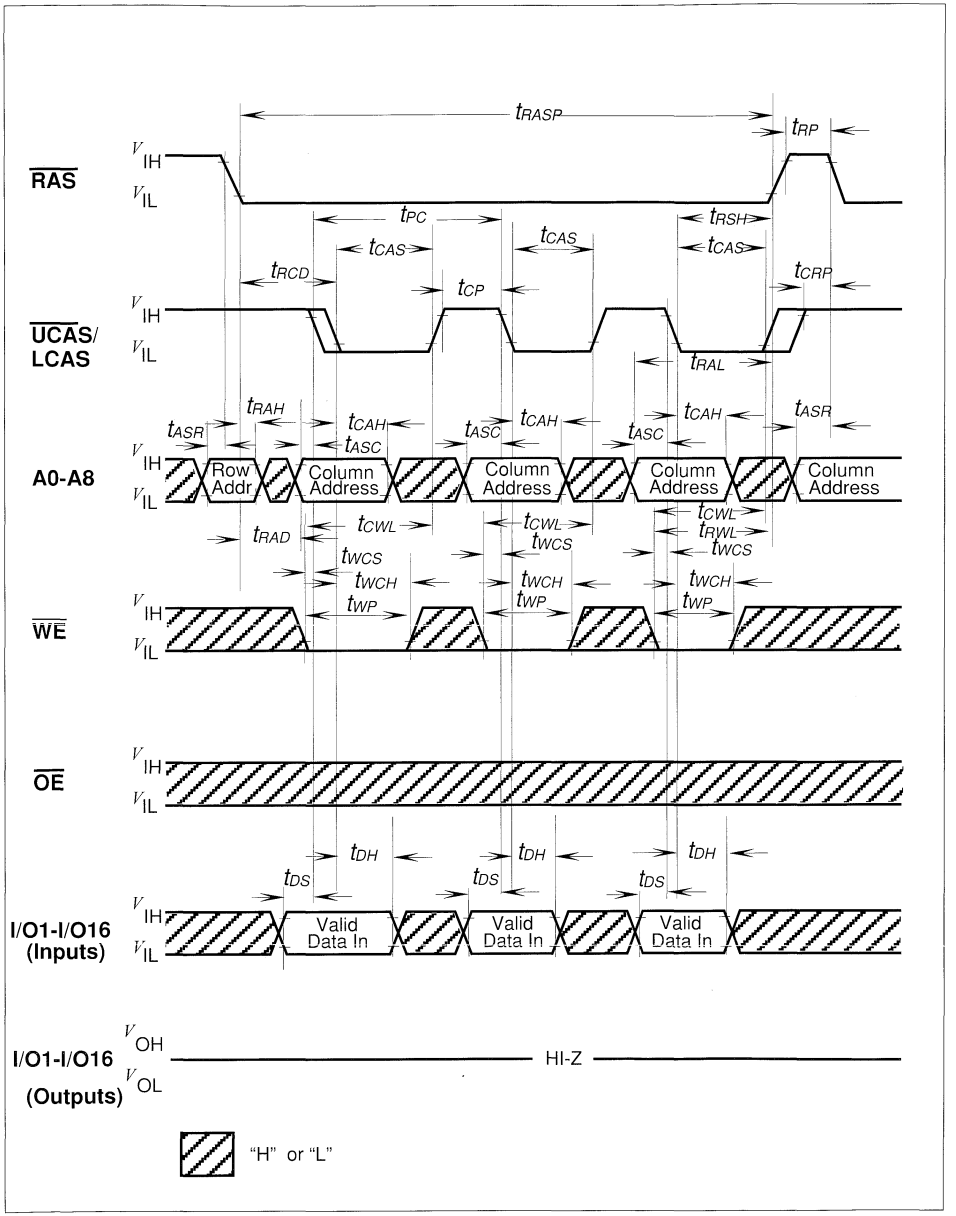
Read-Write (Read-Modify-Write) Cycle



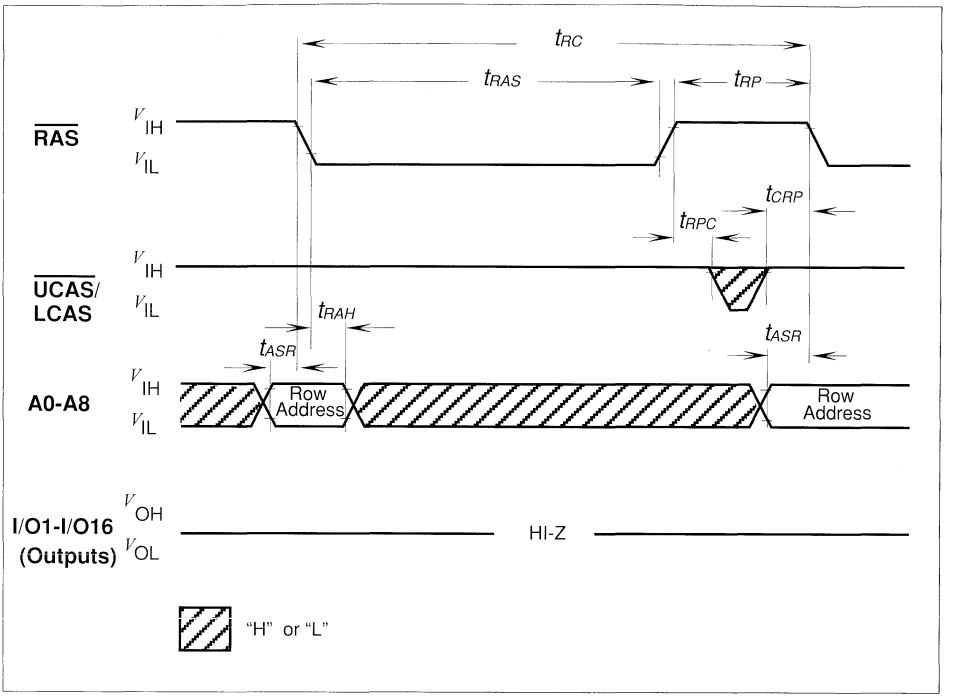
Fast Page Mode Read-Modify-Write Cycle



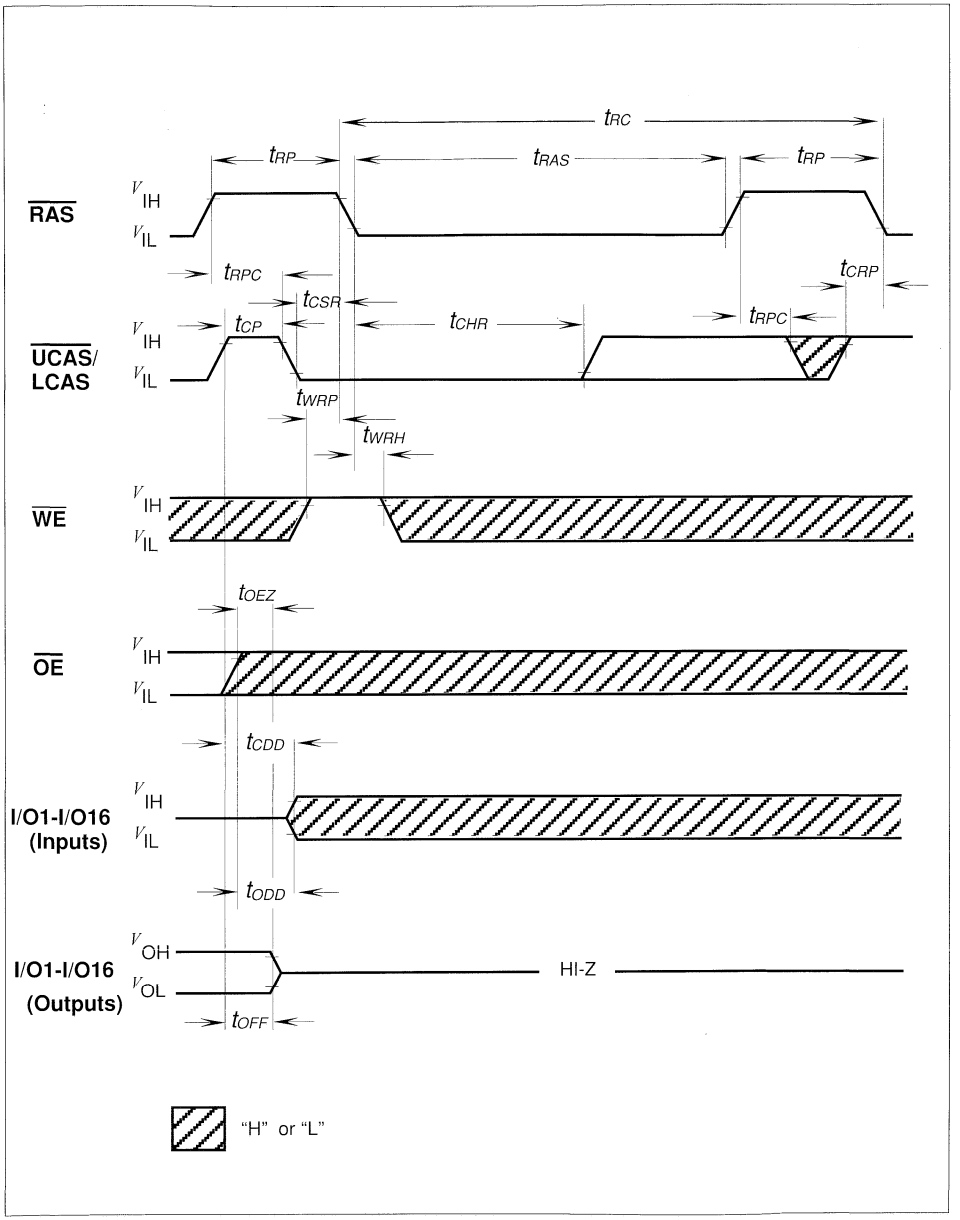
Fast Page Mode Read Cycle



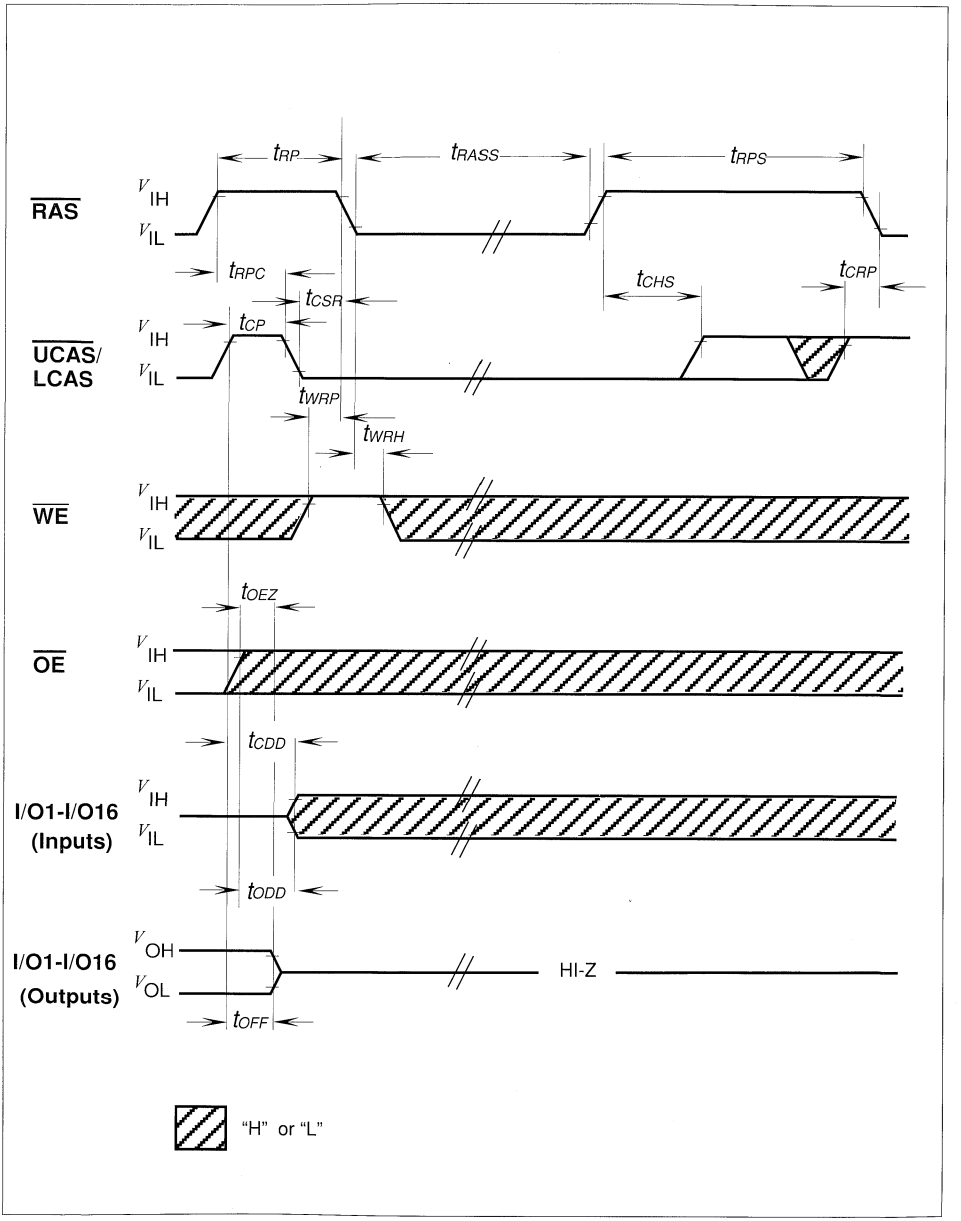
Fast Page Mode Early Write Cycle



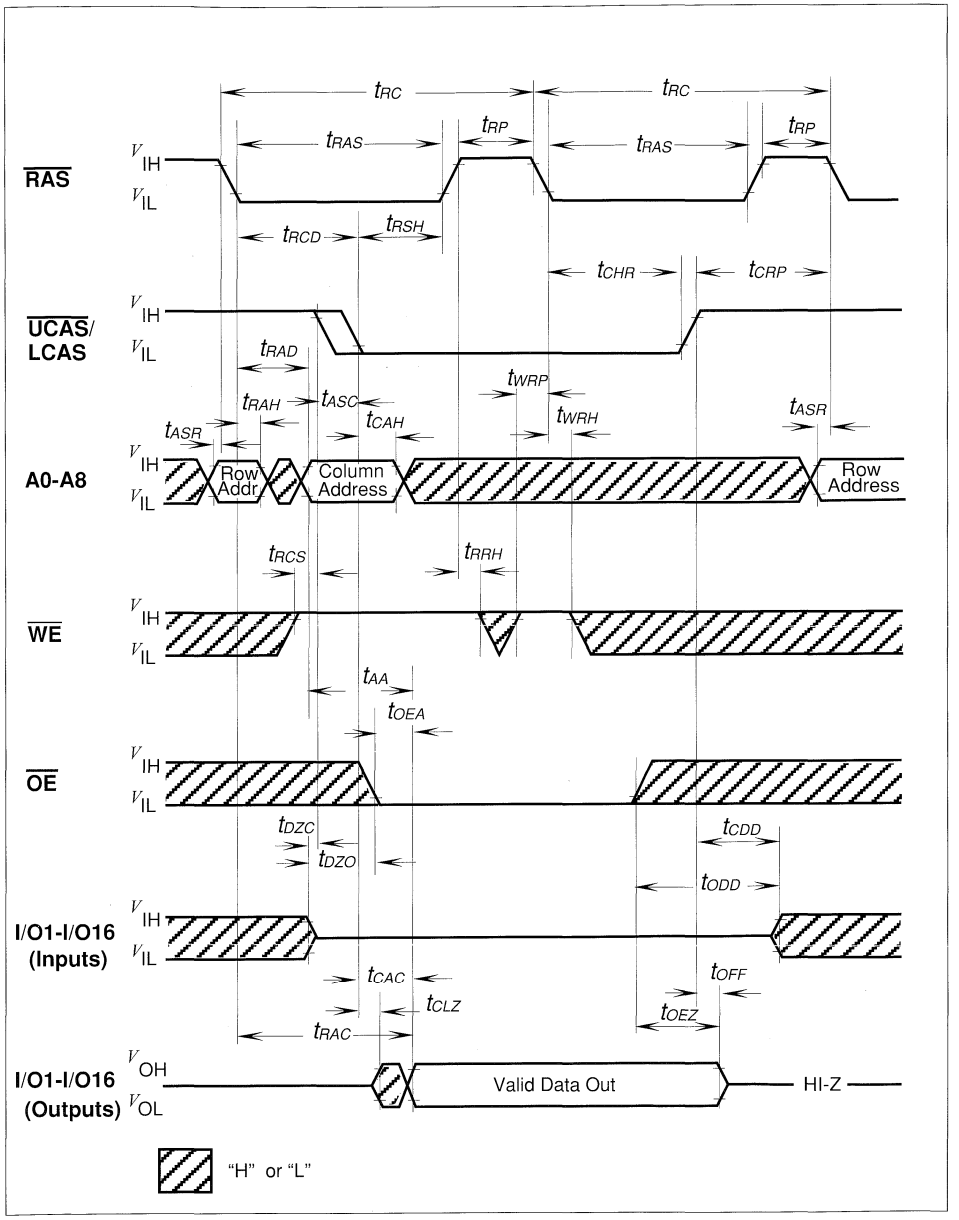
RAS-Only Refresh Cycle



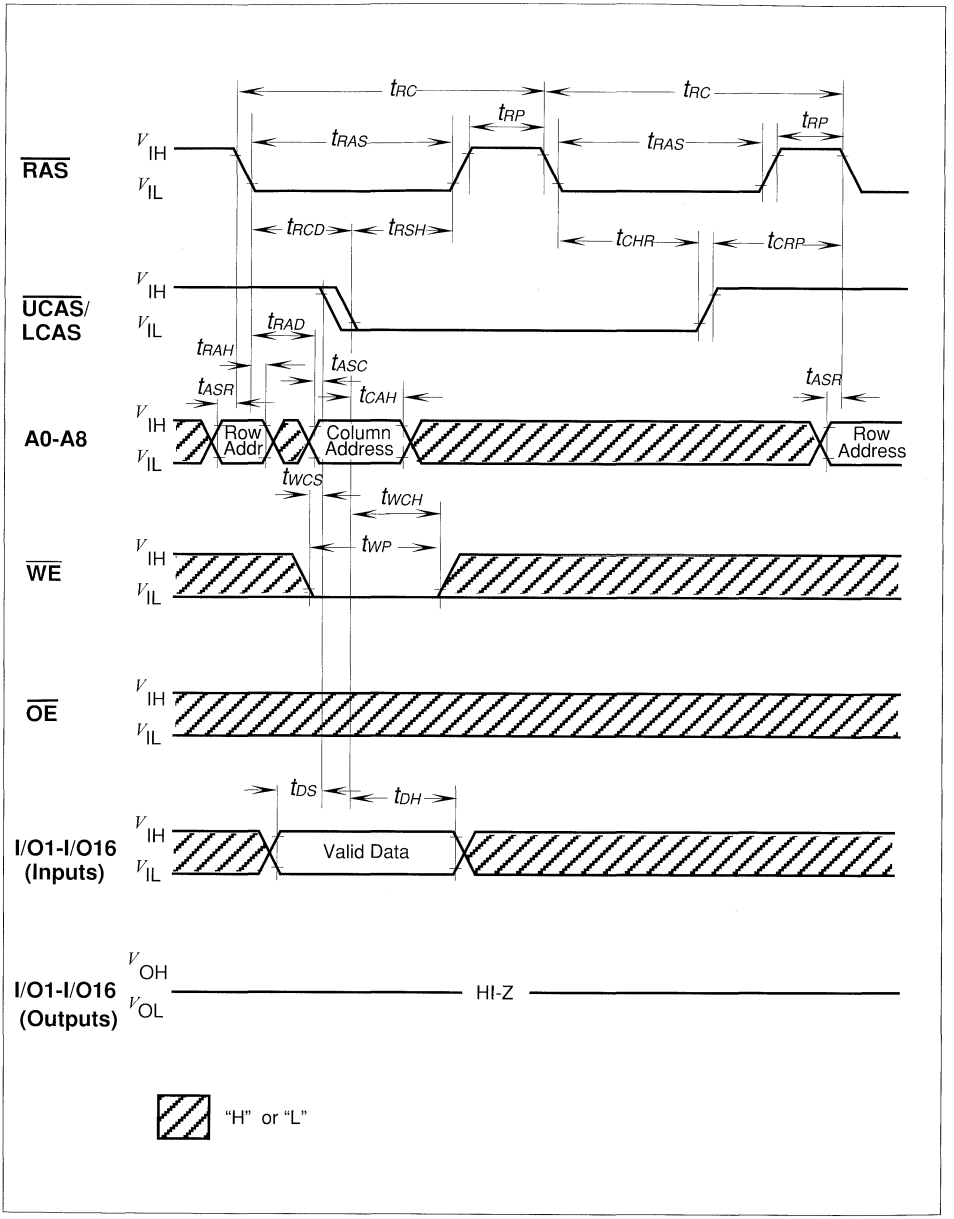
CAS-Before-RAS Refresh Cycle



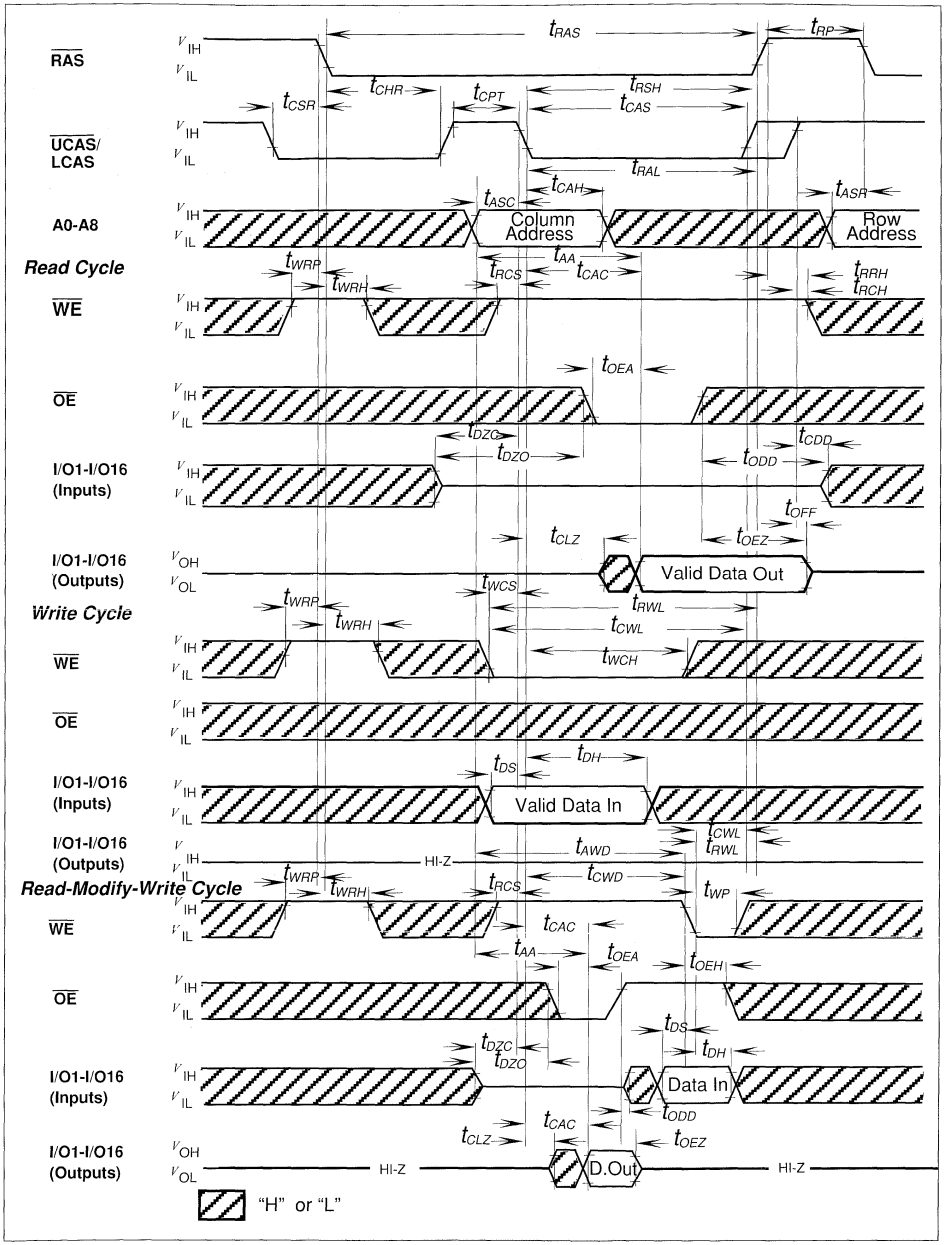
CAS before RAS Self Refresh Cycle



Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Early Write)



CAS/-Before-RAS Refresh Counter Test Cycle

4M x 4-Bit Dynamic RAM

HYB 5116400BJ -50/-60/-70
HYB 5116400BT -50/-60/-70

Advanced Information

- 4 194 304 words by 4-bit organization
- 0 to 70 °C operating temperature
- Fast access and cycle time
  $\overline{RAS}$ access time:
  50 ns (-50 version)
  60 ns (-60 version)
  70 ns (-70 version)
  Cycle time:
  95 ns (-50 version)
  110 ns (-60 version)
  130 ns (-70 version)
  CAS access time:
  15 ns (-50,-60 version)
  20 ns (-70 version)
- Fast page mode cycle time
  35 ns (-50 version)
  40 ns (-60 version)
  45 ns (-70 version)
- Single + 5 V (± 10 %) supply
- Low power dissipation
  max. 550 active mW (-50 version)
  max. 495 active mW (-60 version)
  max. 440 active mW (-70 version)
  11 mW standby (TTL)
  5.5 mW standby (MOS)
- Output unlatched at cycle end allows two-dimensional chip selection
- Read, write, read-modify-write, $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, hidden refresh, Self Refresh and test mode
- Fast page mode capability
- All inputs, outputs and clocks fully TTL-compatible
- 4096 refresh cycles / 64 ms
- Plastic Package: P-SOJ-26/24 300 mil
  P TSOPII-26/24 300 mil

Ordering Information

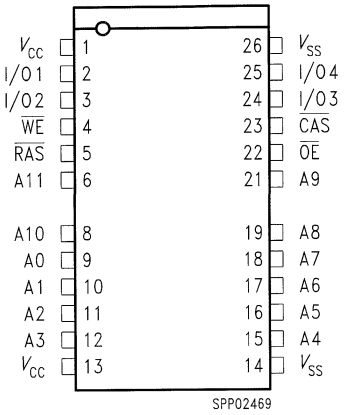
Type	Ordering Code	Package	Descriptions
HYB 5116400BJ-50	Q67100-Q1049	P-SOJ-26/24-1 300 mil	DRAM (access time 50 ns)
HYB 5116400BJ-60	Q67100-Q1050	P-SOJ-26/24-1 300 mil	DRAM (access time 60 ns)
HYB 5116400BJ-70	Q67100-Q1051	P-SOJ-26/24-1 300 mil	DRAM (access time 70 ns)
HYB 5116400BT-50	on request	P-TSOPII-26/24-1 300mil	DRAM (access time 50 ns)
HYB 5116400BT-60	on request	P-TSOPII-26/24-1 300mil	DRAM (access time 60 ns)
HYB 5116400BT-70	on request	P-TSOPII-26/24-1 300mil	DRAM (access time 70 ns)

The HYB 5116400BJ/BT is the new generation dynamic RAM organized as 4194304 words by 4-bits. The HYB 5116400BJ/BT utilizes a submicron CMOS silicon gate process technology, as well as advanced circuit techniques to provide wide operating margins, both internally and for the system user. Multiplexed address inputs permit the HYB 5116400BJ/BT to be packaged in a standard SOJ 26/24 or TSOPII-26/24 plastic package, both with 300 mil width. These packages provide high system bit densities and are compatible with commonly used automatic testing and insertion equipment. System-oriented features include single + 5 V (± 10 %) power supply, direct interfacing with high-performance logic device families such as Schottky TTL.

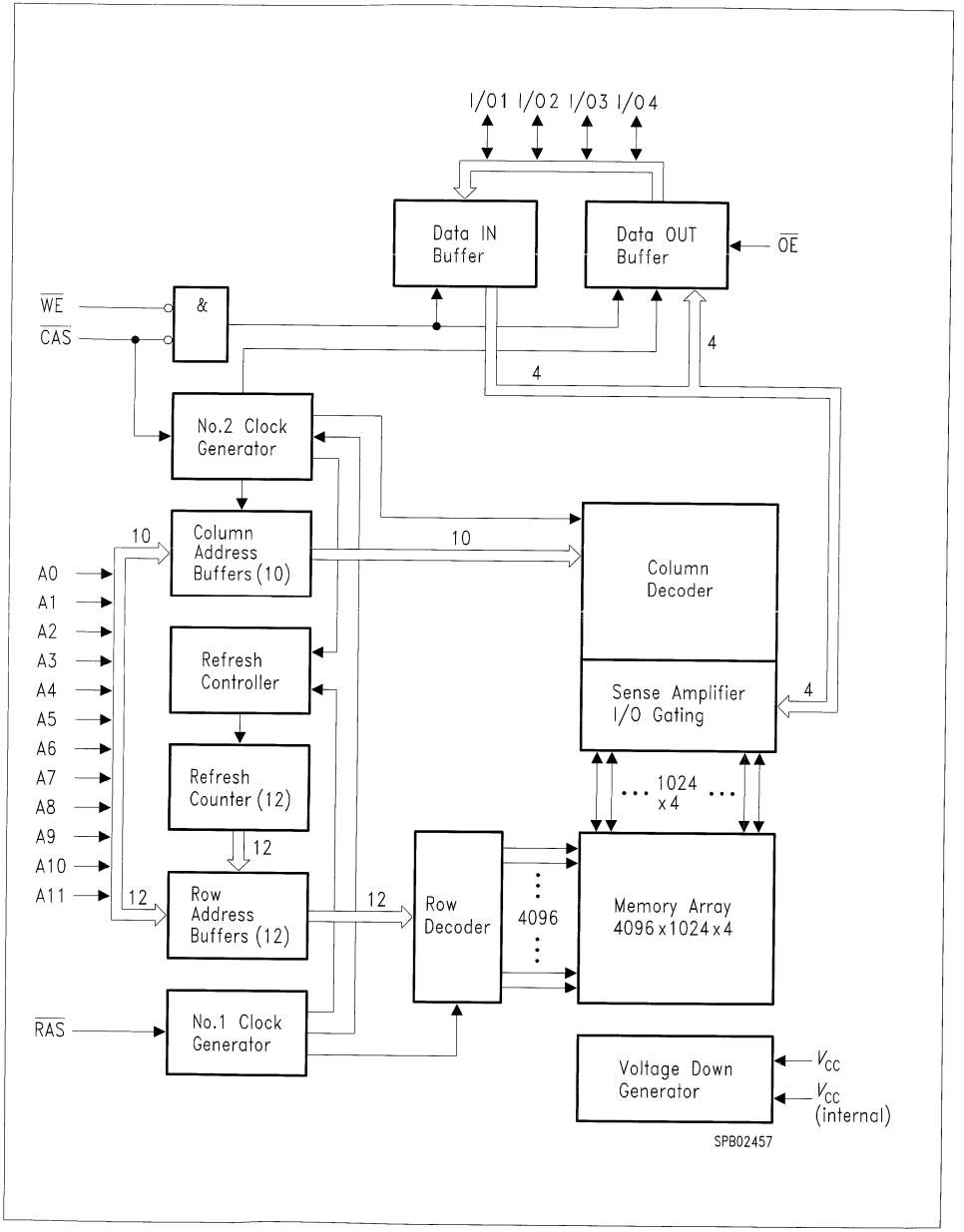
Pin Definitions and Functions

Pin No.	Function
A0-A11	Row Address Inputs
A0-A9	Column Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{OE}$	Output Enable
I/O1-I/O4	Data Input/Output
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground (0 V)
N.C.	not connected

Pin Configuration
(top view)



P-SOJ-26/24 300 mil
P-TSOPII-26/24 300 mil



Block Diagram

Absolute Maximum Ratings

Operating temperature range ..... 0 to 70 °C
Storage temperature range ..... – 55 to 150 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 0.5 to min (V_{CC} + 0.5, 7.0) V
Power supply voltage ..... – 1.0 V to 7.0 V
Power dissipation ..... 1.0 W
Data out current (short circuit) ..... 50 mA

Note:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	V_{CC} + 0.5	V	1)
Input low voltage	V_{IL}	– 0.5	0.8	V	1)
Output high voltage (I_{OUT} = – 5 mA)	V_{OH}	2.4	–	V	1)
Output low voltage (I_{OUT} = 4.2 mA)	V_{OL}	–	0.4	V	1)
Input leakage current (0 V ≤ V_{IH} ≤ V_{CC} + 0.3 V, all other pins = 0 V)	$I_{I(L)}$	– 10	10	µA	1)
Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ V_{CC} + 0.3 V)	$I_{O(L)}$	– 10	10	µA	1)
Average V_{CC} supply current:	I_{CC1}				
-50 ns version		–	100	mA	2) 3) 4)
-60 ns version		–	90	mA	2) 3) 4)
-70 ns version		–	80	mA	2) 3) 4)
($\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = t_{RC} min.)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	2	mA	–
Average V_{CC} supply current, during $\overline{RAS}$-only refresh cycles:	I_{CC3}				
-50 ns version		–	100	mA	2) 4)
-60 ns version		–	90	mA	2) 4)
-70 ns version		–	80	mA	2) 4)
($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)					

DC Characteristics (cont'd)

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current, during fast page mode: -50 ns version -60 ns version -70 ns version ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling: t_{PC} = t_{PC} min.)	I_{CC4}	– – –	85 75 65	mA mA mA	2) 3) 4) 2) 3) 4) 2) 3) 4)
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	–	1	mA	1)
Average V_{CC} supply current, during $\overline{CAS}$-before-RAS refresh mode: -50 ns version -60 ns version -70 ns version ($\overline{RAS}$, $\overline{CAS}$ cycling: t_{RC} = t_{RC} min.)	I_{CC6}	– – –	100 90 80	mA mA mA	2) 4) 2) 4) 2) 4)
Average Self Refresh Current (CBR cycle with t_{RAS} > t_{RASS}min., $\overline{CAS}$ held low, $\overline{WE}$ = V_{CC} – 0.2 V, Address and Din = V_{CC} – 0.2 V or 0.2 V)	I_{CC7}	–	1	mA	

AC Characteristics [5]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		HYB 5116400BJ/ BT-50		HYB 5116400BJ/ BT-60		HYB 5116400BJ/ BT-70		
		min.	max.	min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	95	–	110	–	130	–	ns
Read-write cycle time	t_{RWC}	135	–	150	–	180	–	ns
Fast page mode cycle time	t_{PC}	35	–	40	–	45	–	ns
Fast page mode read-write cycle time	t_{PRWC}	75	–	80	–	95	–	ns
Access time from $\overline{RAS}$ [7) 12)]	t_{RAC}	–	50	–	60	–	70	ns
Access time from $\overline{CAS}$ [7) 12)]	t_{CAC}	–	15	–	15	–	20	ns
Access time from column address [7) 13)]	t_{AA}	–	25	–	30	–	35	ns
Access time from $\overline{CAS}$ precharge [7)]	t_{CPA}	–	30	–	35	–	40	ns
$\overline{CAS}$ to output in low-Z [7)]	t_{CLZ}	0	–	0	–	0	–	ns
Output buffer turn-off delay [8)]	t_{OFF}	0	15	0	15	0	20	ns
Transition time (rise and fall) [6)]	t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	35	–	40	–	50	–	ns
$\overline{RAS}$ pulse width	t_{RAS}	50	10k	60	10k	70	10k	ns
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	50	200k	60	200k	70	200k	ns
$\overline{CAS}$ precharge to $\overline{RAS}$ Delay	t_{RHCP}	30	–	35	–	40	–	ns
$\overline{CAS}$ precharge to $\overline{WE}$ (FPMR RMW)	t_{CPWD}	50	–	55	–	65	–	ns
$\overline{RAS}$ hold time	t_{RSH}	15		15	–	20	–	ns
$\overline{CAS}$ hold time	t_{CSH}	50		60	–	70	–	ns
$\overline{CAS}$ pulse width	t_{CAS}	15	10k	15	10k	20	10k	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time [12)]	t_{RCD}	20	35	20	45	20	50	

AC Characteristics (cont'd) [5]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		HYB 5116400BJ/ BT-50		HYB 5116400BJ/ BT-60		HYB 5116400BJ/ BT-70		
		min.	max.	min.	max.	min.	max.	
$\overline{RAS}$ to column address delay time [13]	t_{RAD}	15	25	15	30	15	35	ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	5	–	ns
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns
Row address hold time	t_{RAH}	10	–	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns
Column address hold time	t_{CAH}	10	–	15	–	15	–	ns
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	–	30	–	35	–	ns
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns
Read command hold time [9]	t_{RCH}	0	–	0	–	0	–	ns
Read command hold time referenced to $\overline{RAS}$ [9]	t_{RRH}	0	–	0	–	0	–	ns
Write command hold time	t_{WCH}	10	–	15	–	15	–	ns
Write command pulse width	t_{WP}	10	–	15	–	15	–	ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	–	15	–	20	–	ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	–	15	–	20	–	ns
Data setup time [10]	t_{DS}	0	–	0	–	0	–	ns
Data hold time [10]	t_{DH}	10	–	15	–	15	–	ns
Refresh period	t_{REF}	–	64	–	64	–	64	ms
Write command setup time [11]	t_{WCS}	0	–	0	–	0	–	ns
$\overline{CAS}$ to $\overline{WE}$ delay time [11]	t_{CWD}	35	–	35	–	45	–	ns
$\overline{RAS}$ to WE delay time [11]	t_{RWD}	70	–	80	–	95	–	ns
Column address to $\overline{WE}$ delay time [11]	t_{AWD}	45	–	50	–	60	–	ns
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CSR}	10	–	10	–	10	–	ns

AC Characteristics (cont'd) [5]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		HYB 5116400BJ/ BT-50		HYB 5116400BJ/ BT-60		HYB 5116400BJ/ BT-70		
		min.	max.	min.	max.	min.	max.	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CHR}	10	–	10	–	10	–	ns
$\overline{CAS}$ hold time (Test mode entry cycle)	t_{CHRT}	30	–	30	–	30	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5	–	5	–	5	–	ns
$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ counter test cycle)	t_{CPT}	35	–	40	–	40	–	ns
Write command setup time (in test mode entry cycle)	t_{WTS}	10	–	10	–	10	–	ns
Write command hold time (in test mode entry cycle)	t_{WTH}	10	–	10	–	10	–	ns
Write to $\overline{RAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{WRP}	10	–	10	–	10	–	ns
Write hold time referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{WRH}	10	–	10	–	10	–	ns
$\overline{OE}$ command hold time	t_{OEH}	15	–	15	–	20	–	ns
$\overline{OE}$ access time	t_{OEA}	–	15	–	15	–	20	ns
Output buffer turn-off delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	ns
Data to $\overline{CAS}$ low delay [15]	t_{DZC}	0	–	0	–	0	–	ns
Data to $\overline{OE}$ low delay [15]	t_{DZO}	0	–	0	–	0	–	ns
$\overline{CAS}$ high to data delay [16]	t_{CDD}	15	–	15	–	20	–	ns
$\overline{OE}$ high to data delay [16]	t_{ODD}	15	–	15	–	20	–	ns
$\overline{RAS}$ pulse width during self refresh	t_{RASS}	100k	–	100k	–	100k	–	ns
$\overline{RAS}$ precharge time during self refresh	t_{RPS}	95	–	110	–	130	–	ns
$\overline{CAS}$ hold time during self refresh	t_{CHS}	– 50	–	– 50	–	– 50	–	ns

Capacitance

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A11)	C_{I1}	–	5	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}	–	7	pF
I/O capacitance (I/O1-I/O4)	C_{IO}	–	7	pF

Notes:

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.

4) Address can be changed once or less while $\overline{RAS} = V_{IL}$. In the case of I_{CC4} it can be changed once or less during a fast page mode cycle (t_{PC}).

5) An initial pause of 200 µs is required after power-up followed by 8 RAS cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS cycles are required.

6) $V_{IH\ (min.)}$ and $V_{IL\ (max.)}$ are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.

7) Measured with a load equivalent to 2 TTL loads and 100 pF.

8) $t_{OFF\ (max.)}$ and $t_{OEZ\ (max.)}$ define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.

9) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

10) These parameters are referenced to the CAS leading edge in early write cycles and to the WE leading edge in read-write cycles.

11) t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS\ (min.)}$, the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} > t_{RWD\ (min.)}$, $t_{CWD} > t_{CWD\ (min.)}$, $t_{AWD} > t_{AWD\ (min.)}$ and $t_{CPWD} > t_{CPWD\ (min.)}$, the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.

12) Operation within the $t_{RCD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RCD\ (max.)}$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD\ (max.)}$ limit, then access time is controlled by t_{CAC}.

13) Operation within the $t_{RAD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RAD\ (max.)}$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD\ (max.)}$ limit, then access time is controlled by t_{AA}.

14) AC measurements assume t_T = 5 ns.

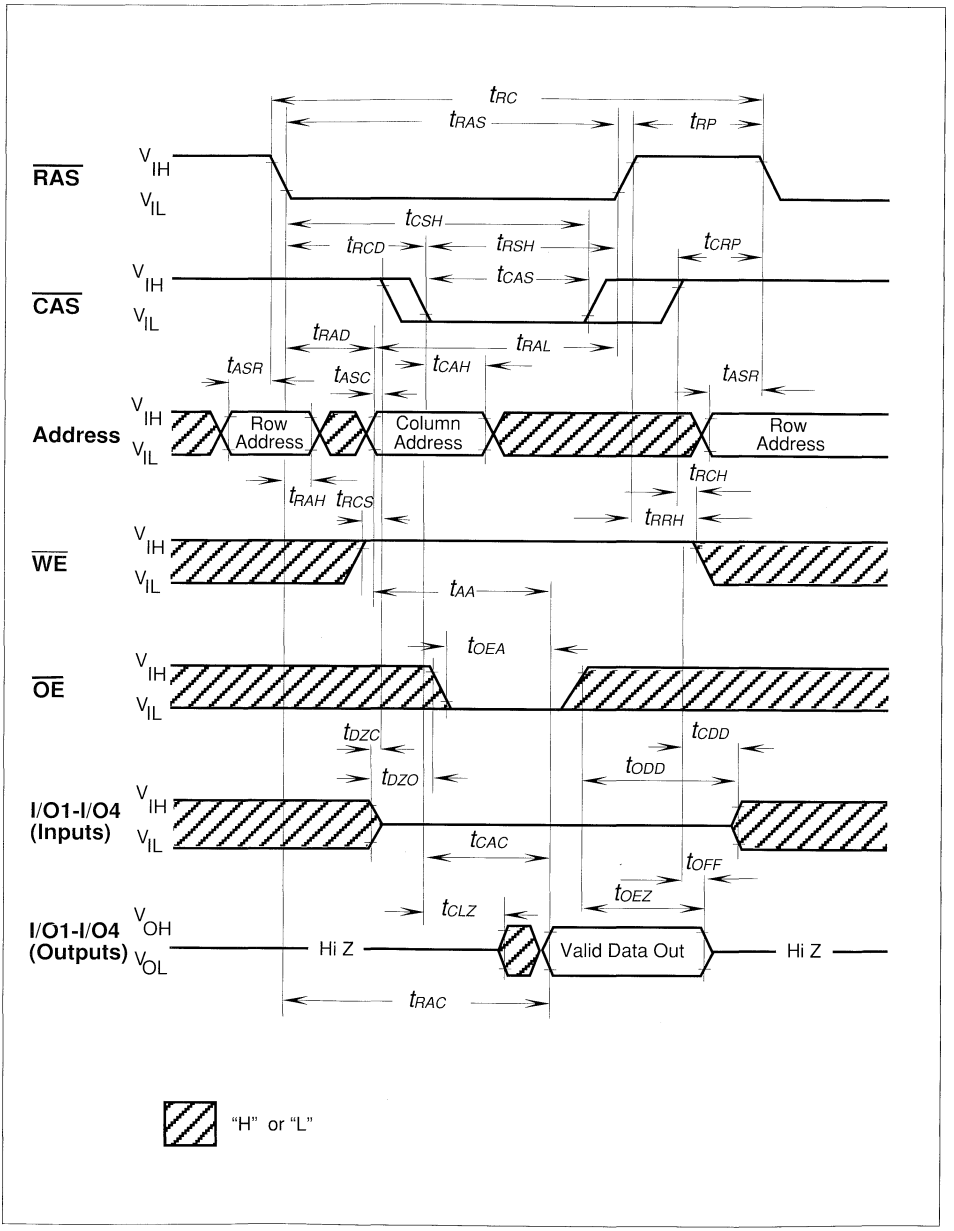
15) Either t_{DZC} or t_{DZO} must be satisfied.

16) Either t_{CDD} or t_{ODD} must be satisfied.

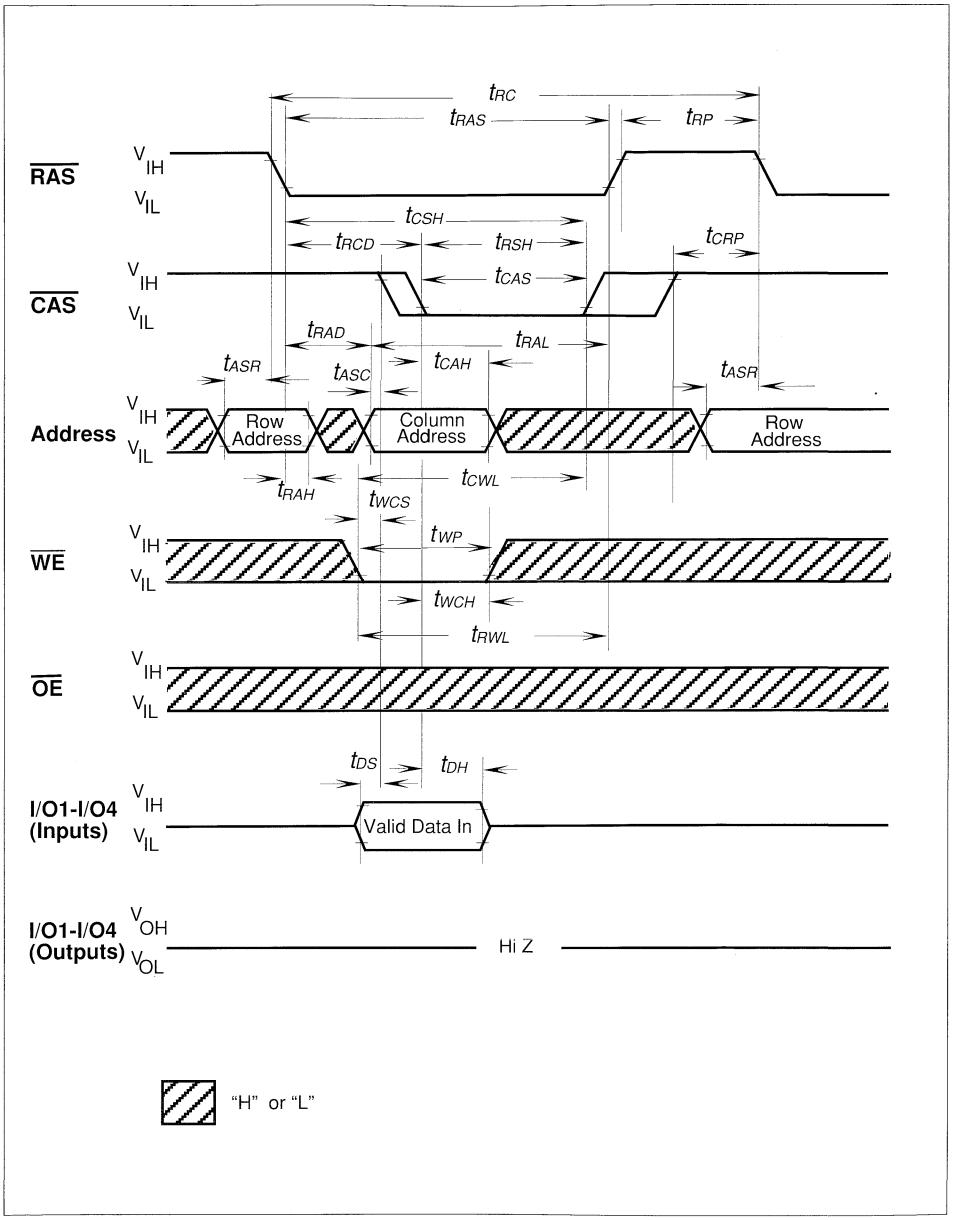
17) When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:

    If row addresses are being refreshed on an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh.

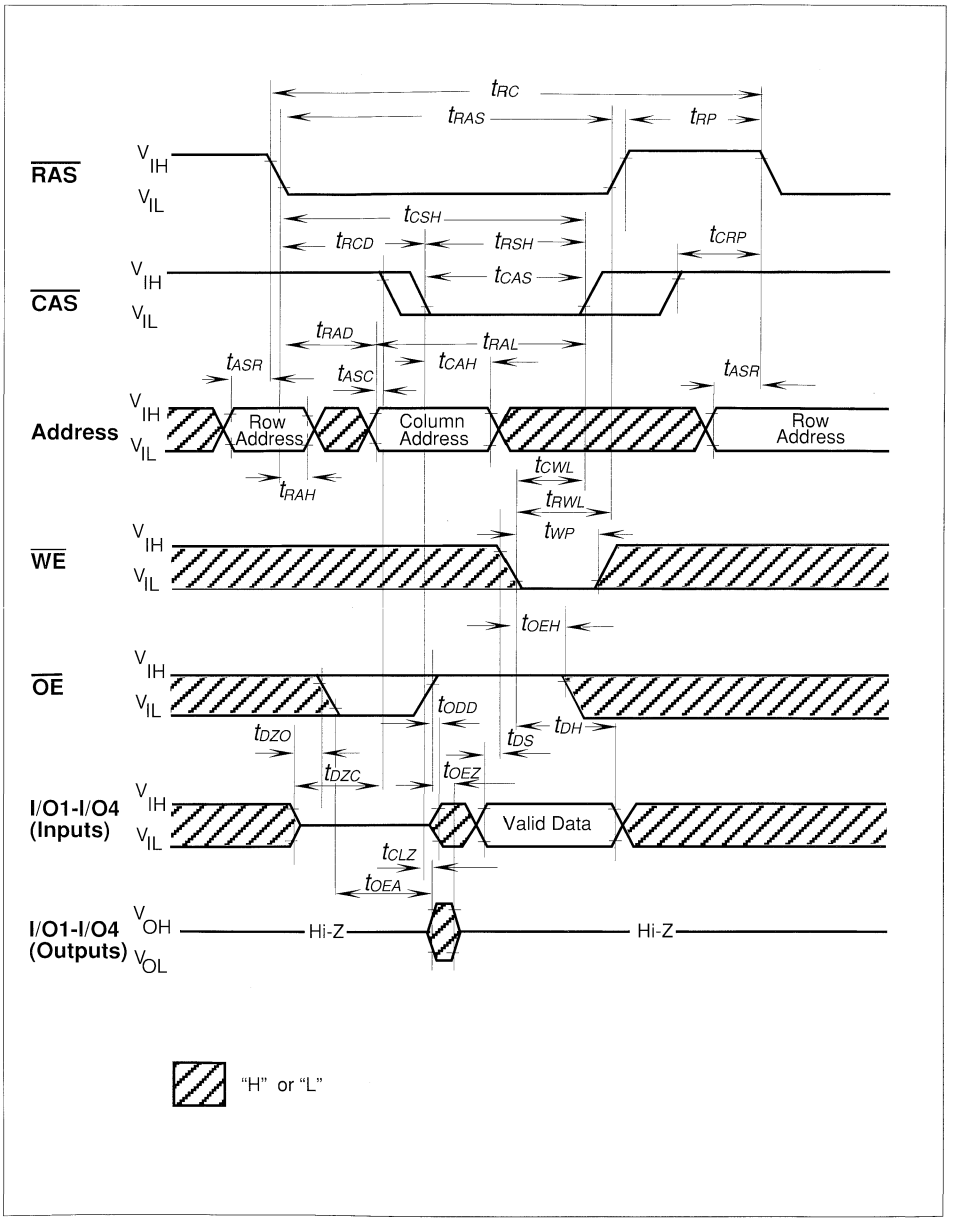
    If row addresses are being refreshed in any other manner (ROR - Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh.


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tASR
tASC
tCAH
tASR
Address
Row Address
Column Address
Row Address
tRCH
tRAH
tRCS
tRRH
WE
tAA
tOEA
OE
tDZC
tCDD
tDZO
tODD
I/O1-I/O4 (Inputs)
tCAC
tOFF
tOEZ
tCLZ
I/O1-I/O4 (Outputs)
VOH
VOL
Hi Z
Valid Data Out
Hi Z
tRAC
"H" or "L"

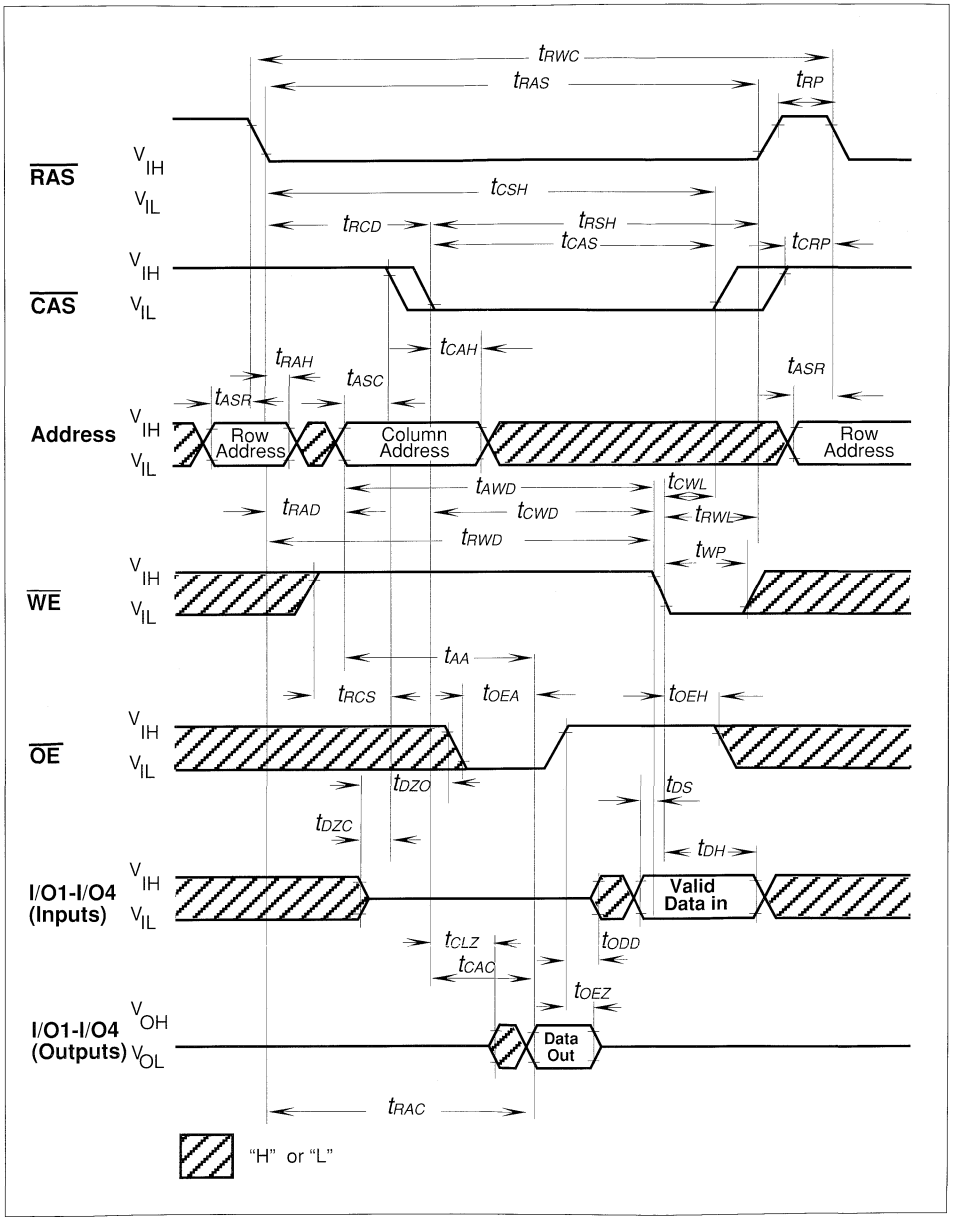
Read Cycle



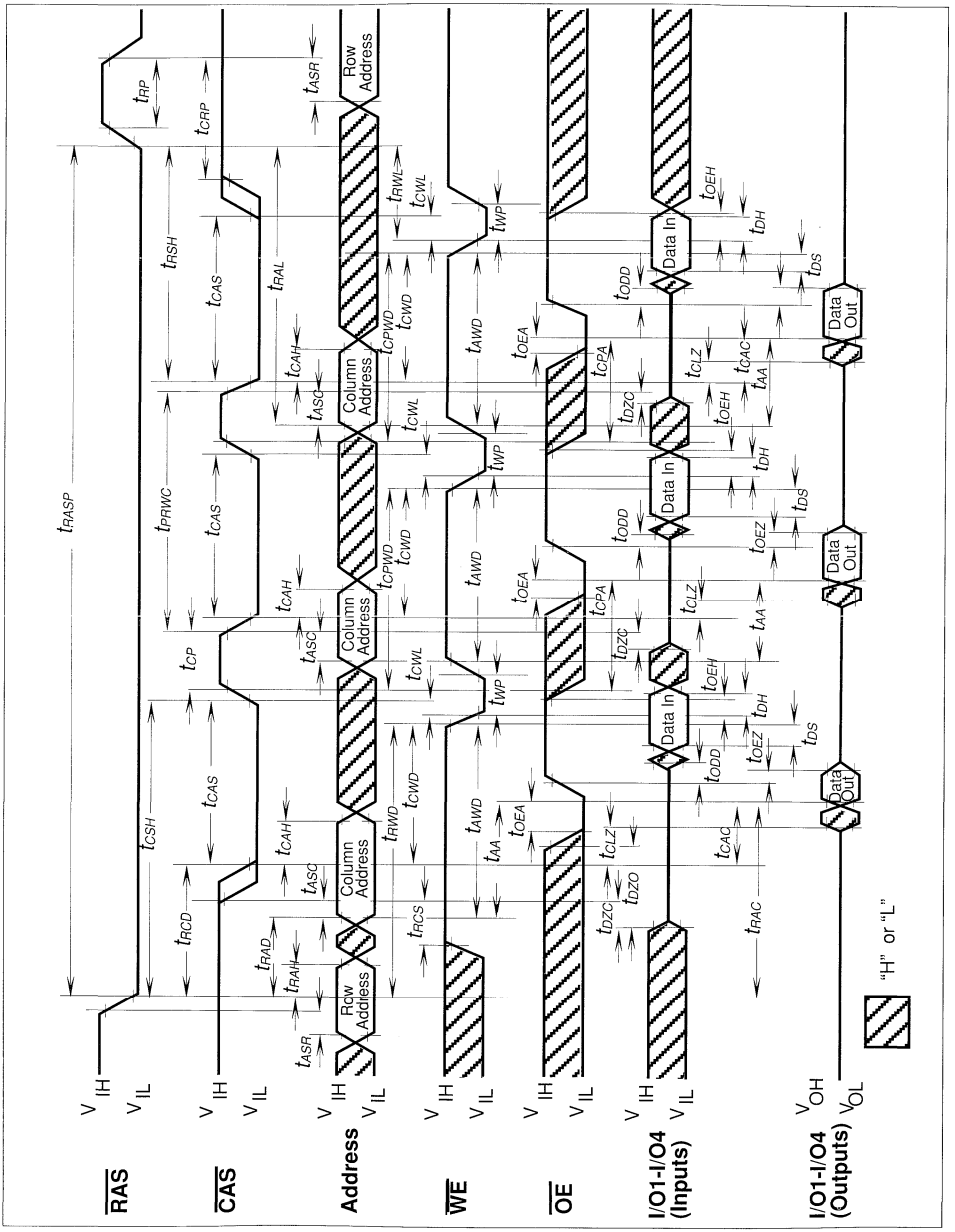
Write Cycle (Early Write)



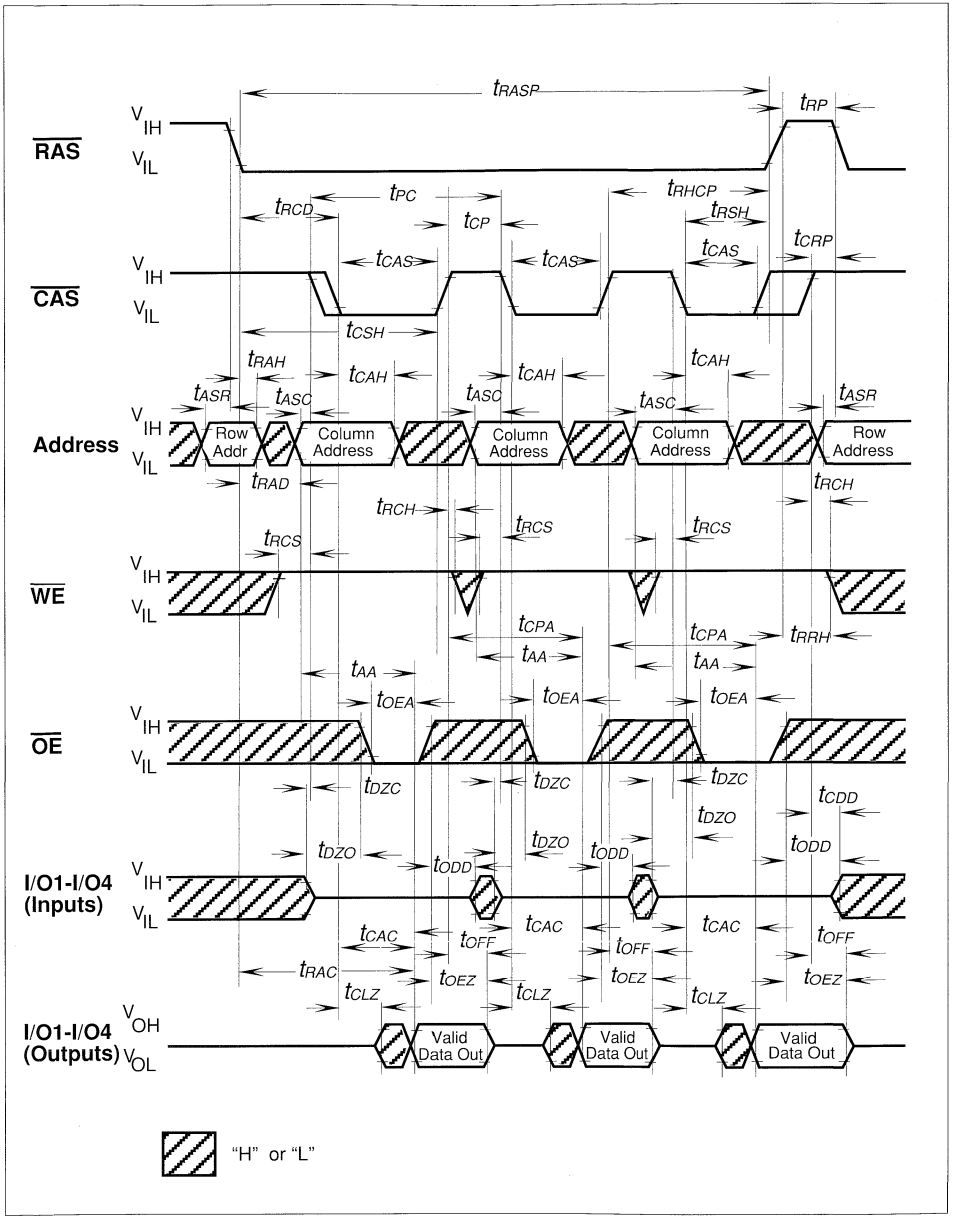
Write Cycle ($\overline{OE}$ Controlled Write)



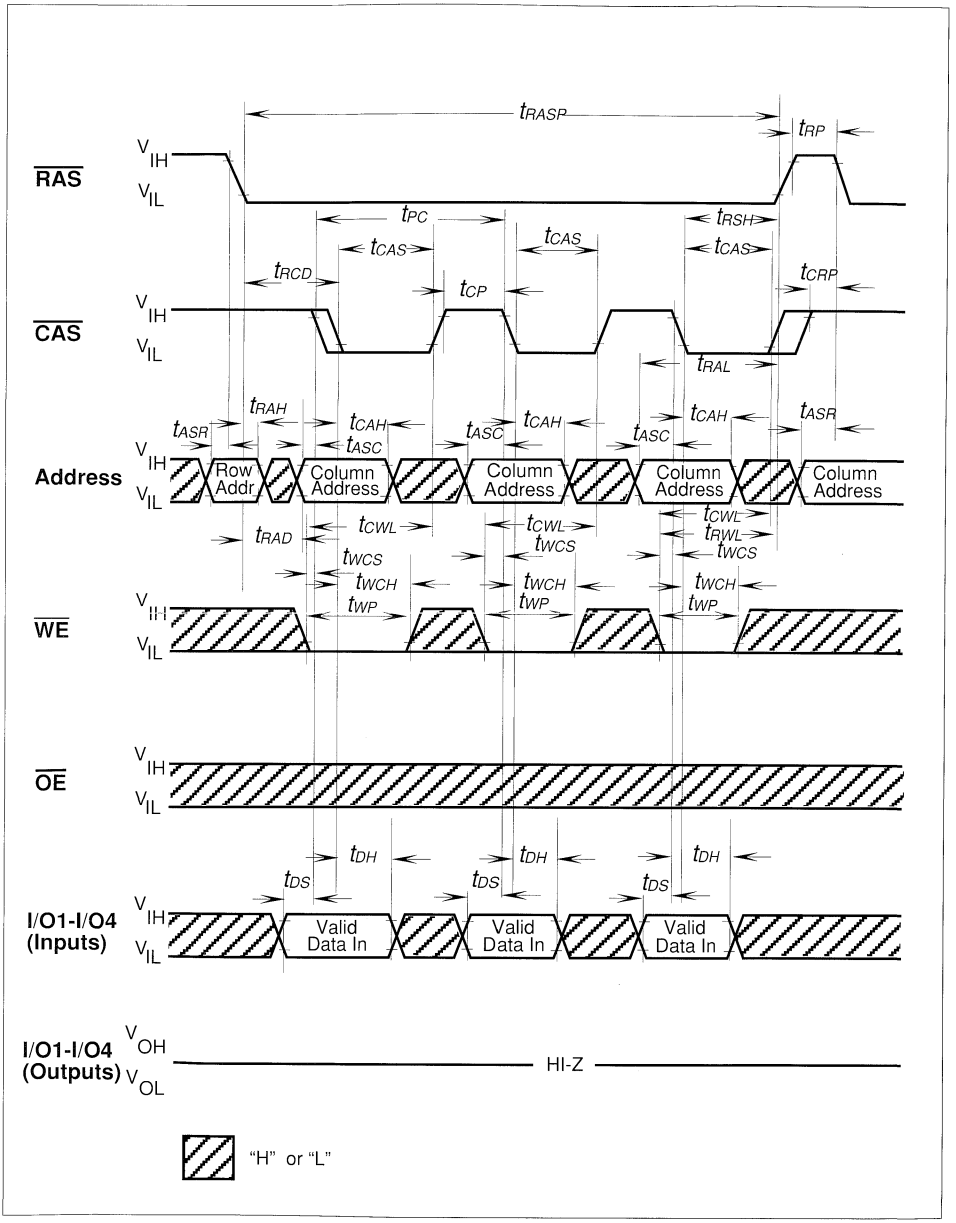
Read-Write (Read-Modify-Write) Cycle



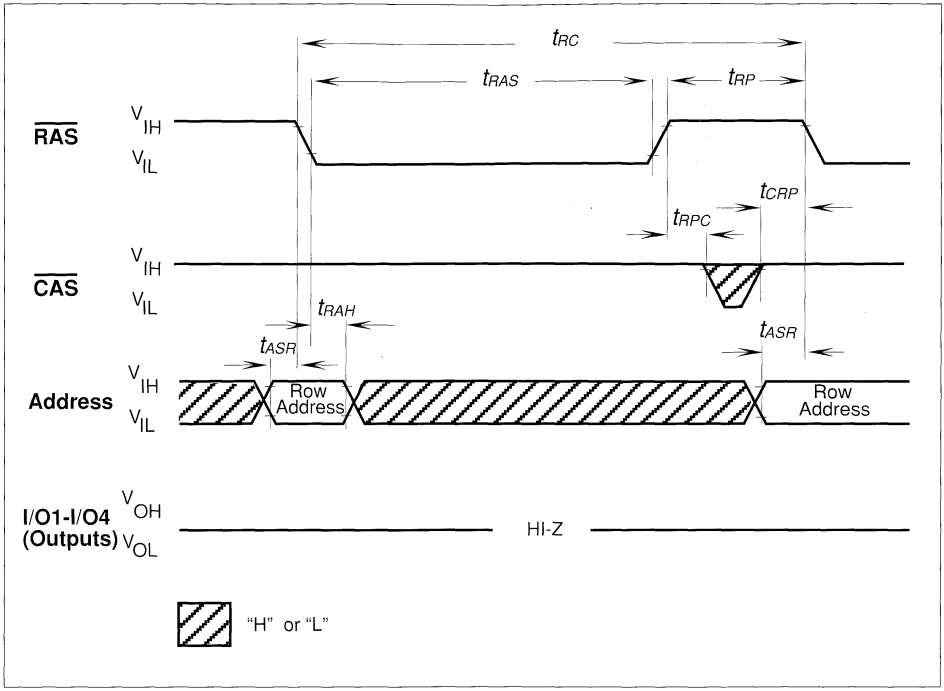
Fast Page Mode Read-Modify-Write Cycle



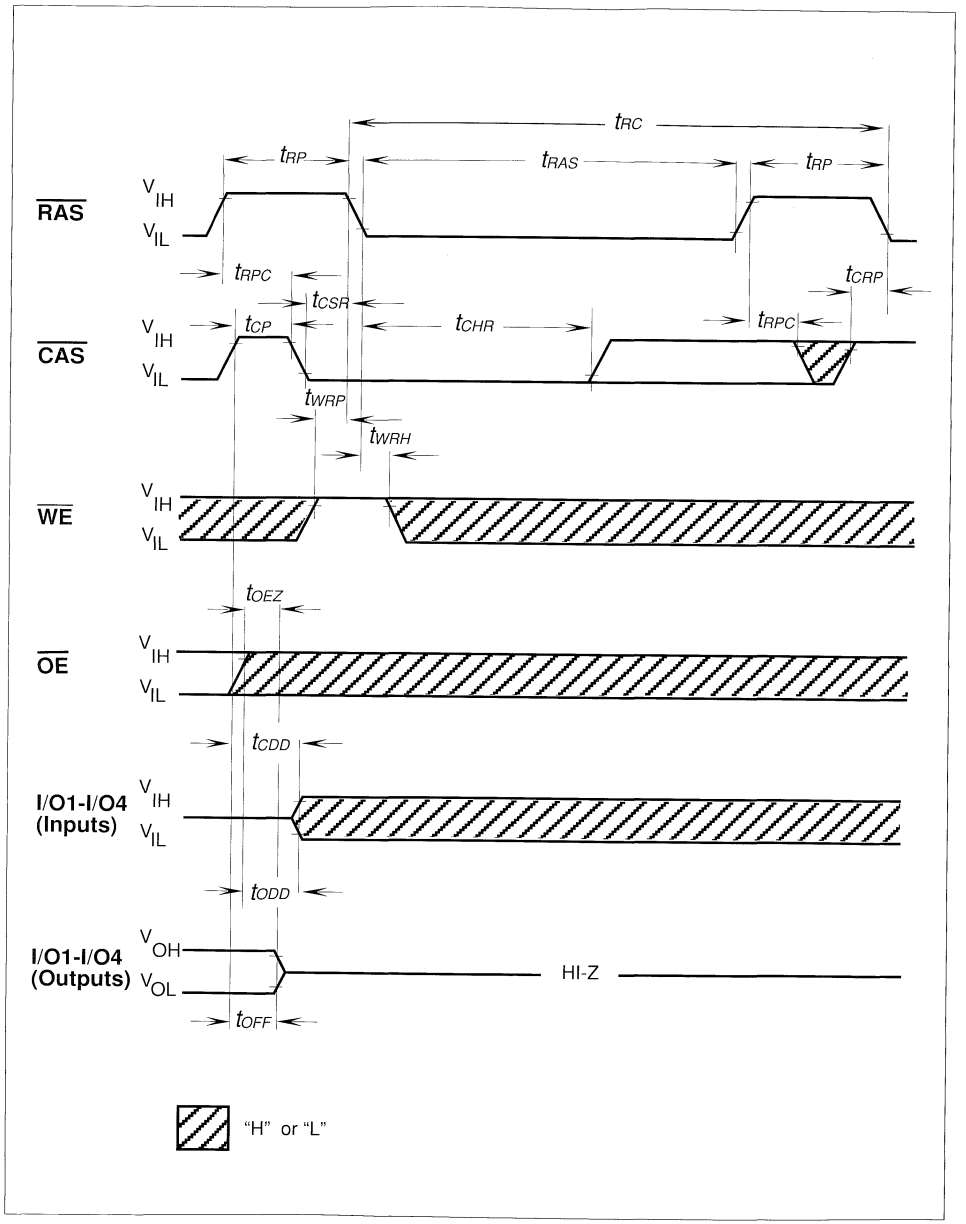
Fast Page Mode Read Cycle



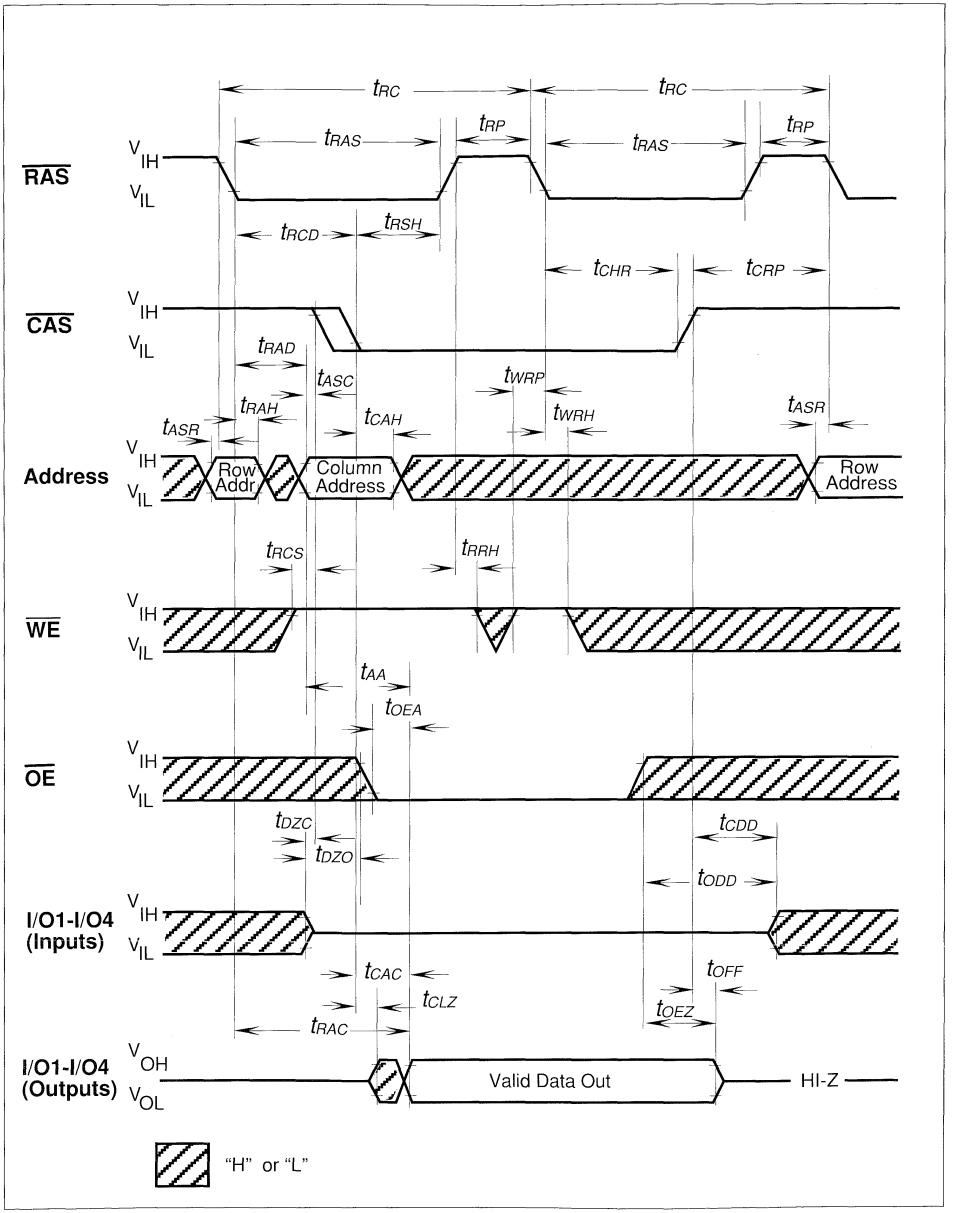
Fast Page Mode Early Write Cycle



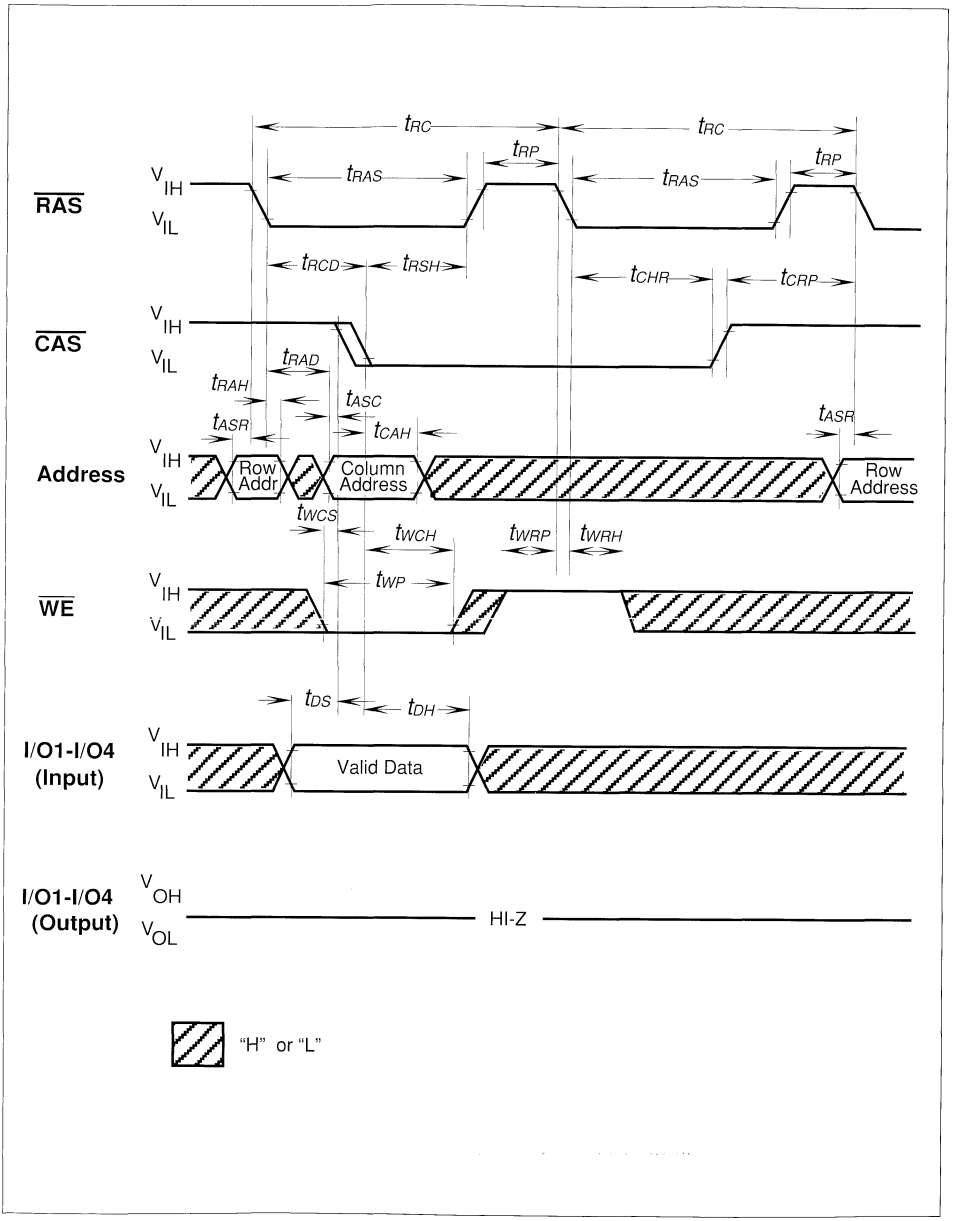
RAS-Only Refresh Cycle



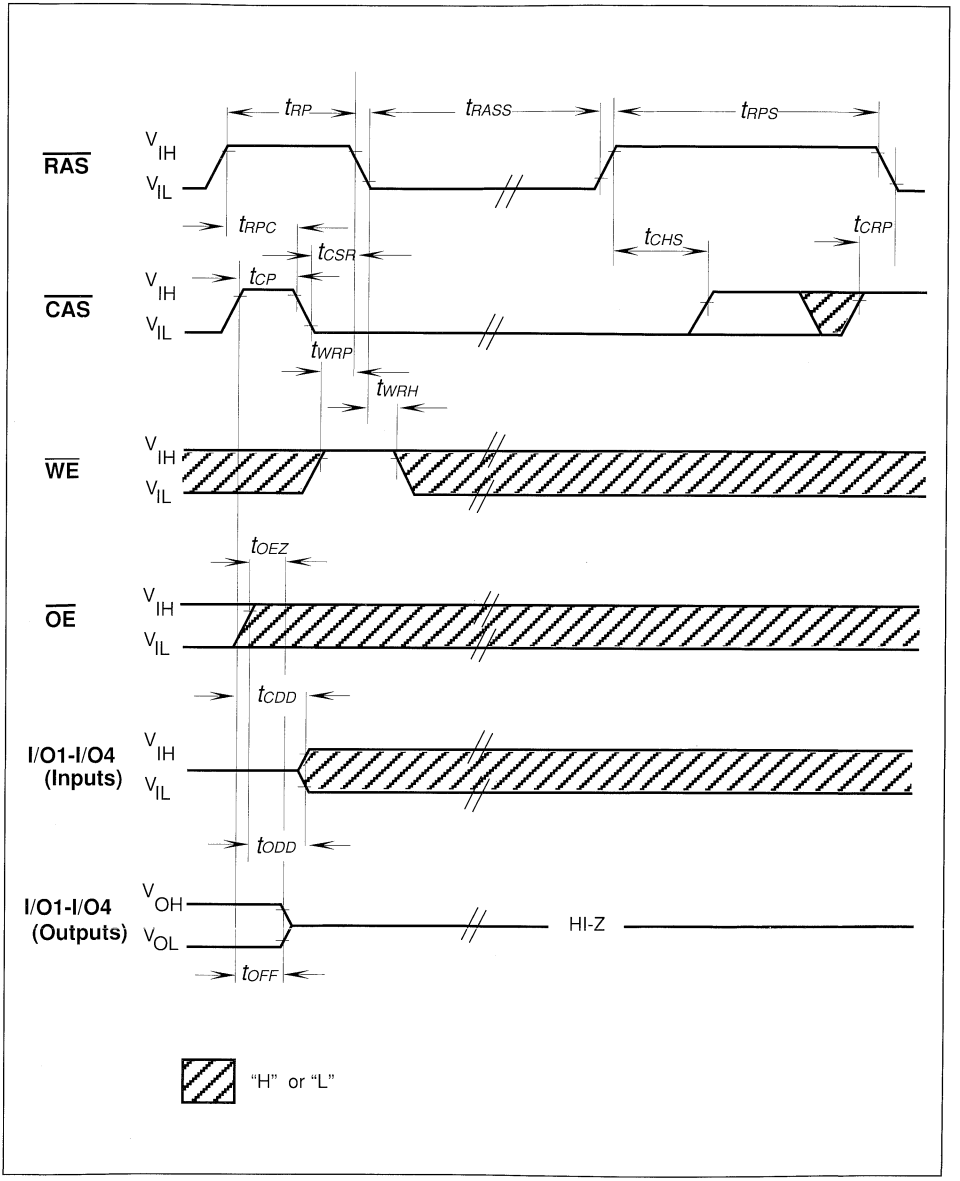
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



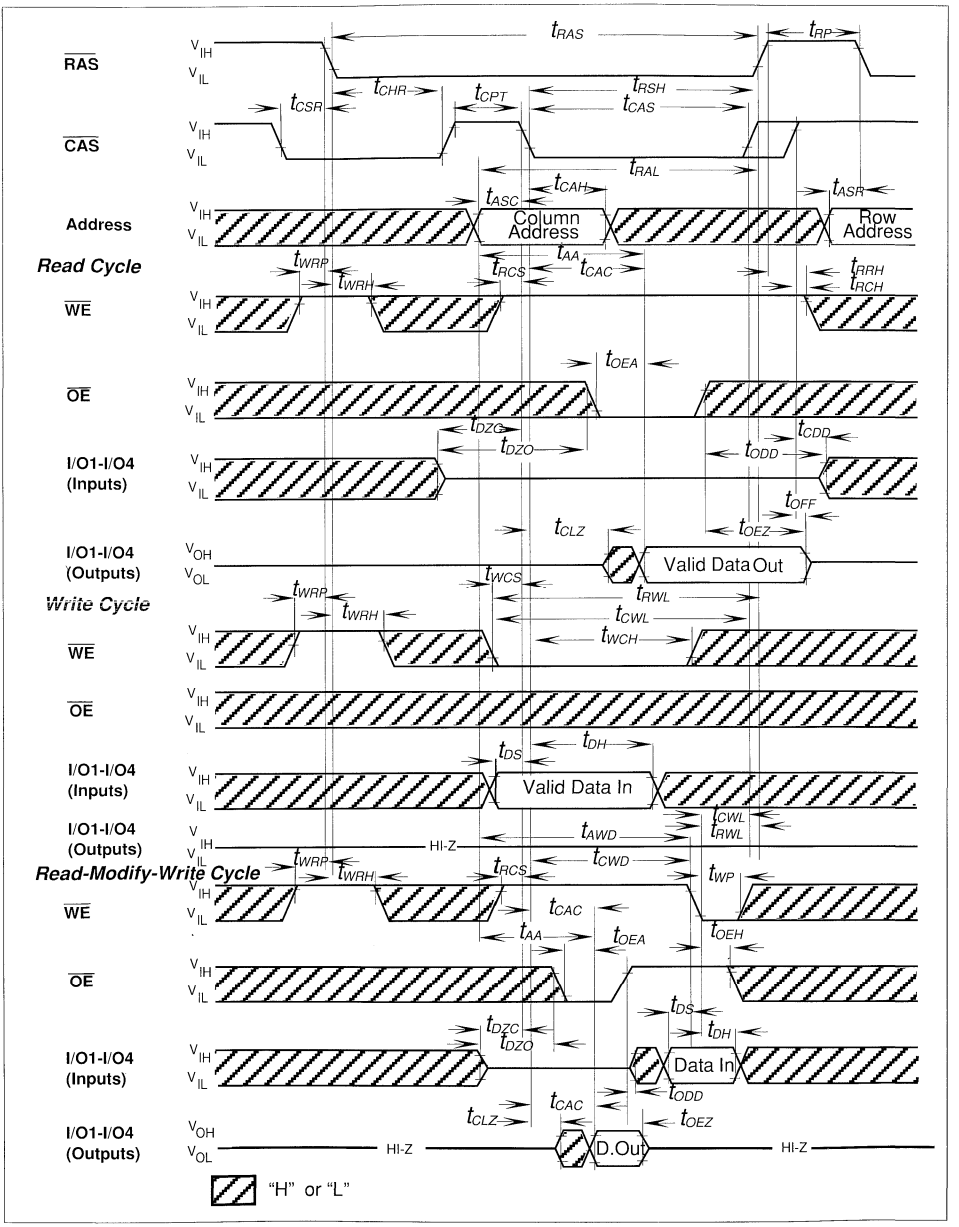
Hidden Refresh Cycle (Read)



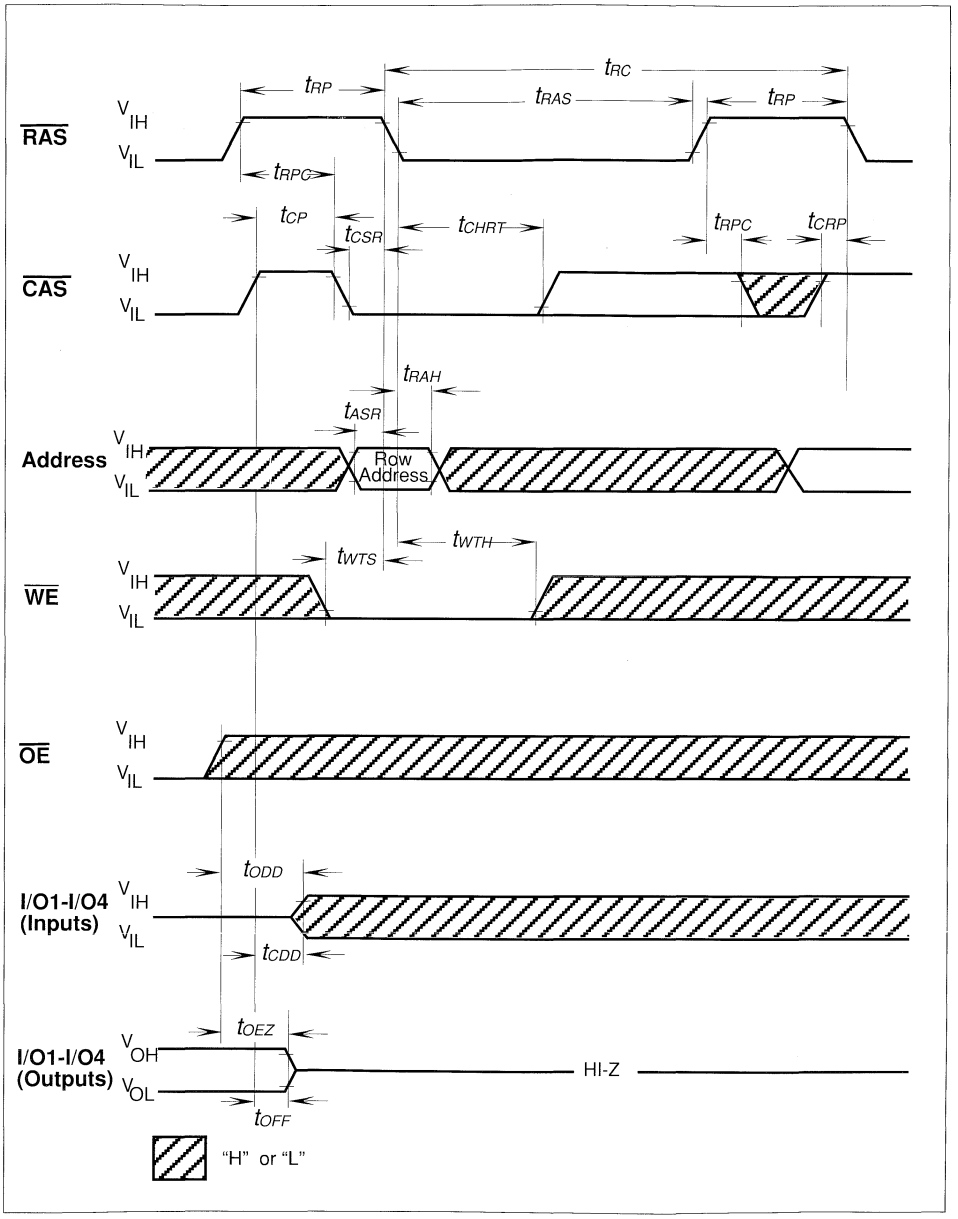
Hidden Refresh Cycle (Early Write)



$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Self Refresh



CAS-Before-RAS Refresh Counter Test Cycle



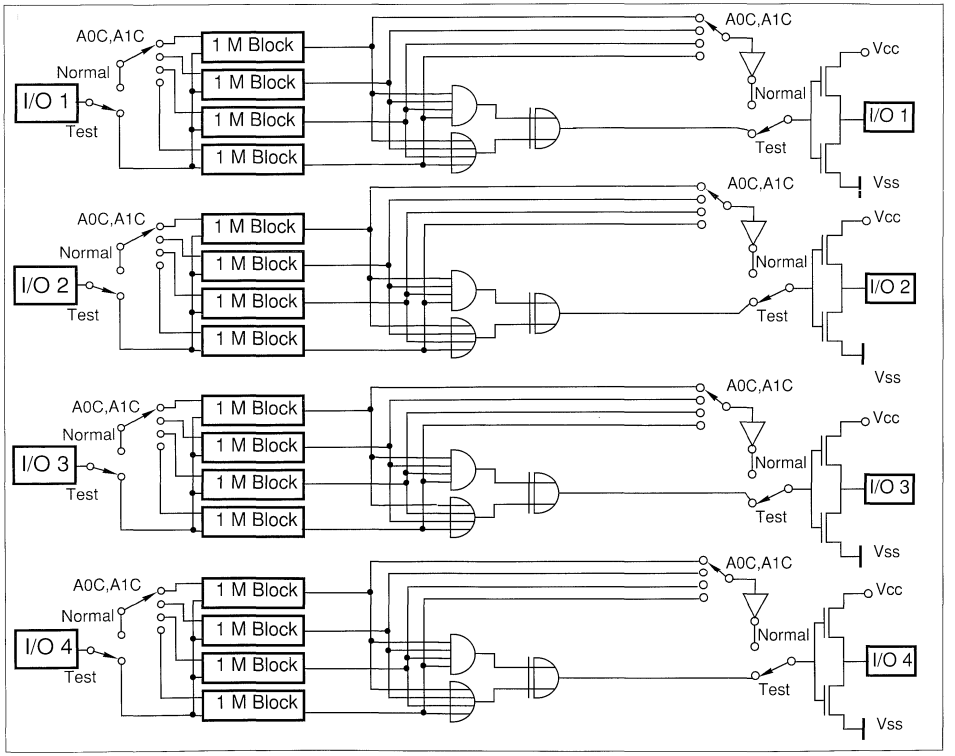
Test Mode Entry

Test Mode

As the HYB 5116400BJ/BT is organized internally as 1M x 16-bits, a test mode cycle using 4:1 compression can be used to improve test time. Note that in the 4M x 4 version the test time is reduced by 1/4 for a N test pattern.

In a test mode "write" the data from each I/O pin is written into four 1M blocks simultaneously (all "1" s or all "0" s). In test mode "read" each I/O output is used for indicating the test mode result. If the internal four bits are equal, the I/O would indicate a "1". If they were not equal, the I/O would indicate a "0". The WCBR cycle ($\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$) puts the device into test mode. To exit from test mode, a "$\overline{CAS}$ before $\overline{RAS}$ refresh", "$\overline{RAS}$ only refresh" or "Hidden refresh" can be used.Refresh during test mode operation can be performed by normal read cylces or by WCBR refresh cycles.

Row addresses A0 through A9 have to kept high to perform a testmode entry cylce. All other addresses are don't care.



Block Diagram in Test Mode

4M x 4-Bit Dynamic RAM

HYB 5117400BJ -50/-60/-70
HYB 5117400BT -50/-60/-70

Advanced Information

- 4 194 304 words by 4-bit organization
- 0 to 70 °C operating temperature
- Fast access and cycle time
  RAS access time:
  50 ns (-50 version)
  60 ns (-60 version)
  70 ns (-70 version)
  Cycle time:
  95 ns (-50 version)
  110 ns (-60 version)
  130 ns (-70 version)
  CAS access time:
  15 ns (-50,-60 version)
  20 ns (-70 version)
- Fast page mode cycle time
  35 ns (-50 version)
  40 ns (-60 version)
  45 ns (-70 version)
- Single + 5 V (± 10 %) supply
- Low power dissipation
  max. 660 active mW (-50 version)
  max. 605 active mW (-60 version)
  max. 550 active mW (-70 version)
  11 mW standby (TTL)
  5.5 mW standby (MOS)
- Output unlatched at cycle end allows two-dimensional chip selection
- Read, write, read-modify-write, CAS-before-RAS refresh, RAS-only refresh, hidden refresh, Self Refresh and test mode
- Fast page mode capability
- All inputs, outputs and clocks fully TTL-compatible
- 2048 refresh cycles / 32 ms
- Plastic Package: P-SOJ-26/24 300 mil
  P TSOPII-26/24 300 mil

Ordering Information

Type	Ordering Code	Package	Descriptions
HYB 5117400BJ-50	Q67100-Q1086	P-SOJ-26/24-1 300 mil	DRAM (access time 50 ns)
HYB 5117400BJ-60	Q67100-Q1087	P-SOJ-26/24-1 300 mil	DRAM (access time 60 ns)
HYB 5117400BJ-70	Q67100-Q1088	P-SOJ-26/24-1 300 mil	DRAM (access time 70 ns)
HYB 5117400BT-50	on request	P-TSOPII-26/24-1 300mil	DRAM (access time 50 ns)
HYB 5117400BT-60	on request	P-TSOPII-26/24-1 300mil	DRAM (access time 60 ns)
HYB 5117400BT-70	on request	P-TSOPII-26/24-1 300mil	DRAM (access time 70 ns)

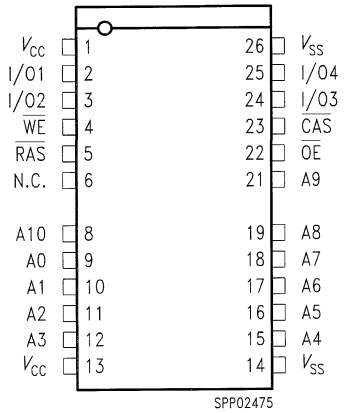
The HYB 5117400BJ/BT is the new generation dynamic RAM organized as 4194304 words by 4-bits. The HYB 5117400BJ/BT utilizes a submicron CMOS silicon gate process technology, as well as advanced circuit techniques to provide wide operating margins, both internally and for the system user. Multiplexed address inputs permit the HYB 5117400BJ/BT to be packaged in a standard SOJ 26/24 or TSOPII-26/24 plastic package, both with 300 mil width. These packages provide high system bit densities and are compatible with commonly used automatic testing and insertion equipment. System-oriented features include single + 5 V (± 10 %) power supply, direct interfacing with high-performance logic device families such as Schottky TTL.

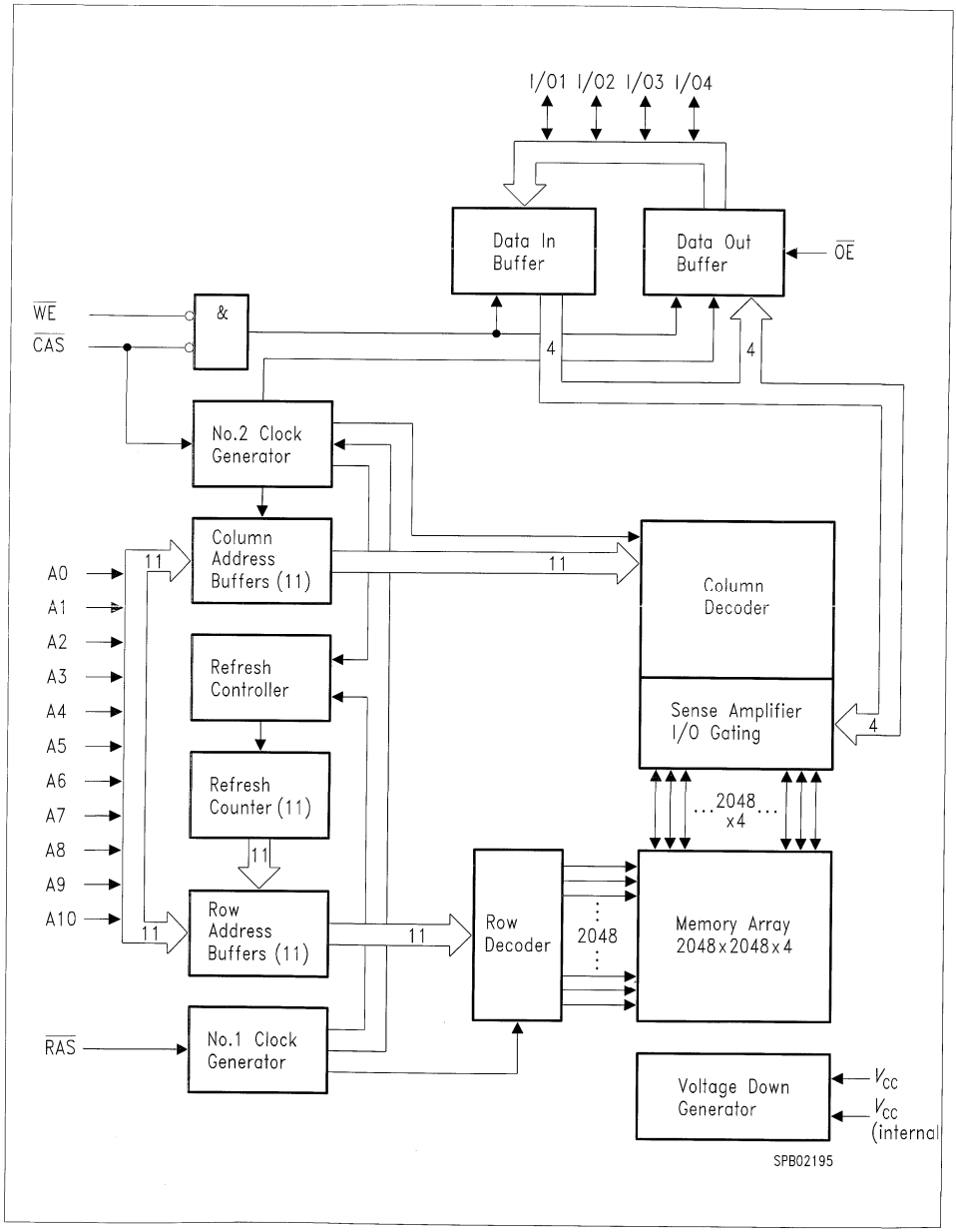
Pin Definitions and Functions

Pin No.	Function
A0 to A10	Row Address Inputs
A0 to A10	Column Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{OE}$	Output Enable
I/O1-I/O4	Data Input/Output
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground (0 V)
N.C.	not connected

Pin Configuration
(top view)

P-SOJ-26/24 300 mil
P-TSOPII-26/24 300mil





Block Diagram

Absolute Maximum Ratings

Operating temperature range ..... 0 to 70 °C
Storage temperature range ..... – 55 to 150 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 0.5 to min (V_{CC} + 0.5, 7.0) V
Power supply voltage ..... – 1.0 V to 7.0 V
Power dissipation ..... 1.0 W
Data out current (short circuit) ..... 50 mA

Note:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	V_{CC}+0.5	V	1)
Input low voltage	V_{IL}	– 0.5	0.8	V	1)
Output high voltage (I_{OUT} = – 5 mA)	V_{OH}	2.4	–	V	1)
Output low voltage (I_{OUT} = 4.2 mA)	V_{OL}	–	0.4	V	1)
Input leakage current (0 V ≤ V_{IH} ≤ V_{CC} + 0.3 V, all other pins = 0 V)	$I_{I(L)}$	– 10	10	µA	1)
Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ V_{CC} + 0.3 V)	$I_{O(L)}$	– 10	10	µA	1)
Average V_{CC} supply current:	I_{CC1}				
-50 ns version		–	120	mA	2) 3) 4)
-60 ns version		–	110	mA	2) 3) 4)
-70 ns version		–	100	mA	2) 3) 4)
(RAS, CAS, address cycling: t_{RC} = t_{RC} min.)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	2	mA	–
Average V_{CC} supply current, during $\overline{RAS}$-only refresh cycles:	I_{CC3}				
-50 ns version		–	120	mA	2) 4)
-60 ns version		–	110	mA	2) 4)
-70 ns version		–	100	mA	2) 4)
($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)					

DC Characteristics (cont'd)

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current, during fast page mode: -50 ns version -60 ns version -70 ns version ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling: t_{PC} = t_{PC} min.)	I_{CC4}	– – –	90 80 70	mA mA mA	2) 3) 4) 2) 3) 4) 2) 3) 4)
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	–	1	mA	1)
Average V_{CC} supply current, during $\overline{CAS}$-before-RAS refresh mode: -50 ns version -60 ns version -70 ns version ($\overline{RAS}$, $\overline{CAS}$ cycling: t_{RC} = t_{RC} min.)	I_{CC6}	– – –	120 110 100	mA mA mA	2) 4) 2) 4) 2) 4)
Average Self Refresh Current ($\overline{CBR}$ cycle with t_{RAS} > t_{RASS} min., $\overline{CAS}$ held low, $\overline{WE}$ = V_{CC} - 0.2 V, Address and Din = V_{CC} - 0.2 V or 0.2 V)	I_{CC7}	–	1	mA	

AC Characteristics [5]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		HYB 5117400BJ/ BT-50		HYB 5117400BJ/ BT-60		HYB 5117400BJ/ BT-70		
		min.	max.	min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	95	–	110	–	130	–	ns
Read-write cycle time	t_{RWC}	135	–	150	–	180	–	ns
Fast page mode cycle time	t_{PC}	35	–	40	–	45	–	ns
Fast page mode read-write cycle time	t_{PRWC}	75	–	80	–	95	–	ns
Access time from $\overline{RAS}$ [7) 12)]	t_{RAC}	–	50	–	60	–	70	ns
Access time from $\overline{CAS}$ [7) 12)]	t_{CAC}	–	15	–	15	–	20	ns
Access time from column address [7) 13)]	t_{AA}	–	25	–	30	–	35	ns
Access time from $\overline{CAS}$ precharge [7)]	t_{CPA}	–	30	–	35	–	40	ns
$\overline{CAS}$ to output in low-Z [7)]	t_{CLZ}	0	–	0	–	0	–	ns
Output buffer turn-off delay [8)]	t_{OFF}	0	15	0	15	0	20	ns
Transition time (rise and fall) [6)]	t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	35	–	40	–	50	–	ns
$\overline{RAS}$ pulse width	t_{RAS}	50	10k	60	10k	70	10k	ns
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	50	200k	60	200k	70	200k	ns
$\overline{CAS}$ precharge to $\overline{RAS}$ Delay	t_{RHCP}	30	–	35	–	40	–	ns
$\overline{CAS}$ precharge to $\overline{WE}$ (FPMR RMW)	t_{CPWD}	50	–	55	–	65	–	ns
$\overline{RAS}$ hold time	t_{RSH}	15		15	–	20	–	ns
$\overline{CAS}$ hold time	t_{CSH}	50		60	–	70	–	ns
$\overline{CAS}$ pulse width	t_{CAS}	15	10k	15	10k	20	10k	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time [12)]	t_{RCD}	20	35	20	45	20	50	
$\overline{RAS}$ to column address delay time [13)]	t_{RAD}	15	25	15	30	15	35	ns

AC Characteristics (cont'd) [5]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		HYB 5117400BJ/ BT-50		HYB 5117400BJ/ BT-60		HYB 5117400BJ/ BT-70		
		min.	max.	min.	max.	min.	max.	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	5	–	ns
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns
Row address hold time	t_{RAH}	10	–	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns
Column address hold time	t_{CAH}	10	–	15	–	15	–	ns
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	–	30	–	35	–	ns
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns
Read command hold time [9]	t_{RCH}	0	–	0	–	0	–	ns
Read command hold time referenced to $\overline{RAS}$ [9]	t_{RRH}	0	–	0	–	0	–	ns
Write command hold time	t_{WCH}	10	–	15	–	15	–	ns
Write command pulse width	t_{WP}	10	–	15	–	15	–	ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	–	15	–	20	–	ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	–	15	–	20	–	ns
Data setup time [10]	t_{DS}	0	–	0	–	0	–	ns
Data hold time [10]	t_{DH}	10	–	15	–	15	–	ns
Refresh period	t_{REF}	–	32	–	32	–	32	ms
Write command setup time [11]	t_{WCS}	0	–	0	–	0	–	ns
$\overline{CAS}$ to $\overline{WE}$ delay time [11]	t_{CWD}	35	–	35	–	45	–	ns
$\overline{RAS}$ to WE delay time [11]	t_{RWD}	70	–	80	–	95	–	ns
Column address to $\overline{WE}$ delay time [11]	t_{AWD}	45	–	50	–	60	–	ns
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CSR}	10	–	10	–	10	–	ns
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CHR}	10	–	10	–	10	–	ns

AC Characteristics (cont'd) [5]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		HYB 5117400BJ/ BT-50		HYB 5117400BJ/ BT-60		HYB 5117400BJ/ BT-70		
		min.	max.	min.	max.	min.	max.	
$\overline{CAS}$ hold time (Test mode entry cycle)	t_{CHRT}	30	–	30	–	30	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5	–	5	–	5	–	ns
$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ counter test cycle)	t_{CPT}	35	–	40	–	40	–	ns
Write command setup time (in test mode entry cycle)	t_{WTS}	10	–	10	–	10	–	ns
Write command hold time (in test mode entry cycle)	t_{WTH}	10	–	10	–	10	–	ns
Write to $\overline{RAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{WRP}	10	–	10	–	10	–	ns
Write hold time referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{WRH}	10	–	10	–	10	–	ns
$\overline{OE}$ command hold time	t_{OEH}	15	–	15	–	20	–	ns
$\overline{OE}$ access time	t_{OEA}	–	15	–	15	–	20	ns
Output buffer turn-off delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	ns
Data to $\overline{CAS}$ low delay [15]	t_{DZC}	0	–	0	–	0	–	ns
Data to $\overline{OE}$ low delay [15]	t_{DZO}	0	–	0	–	0	–	ns
$\overline{CAS}$ high to data delay [16]	t_{CDD}	15	–	15	–	20	–	ns
$\overline{OE}$ high to data delay [16]	t_{ODD}	15	–	15	–	20	–	ns
$\overline{RAS}$ pulse width during self refresh	t_{RASS}	100k	–	100k	–	100k	–	ns
$\overline{RAS}$ precharge time during self refresh	t_{RPS}	95	–	110	–	130	–	ns
$\overline{CAS}$ hold time during self refresh	t_{CHS}	– 50	–	– 50	–	– 50	–	ns

Capacitance

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A10)	C_{I1}	–	5	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}	–	7	pF
I/O capacitance (I/O1-I/O4)	C_{IO}	–	7	pF

Notes:

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.

4) Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4} it can be changed once or less during a fast page mode cycle (t_{PC}).

5) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6) $V_{IH\ (min.)}$ and $V_{IL\ (max.)}$ are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.

7) Measured with a load equivalent to 2 TTL loads and 100 pF.

8) $t_{OFF\ (max.)}$ and $t_{OEZ\ (max.)}$ define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.

9) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

10) These parameters are referenced to the CAS leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.

11) t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS\ (min.)}$, the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} > t_{RWD\ (min.)}$, $t_{CWD} > t_{CWD\ (min.)}$, $t_{AWD} > t_{AWD\ (min.)}$ and $t_{CPWD} > t_{CPWD\ (min.)}$, the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.

12) Operation within the $t_{RCD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RCD\ (max.)}$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD\ (max.)}$ limit, then access time is controlled by t_{CAC}.

13) Operation within the $t_{RAD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RAD\ (max.)}$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD\ (max.)}$ limit, then access time is controlled by t_{AA}.

14) AC measurements assume t_T = 5 ns.

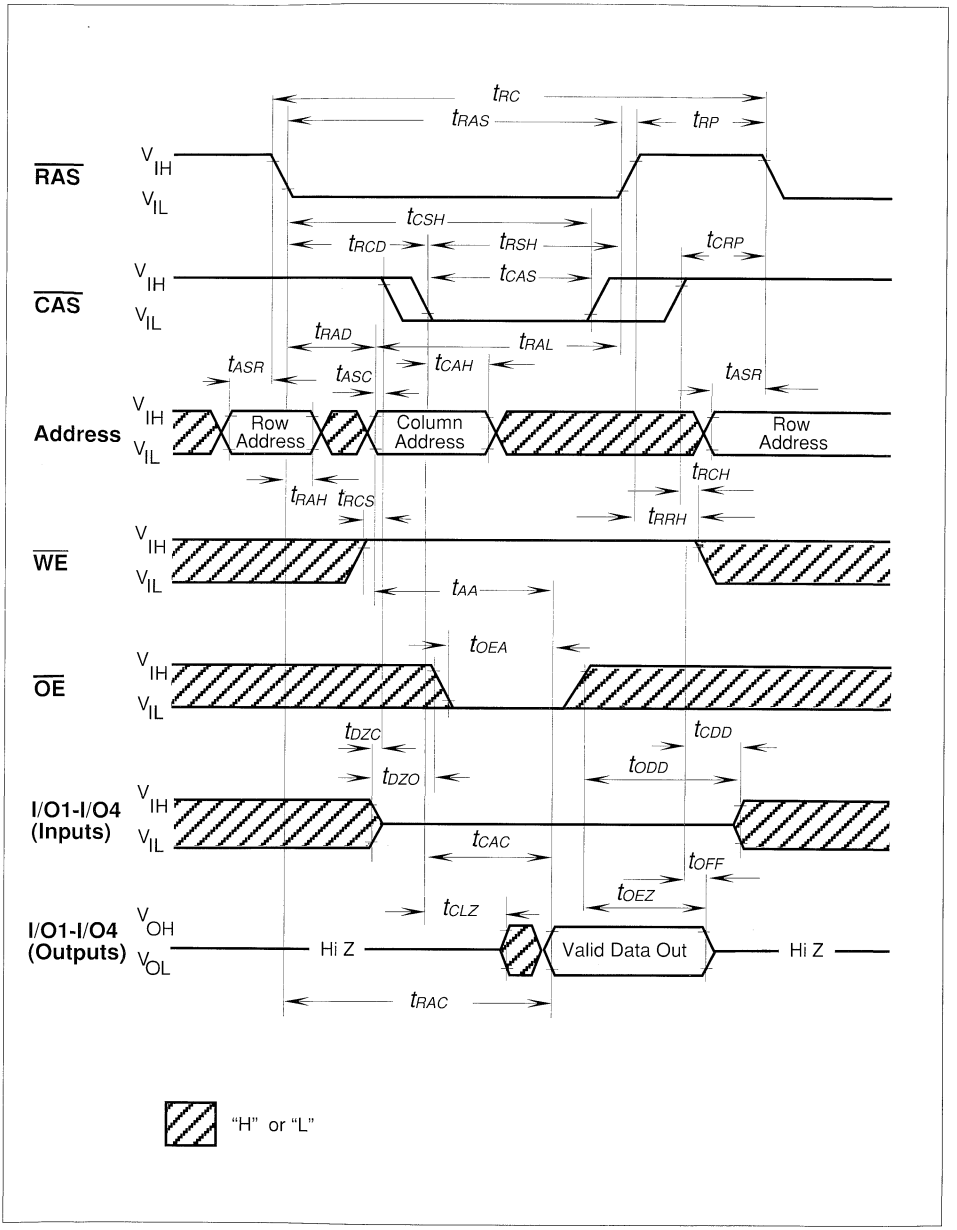
15) Either t_{DZC} or t_{DZO} must be satisfied.

16) Either t_{CDD} or t_{ODD} must be satisfied.

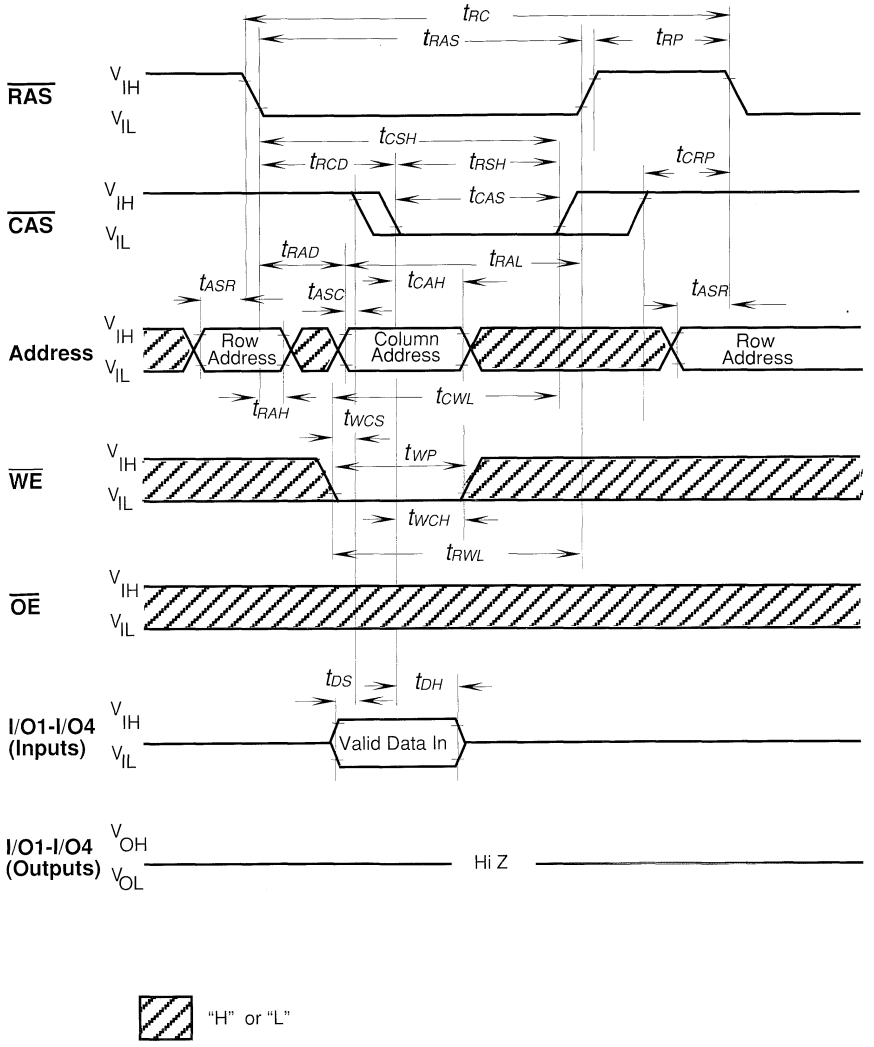
17) When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:

    If row addresses are being refreshed on an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh.

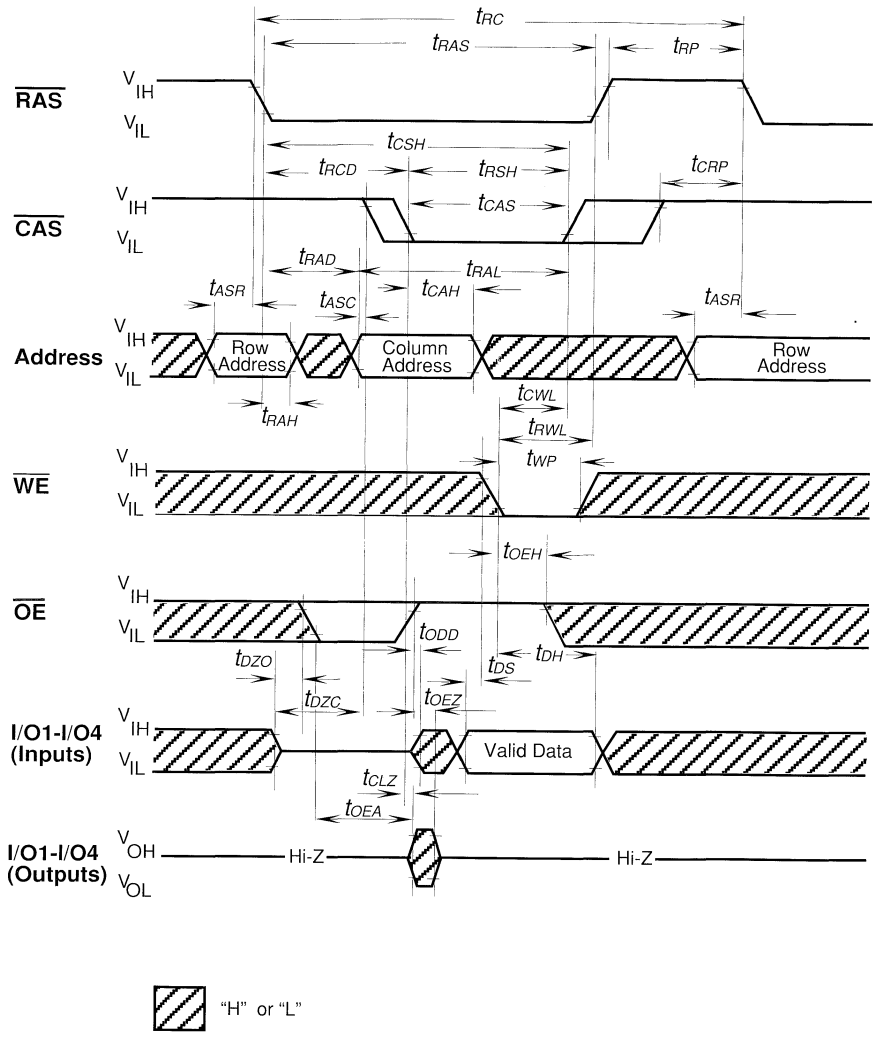
    If row addresses are being refreshed in any other manner (ROR - Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh.


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tASR
tASC
tCAH
Address
Row Address
Column Address
Row Address
tRCH
tRAH
tRCS
tRRH
WE
tAA
tOEA
OE
tDZC
tCDD
tDZO
tODD
I/O1-I/O4 (Inputs)
tCAC
tOFF
tOEZ
tCLZ
I/O1-I/O4 (Outputs)
VOH
VOL
Hi Z
Valid Data Out
Hi Z
tRAC
"H" or "L"

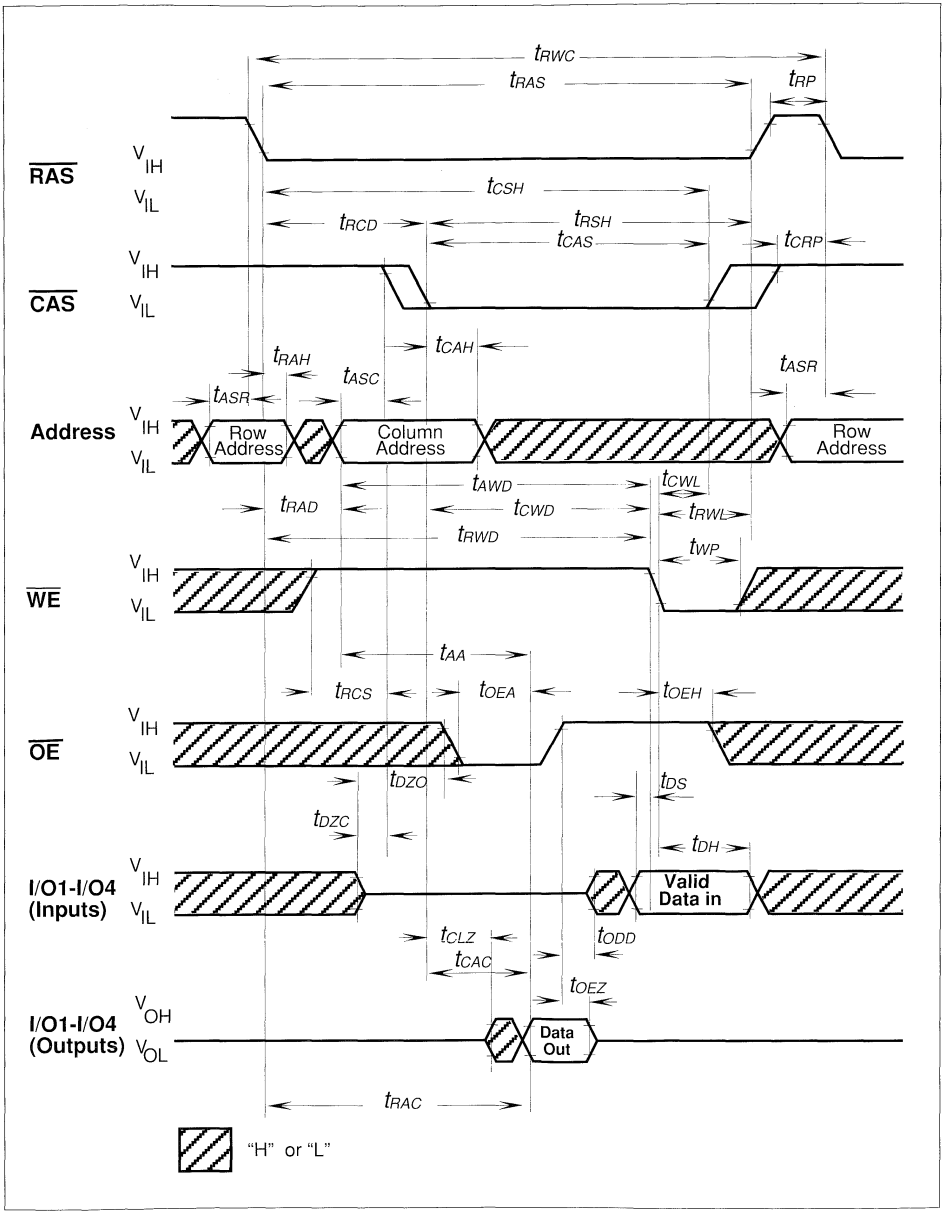
Read Cycle



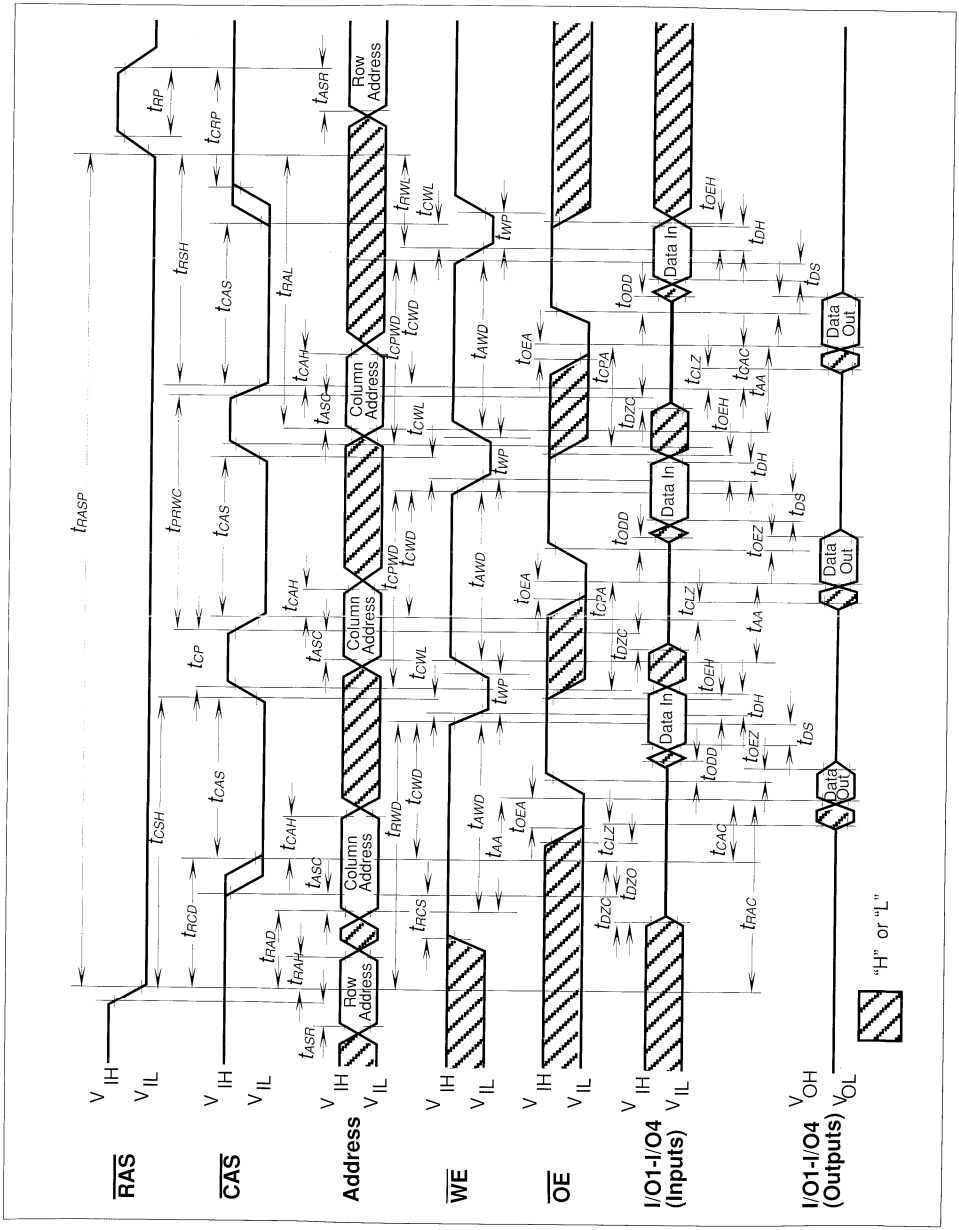
Write Cycle (Early Write)



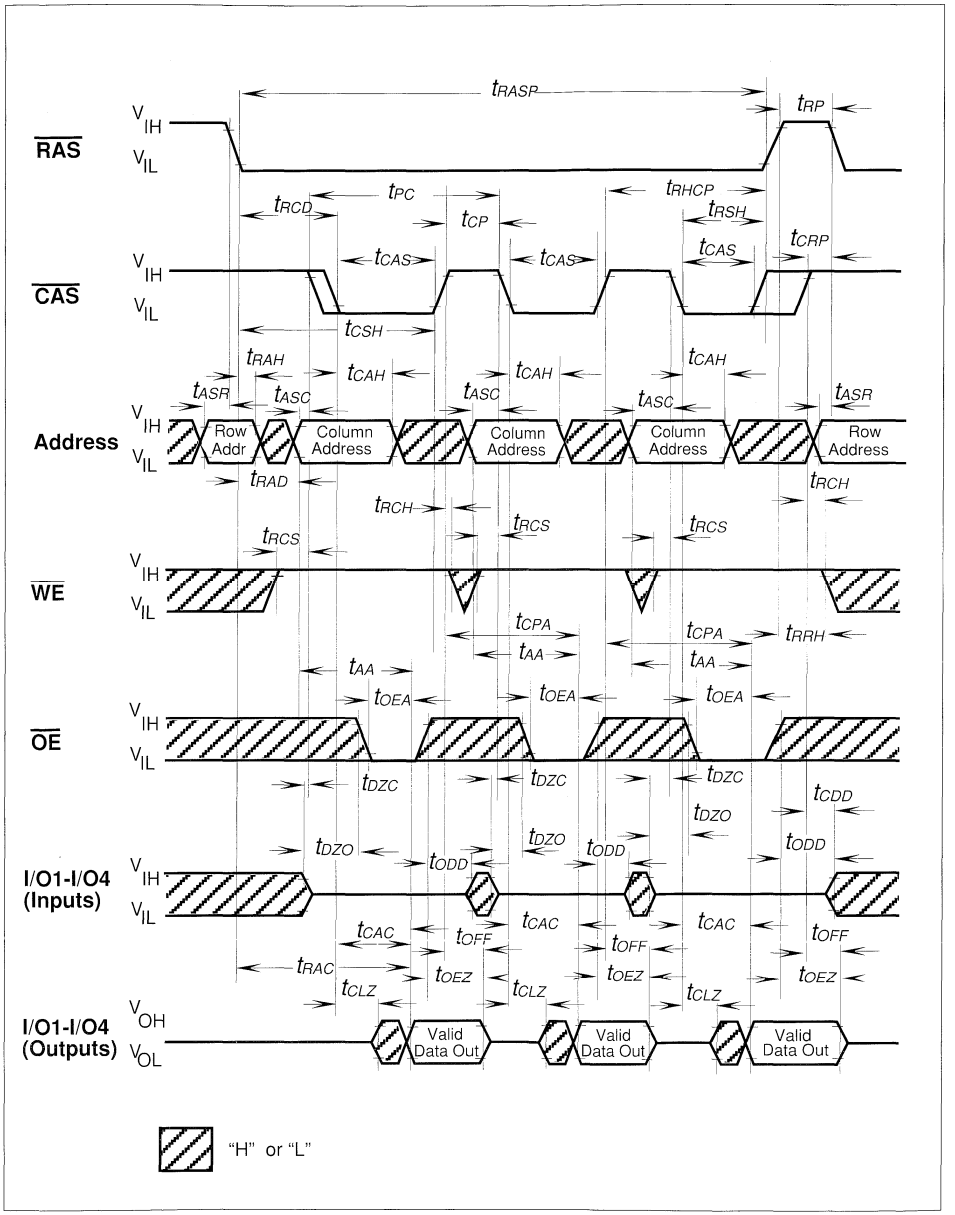
Write Cycle ($\overline{OE}$ Controlled Write)



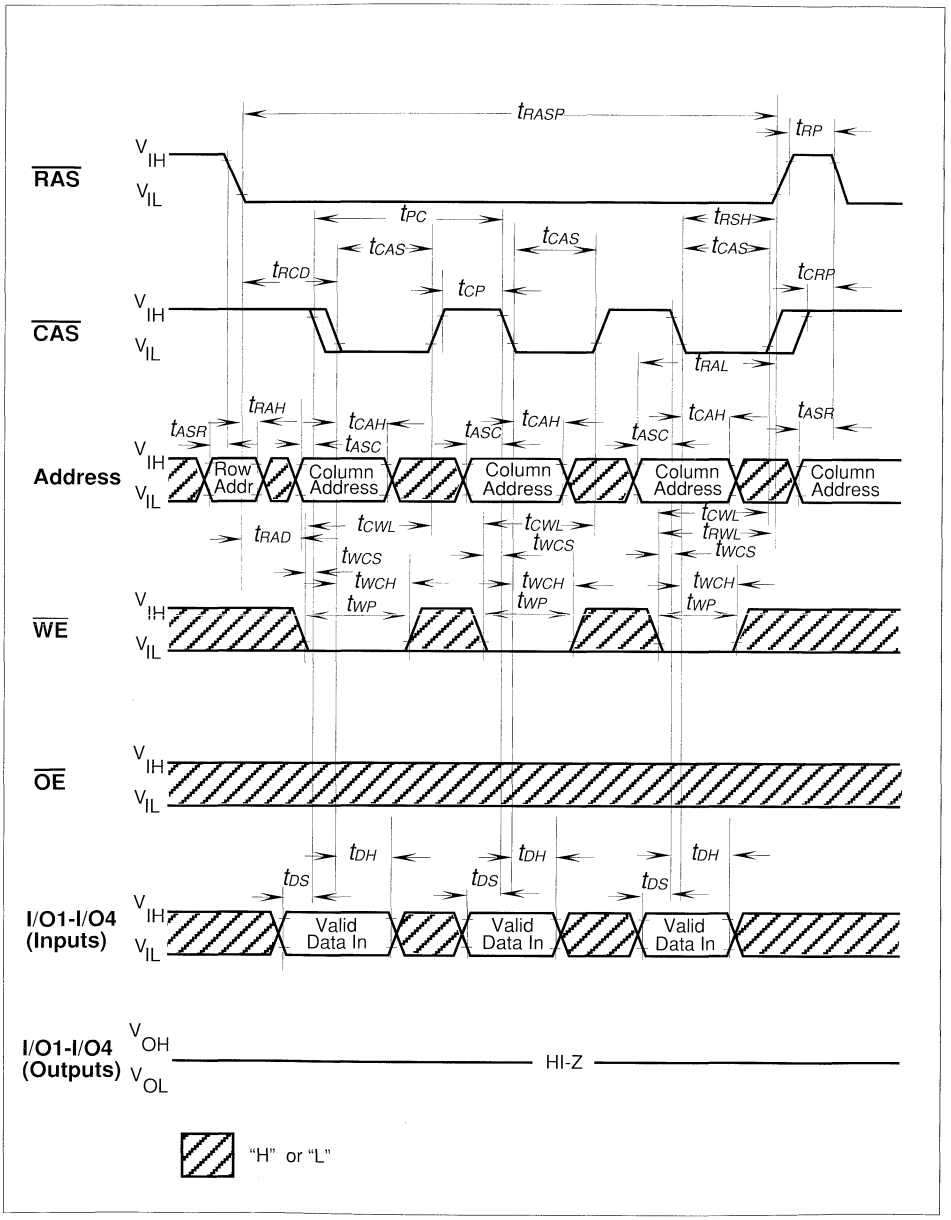
Read-Write (Read-Modify-Write) Cycle



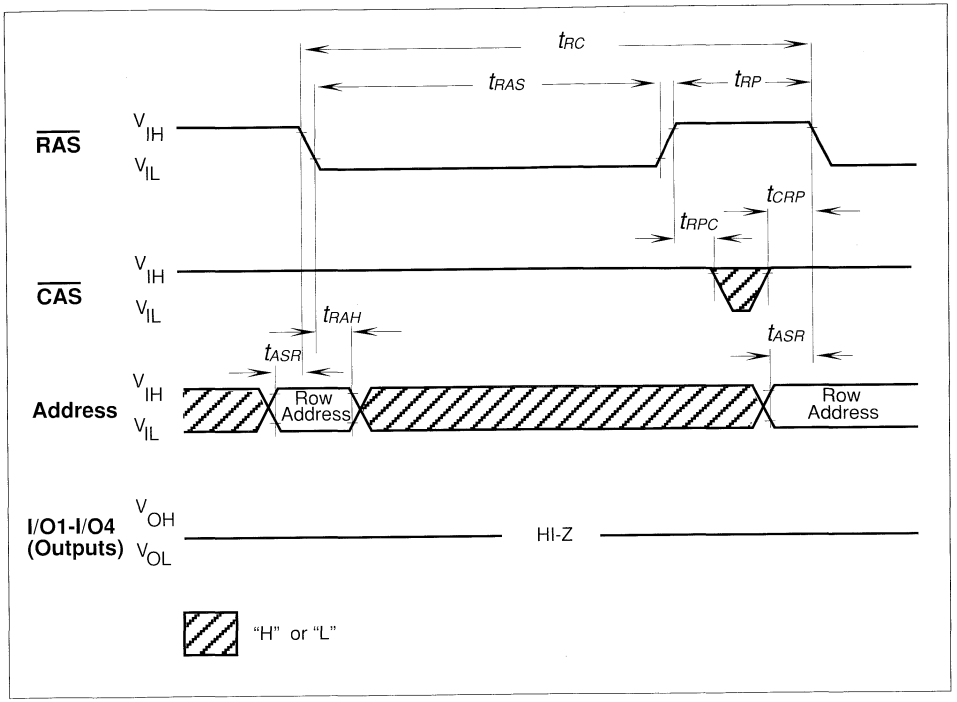
Fast Page Mode Read-Modify-Write Cycle



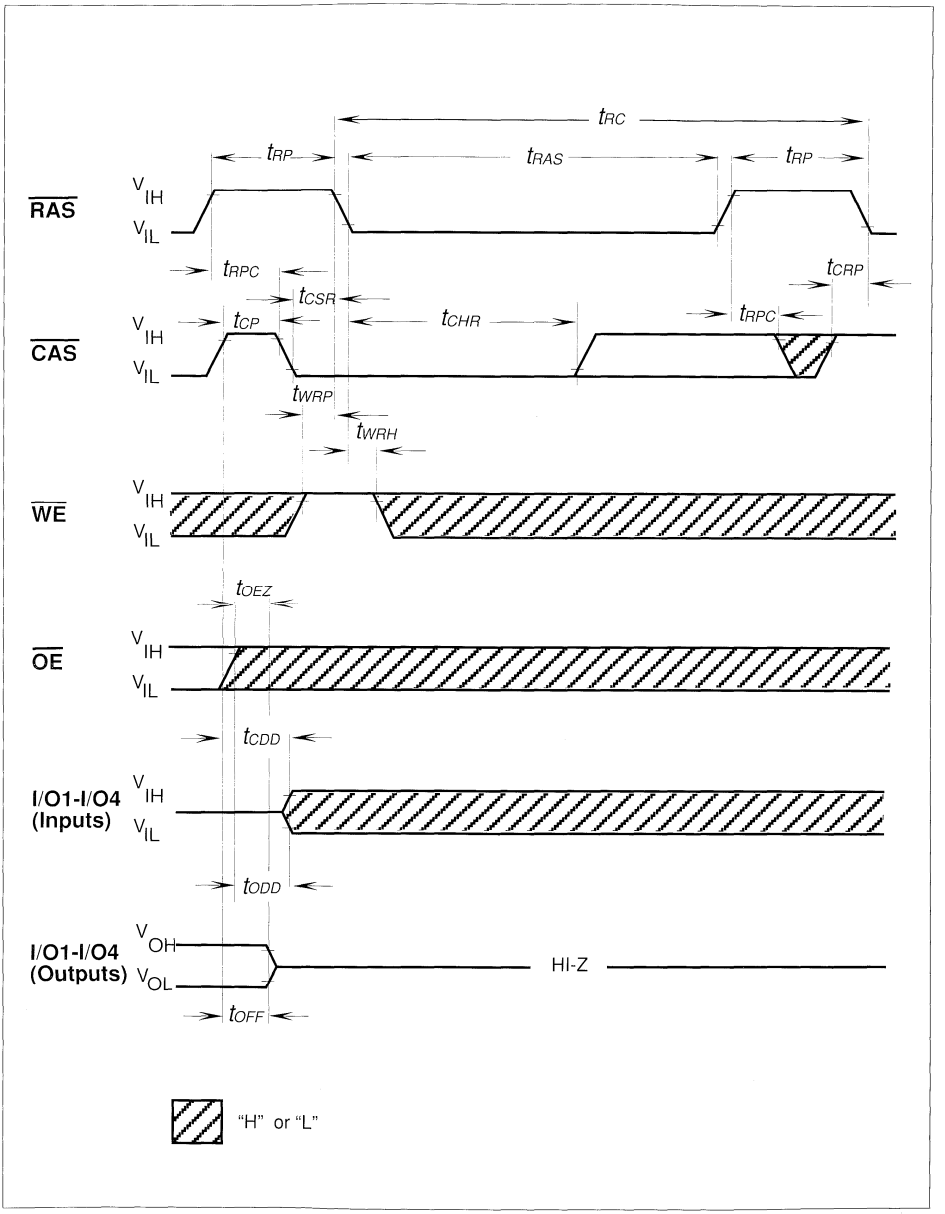
Fast Page Mode Read Cycle



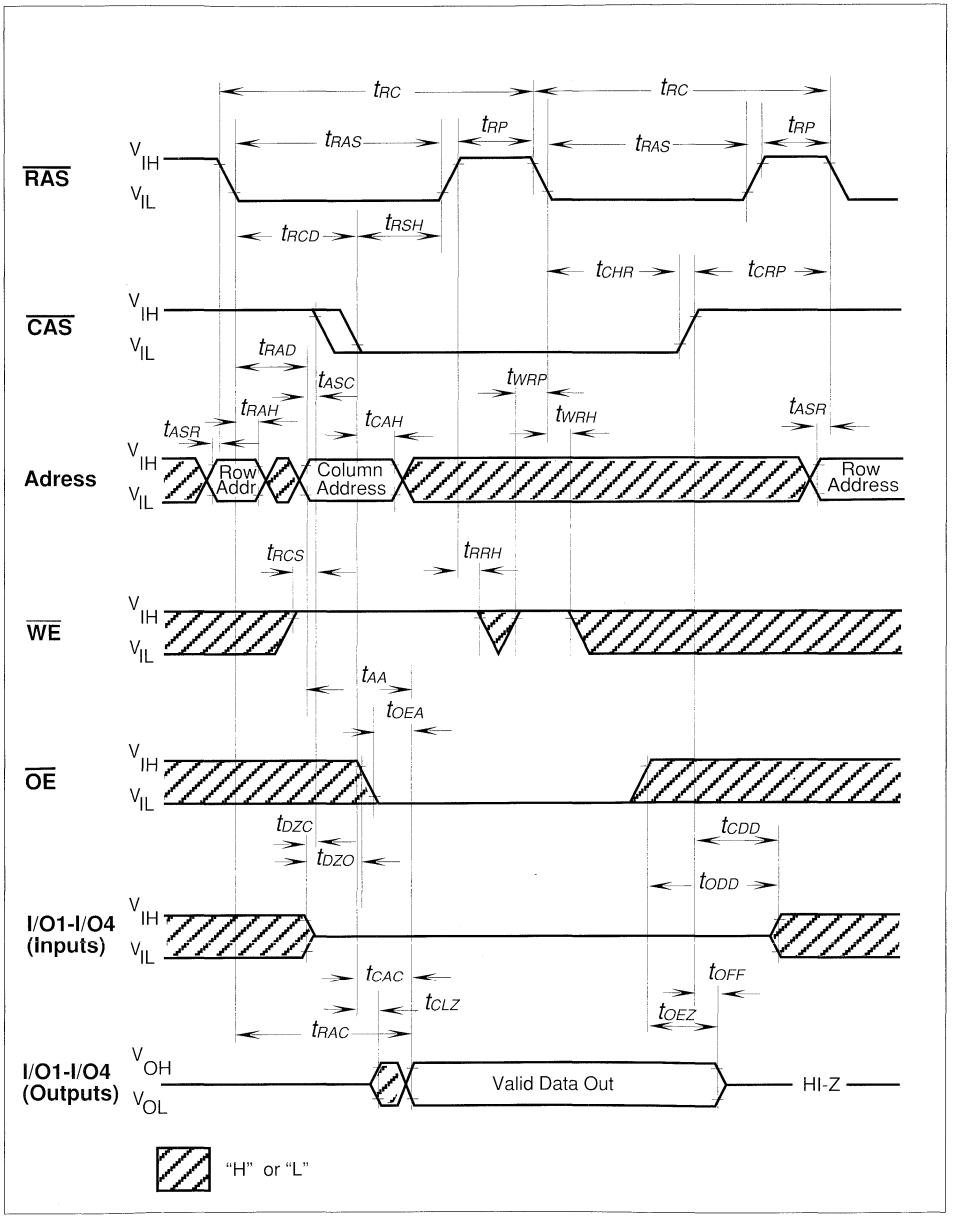
Fast Page Mode Early Write Cycle



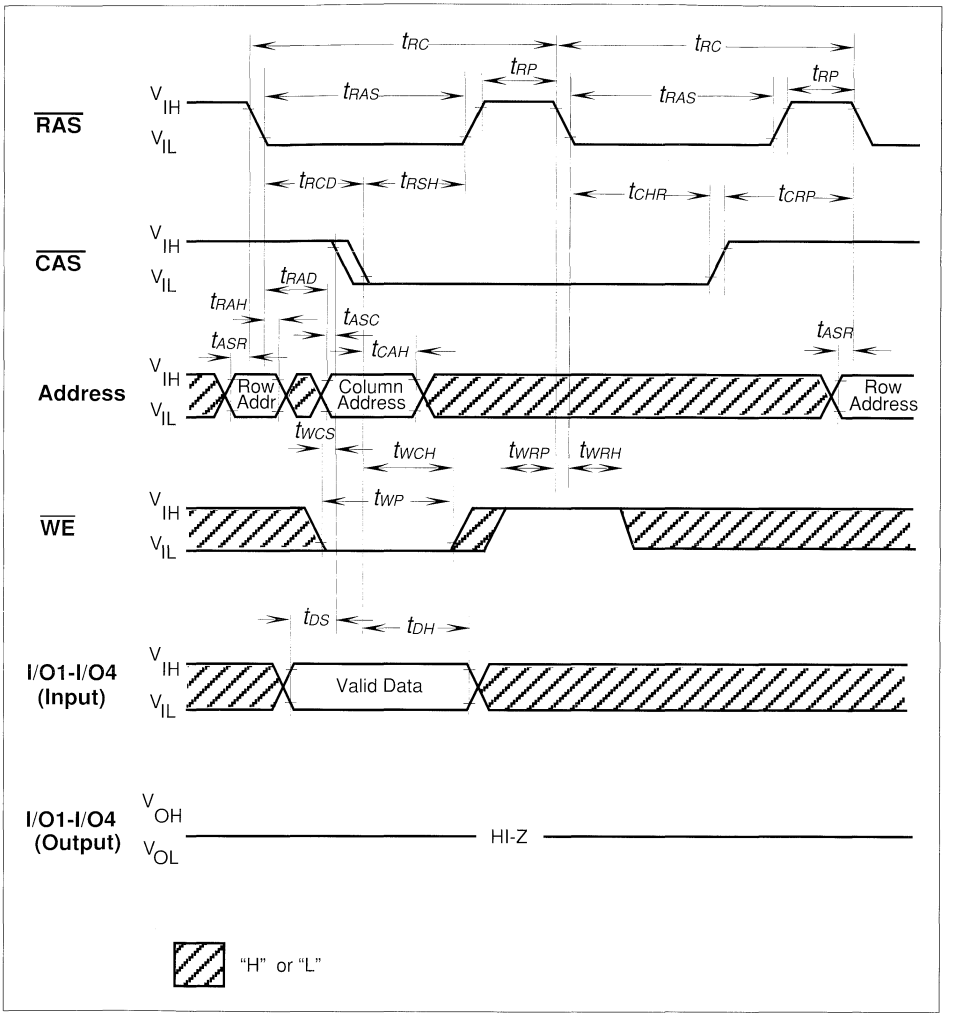
RAS-Only Refresh Cycle



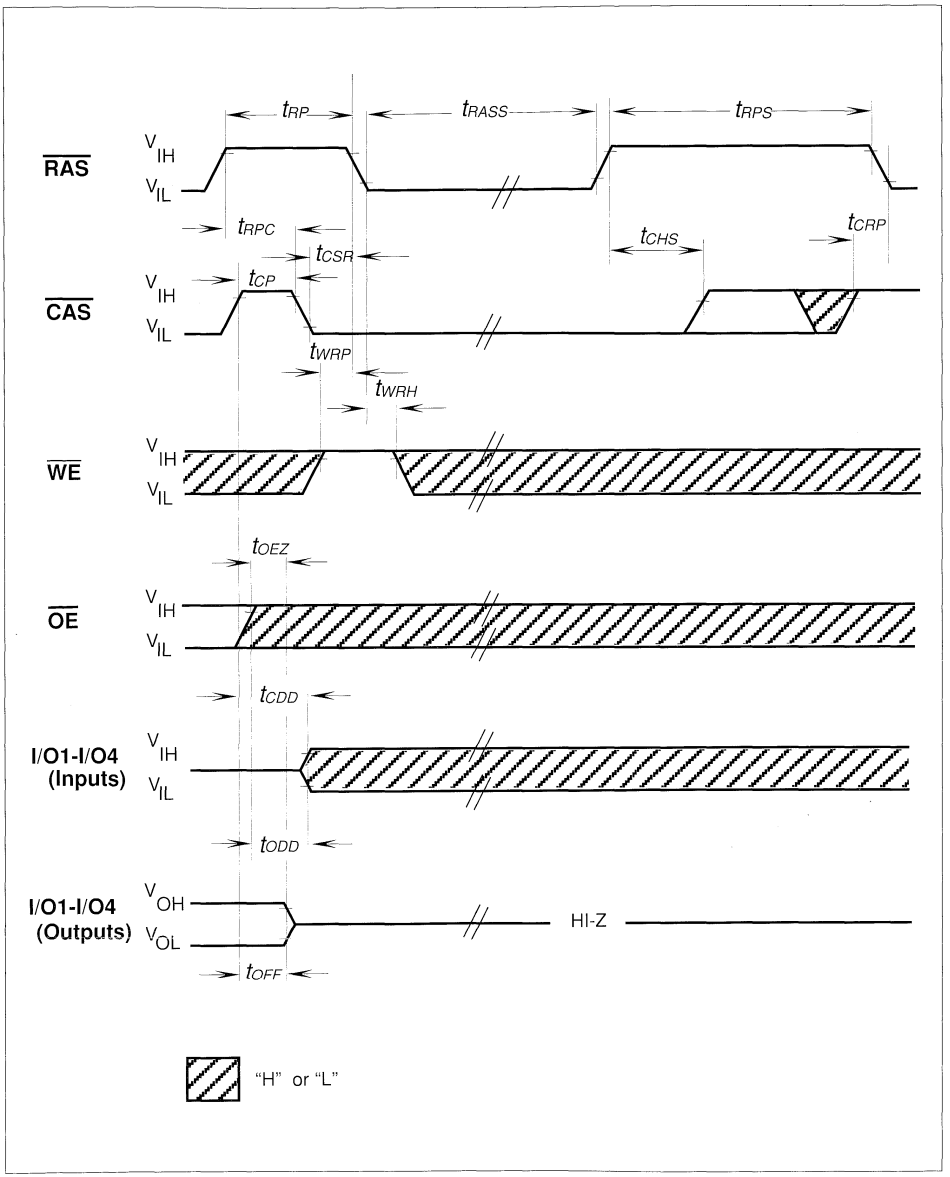
CAS-Before-RAS Refresh Cycle



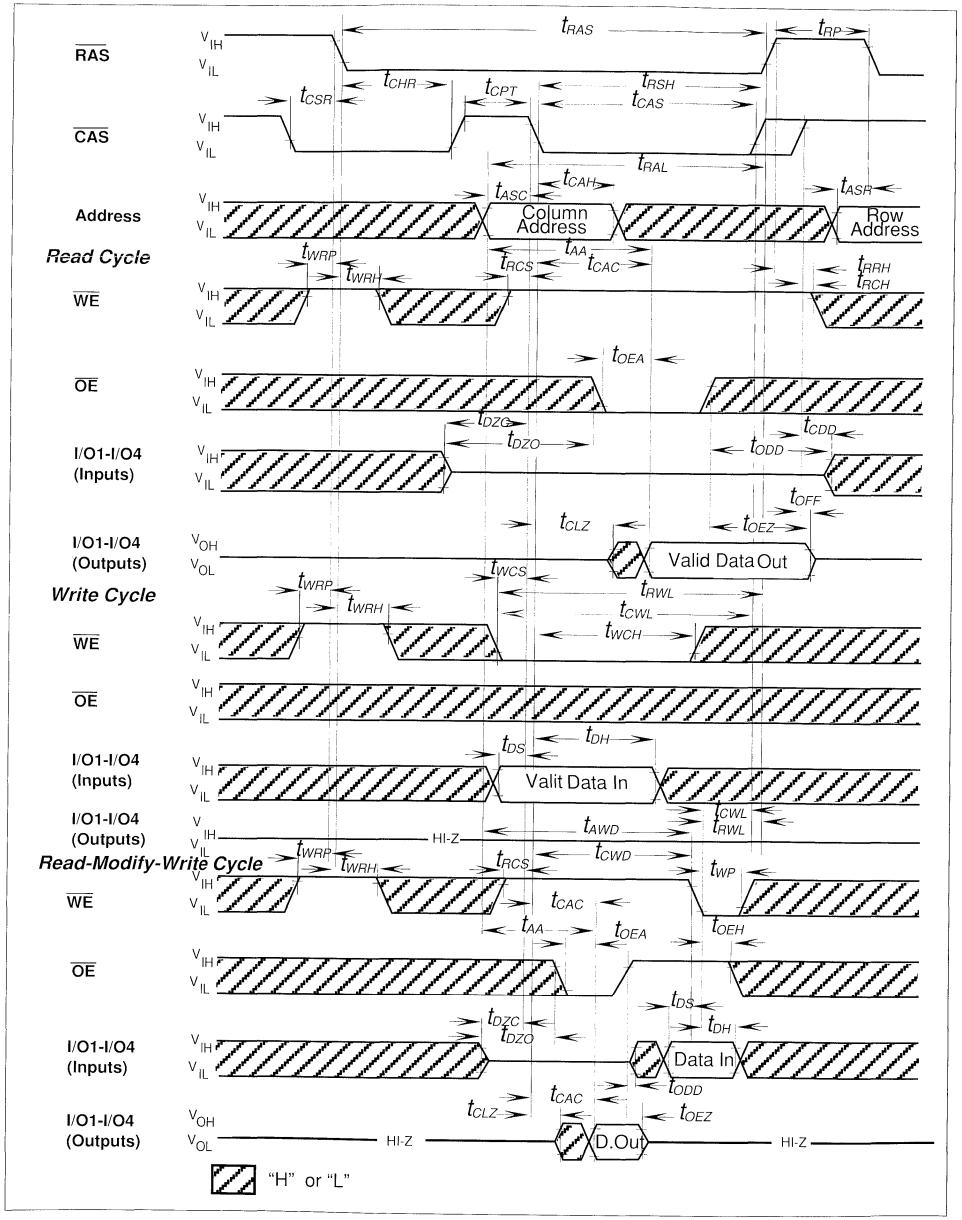
Hidden Refresh Cycle (Read)



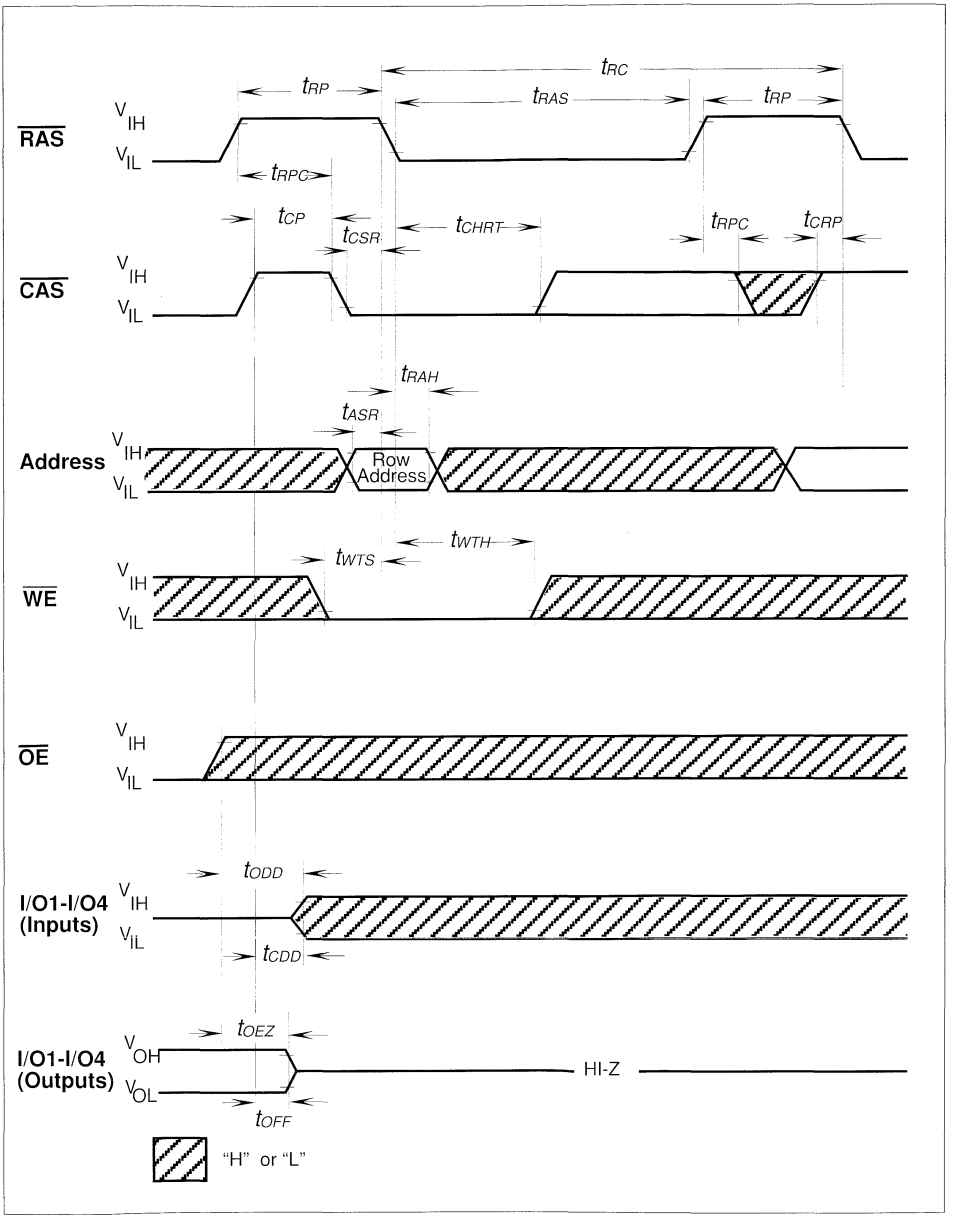
Hidden Refresh Cycle (Early Write)



CAS-before-RAS Self Refresh



CAS-Before-RAS Refresh Counter Test Cycle



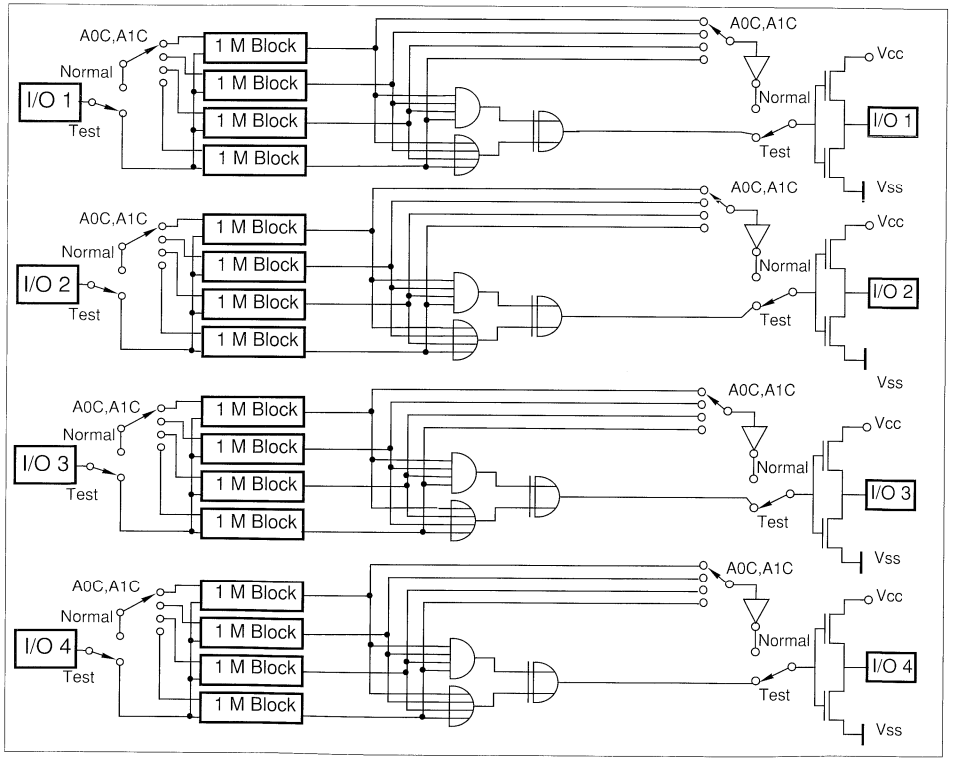
Test Mode Entry

Test Mode

As the HYB 5117400BJ/BT is organized internally as 1M x 16-bits, a test mode cycle using 4:1 compression can be used to improve test time. Note that in the 4M x 4 version the test time is reduced by 1/4 for a N test pattern.

In a test mode "write" the data from each I/O pin is written into four 1M blocks simultaneously (all "1" s or all "0" s). In test mode "read" each I/O output is used for indicating the test mode result. If the internal four bits are equal, the I/O would indicate a "1". If they were not equal, the I/O would indicate a "0". The WCBR cycle ($\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$) puts the device into test mode. To exit from test mode, a "$\overline{CAS}$ before $\overline{RAS}$ refresh", "$\overline{RAS}$ only refresh" or "Hidden refresh" can be used.Refresh during test mode operation can be performed by normal read cylces or by WCBR refresh cycles.

Row addresses A0 through A9 have to kept high to perform a testmode entry cylce. All other addresses are don't care.



Block Diagram in Test Mode

4M x 4-Bit Dynamic RAM (3.3 V, 4k-refresh)

HYB 3116400BJ/BT -50/-60/-70

Preliminary Information

- 4 194 304 words by 4-bit organization
- 0 to 70 °C operating temperature
- Fast access and cycle time
  $\overline{RAS}$ access time:
  50 ns (-50 version)
  60 ns (-60 version)
  70 ns (-70 version)
  Cycle time:
  95 ns (-50 version)
  110 ns (-60 version)
  130 ns (-70 version)
  $\overline{CAS}$ access time:
  15 ns (-50,-60 version)
  20 ns (-70 version)
- Fast page mode cycle time
  35 ns (-50 version)
  40 ns (-60 version)
  45 ns (-70 version)
- Single + 3.3 V (± 0.3V) supply
- Low power dissipation
  max. 360 active mW (-50 version)
  max. 324 active mW (-60 version)
  max. 288 active mW (-70 version)
  6.6 mW standby (TTL)
  3.3 mW standby (MOS)
- Output unlatched at cycle end allows two-dimensional chip selection
- Read, write, read-modify-write, $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, hidden refresh, Self Refresh and test mode
- Fast page mode capability
- All inputs, outputs and clocks fully TTL-compatible
- 4096 refresh cycles / 64 ms
- Plastic Package: P-SOJ-26/24-1 (300 mil)
  P-TSOPII-26/24-1 (300mil)

Ordering Information

Type	Ordering Code	Package	Descriptions
HYB 3116400BJ-50	on request	P-SOJ-26/24-1 300 mil	DRAM (access time 50 ns)
HYB 3116400BJ-60	on request	P-SOJ-26/24-1 300 mil	DRAM (access time 60 ns)
HYB 3116400BJ-70	on request	P-SOJ-26/24-1 300 mil	DRAM (access time 70 ns)
HYB 3116400BT-50	on request	P-TSOPII-26/24-1 300 mil	DRAM (access time 50 ns)
HYB 3116400BT-60	on request	P-TSOPII-26/24-1 300 mil	DRAM (access time 60 ns)
HYB 3116400BT-70	on request	P-TSOPII-26/24-1 300 mil	DRAM (access time 70 ns)

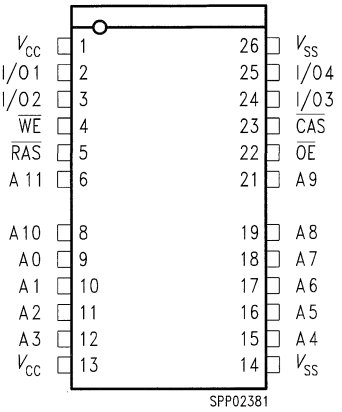
The HYB 3116400BJ/BT is the third generation dynamic RAM organized as 4194304 words by 4-bits. The HYB 3116400BJ/BT utilizes a submicron CMOS silicon gate process technology, as well as advanced circuit techniques to provide wide operating margins, both internally and for the system user. Multiplexed address inputs permit the HYB 3116400BJ/BT to be packaged in a standard SOJ 26/24 300 mil or TSOPII-26/24 300 mil wide plastic package. These packages provide high system bit densities and are compatible with commonly used automatic testing and insertion equipment. System-oriented features include single + 3.3 V (0.3 V) power supply, direct interfacing with high-performance logic device families.

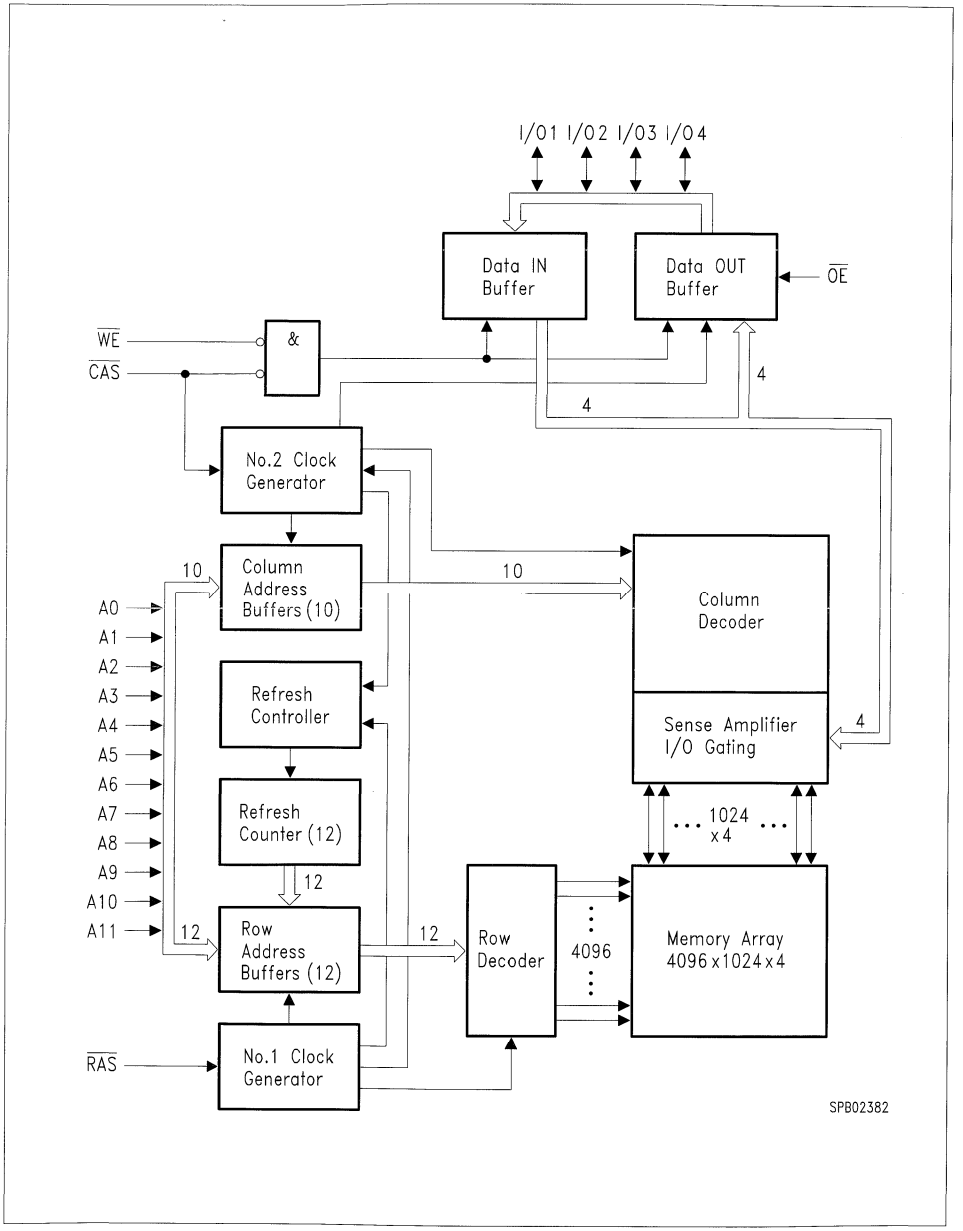
Pin Definitions and Functions

Pin No.	Function
A0 to A11	Row Address Inputs
A0 to A9	Column Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{OE}$	Output Enable
I/O1 -I/O4	Data Input/Output
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power Supply (+ 3.3 V)
V_{SS}	Ground (0 V)
N.C.	not connected

Pin Configuration
(top view)

P-SOJ-26/24-1 (300 mil)
P-TSOPII-26/24-1(300 mil)





Block Diagram

Absolute Maximum Ratings

Operating temperature range ..... 0 to 70 °C
Storage temperature range ..... – 55 to 150 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 0.5 to min (V_{CC} + 0.5, 4.6) V
Power supply voltage ..... – 0.5 V to 4.6 V
Power dissipation ..... 0.5 W
Data out current (short circuit) ..... 50 mA

Note:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 3.3 V ± 0.3 V, t_T = 5 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.0	V_{CC} + 0.5	V	1)
Input low voltage	V_{IL}	– 0.5	0.8	V	1)
TTL Output high voltage (I_{OUT} = – 2 mA)	V_{OH}	2.4	–	V	1)
TTL Output low voltage (I_{OUT} = 2 mA)	V_{OL}	–	0.4	V	1)
CMOS Output high voltage (I_{OUT} = – 100 uA)	V_{OH}	V_{CC} – 0.2	–	V	
CMOS Output low voltage (I_{OUT} = 100 uA)	V_{OL}	–	0.2	V	
Input leakage current (0 V ≤ V_{IH} ≤ V_{CC} + 0.3 V, all other pins = 0 V)	$I_{I(L)}$	– 10	10	µA	1)
Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ V_{CC} + 0.3 V)	$I_{O(L)}$	– 10	10	µA	1)
Average V_{CC} supply current: -50 ns version -60 ns version -70 ns version ($\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = t_{RC} min.)	I_{CC1}	 – – –	 100 90 80	 mA mA mA	 2) 3) 4) 2) 3) 4) 2) 3) 4)
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	2	mA	–

DC Characteristics (cont'd)

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 3.3 V ± 0.3 V, t_T = 5 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current, during $\overline{RAS}$-only refresh cycles: -50 ns version	I_{CC3}	–	100	mA	2) 4)
-60 ns version		–	90	mA	2) 4)
-70 ns version		–	80	mA	2) 4)
($\overline{RAS}$ cycling: $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} min.)					
Average V_{CC} supply current, during fast page mode: -50 ns version	I_{CC4}	–	85	mA	2) 3) 4)
-60 ns version		–	75	mA	2) 3) 4)
-70 ns version		–	65	mA	2) 3) 4)
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling, t_{PC} = t_{PC} min.)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	–	1	mA	1)
Average V_{CC} supply current, during $\overline{CAS}$-before-RAS refresh mode: -50 ns version	I_{CC6}	–	100	mA	2) 4)
-60 ns version		–	90	mA	2) 4)
-70 ns version		–	80	mA	2) 4)
($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min.)					
Average Self Refresh Current ($\overline{CBR}$ cycle with t_{RAS} > t_{RASS} min., $\overline{CAS}$ held low, $\overline{WE}$ = V_{CC} – 0.2 V, Address and Din = V_{CC} – 0.2 V or 0.2 V)	I_{CC7}	–	1	mA	

AC Characteristics [5]

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3V, t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		HYB 3116400BJ/BT -50		HYB 3116400BJ/BT -60		HYB 3116400BJ/BT -70		
		min.	max.	min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	95	–	110	–	130	–	ns
Read-write cycle time	t_{RWC}	135	–	150	–	180	–	ns
Fast page mode cycle time	t_{PC}	35	–	40	–	45	–	ns
Fast page mode read-write cycle time	t_{PRWC}	75	–	80	–	95	–	ns
Access time from $\overline{RAS}$ [7) 12)]	t_{RAC}	–	50	–	60	–	70	ns
Access time from $\overline{CAS}$ [7) 12)]	t_{CAC}	–	15	–	15	–	20	ns
Access time from column address [7) 13)]	t_{AA}	–	25	–	30	–	35	ns
Access time from $\overline{CAS}$ precharge [7)]	t_{CPA}	–	30	–	35	–	40	ns
$\overline{CAS}$ to output in low-Z [7)]	t_{CLZ}	0	–	0	–	0	–	ns
Output buffer turn-off delay [8)]	t_{OFF}	0	15	0	15	0	20	ns
Transition time (rise and fall) [6)]	t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	35	–	40	–	50	–	ns
$\overline{RAS}$ pulse width	t_{RAS}	50	10k	60	10k	70	10k	ns
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	50	200k	60	200k	70	200k	ns
$\overline{CAS}$ precharge to $\overline{RAS}$ Delay	t_{RHCP}	30	–	35	–	40	–	ns
$\overline{CAS}$ precharge to $\overline{WE}$ (FPMR RMW)	t_{CPWD}	50	–	55	–	65	–	ns
$\overline{RAS}$ hold time	t_{RSH}	15		15	–	20	–	ns
$\overline{CAS}$ hold time	t_{CSH}	50		60	–	70	–	ns

AC Characteristics (cont'd) [5]

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3V, t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		HYB 3116400BJ/BT -50		HYB 3116400BJ/BT -60		HYB 3116400BJ/BT -70		
		min.	max.	min.	max.	min.	max.	
$\overline{CAS}$ pulse width	t_{CAS}	15	10k	15	10k	20	10k	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time [12]	t_{RCD}	20	35	20	45	20	50	
$\overline{RAS}$ to column address delay time [13]	t_{RAD}	15	25	15	30	15	35	ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	5	–	ns
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns
Row address hold time	t_{RAH}	10	–	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns
Column address hold time	t_{CAH}	10	–	15	–	15	–	ns
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	–	30	–	35	–	ns
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns
Read command hold time [9]	t_{RCH}	0	–	0	–	0	–	ns
Read command hold time referenced to $\overline{RAS}$ [9]	t_{RRH}	0	–	0	–	0	–	ns
Write command hold time	t_{WCH}	10	–	15	–	15	–	ns
Write command pulse width	t_{WP}	10	–	15	–	15	–	ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	–	15	–	20	–	ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	–	15	–	20	–	ns

AC Characteristics (cont'd) [5]

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3V, t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		HYB 3116400BJ/BT -50		HYB 3116400BJ/BT -60		HYB 3116400BJ/BT -70		
		min.	max.	min.	max.	min.	max.	
Data setup time [10]	t_{DS}	0	–	0	–	0	–	ns
Data hold time [10]	t_{DH}	10	–	15	–	15	–	ns
Refresh period	t_{REF}	–	64	–	64	–	64	ms
Write command setup time [11]	t_{WCS}	0	–	0	–	0	–	ns
$\overline{CAS}$ to $\overline{WE}$ delay time [11]	t_{CWD}	35	–	35	–	45	–	ns
$\overline{RAS}$ to $\overline{WE}$ delay time [11]	t_{RWD}	70	–	80	–	95	–	ns
Column address to $\overline{WE}$ delay time [11]	t_{AWD}	45	–	50	–	60	–	ns
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CSR}	10	–	10	–	10	–	ns
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CHR}	10	–	10	–	10	–	ns
$\overline{CAS}$ hold time (Test mode entry cycle)	t_{CHRT}	30	–	30	–	30	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5	–	5	–	5	–	ns
$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ counter test cycle)	t_{CPT}	35	–	40	–	40	–	ns
Write command setup time (in test mode entry cycle)	t_{WTS}	10	–	10	–	10	–	ns
Write command hold time (in test mode entry cycle)	t_{WTH}	10	–	10	–	10	–	ns
Write to $\overline{RAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{WRP}	10	–	10	–	10	–	ns

AC Characteristics (cont'd) [5]

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3V, t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		HYB 3116400BJ/BT -50		HYB 3116400BJ/BT -60		HYB 3116400BJ/BT -70		
		min.	max.	min.	max.	min.	max.	
Write hold time referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{WRH}	10	–	10	–	10	–	ns
$\overline{OE}$ command hold time	t_{OEH}	15	–	15	–	20	–	ns
$\overline{OE}$ access time	t_{OEA}	–	15	–	15	–	20	ns
Output buffer turn-off delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	ns
Data to $\overline{CAS}$ low delay [15]	t_{DZC}	0	–	0	–	0	–	ns
Data to $\overline{OE}$ low delay [15]	t_{DZO}	0	–	0	–	0	–	ns
$\overline{CAS}$ high to data delay [16]	t_{CDD}	15	–	15	–	20	–	ns
$\overline{OE}$ high to data delay [16]	t_{ODD}	15	–	15	–	20	–	ns
$\overline{RAS}$ pulse width during self refresh [17]	t_{RASS}	100	–	100	–	100	–	s
$\overline{RAS}$ precharge time during self refresh [17]	t_{RPS}	95	–	110	–	130	–	ns
$\overline{CAS}$ hold time during self refresh	t_{CHS}	– 50	–	– 50	–	– 50	–	ns

Capacitance

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3 V, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A11)	C_{I1}	–	5	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}	–	7	pF
I/O capacitance (I/O1 - I/O4)	C_{IO}	–	7	pF

Notes:

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.

4) Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{cc4} it can be changed once or less during a fast page mode cycle (t_{PC}).

5) An initial pause of 200 µs is required after power-up followed by 8 RAS cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS cycles are required.

6) $V_{IH\ (min.)}$ and $V_{IL\ (max.)}$ are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.

7) Measured with a load equivalent to 100 pF and at V_{oh} = 2.0 V (I_{oh} = –2 mA), V_{ol} = 0.8 V (I_{ol} = 2 mA).

8) $t_{OFF\ (max.)}$ and $t_{OEZ\ (max.)}$ define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.

9) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

10) These parameters are referenced to the CAS leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.

11) t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS\ (min.)}$, the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} \geq t_{RWD\ (min.)}$, $t_{CWD} \geq t_{CWD\ (min.)}$, $t_{AWD} > t_{AWD\ (min.)}$ and $t_{CPWD} \geq t_{CPWD\ (min.)}$, the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.

12) Operation within the $t_{RCD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RCD\ (max.)}$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD\ (max.)}$ limit, then access time is controlled by t_{CAC}.

13) Operation within the $t_{RAD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RAD\ (max.)}$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD\ (max.)}$ limit, then access time is controlled by t_{AA}.

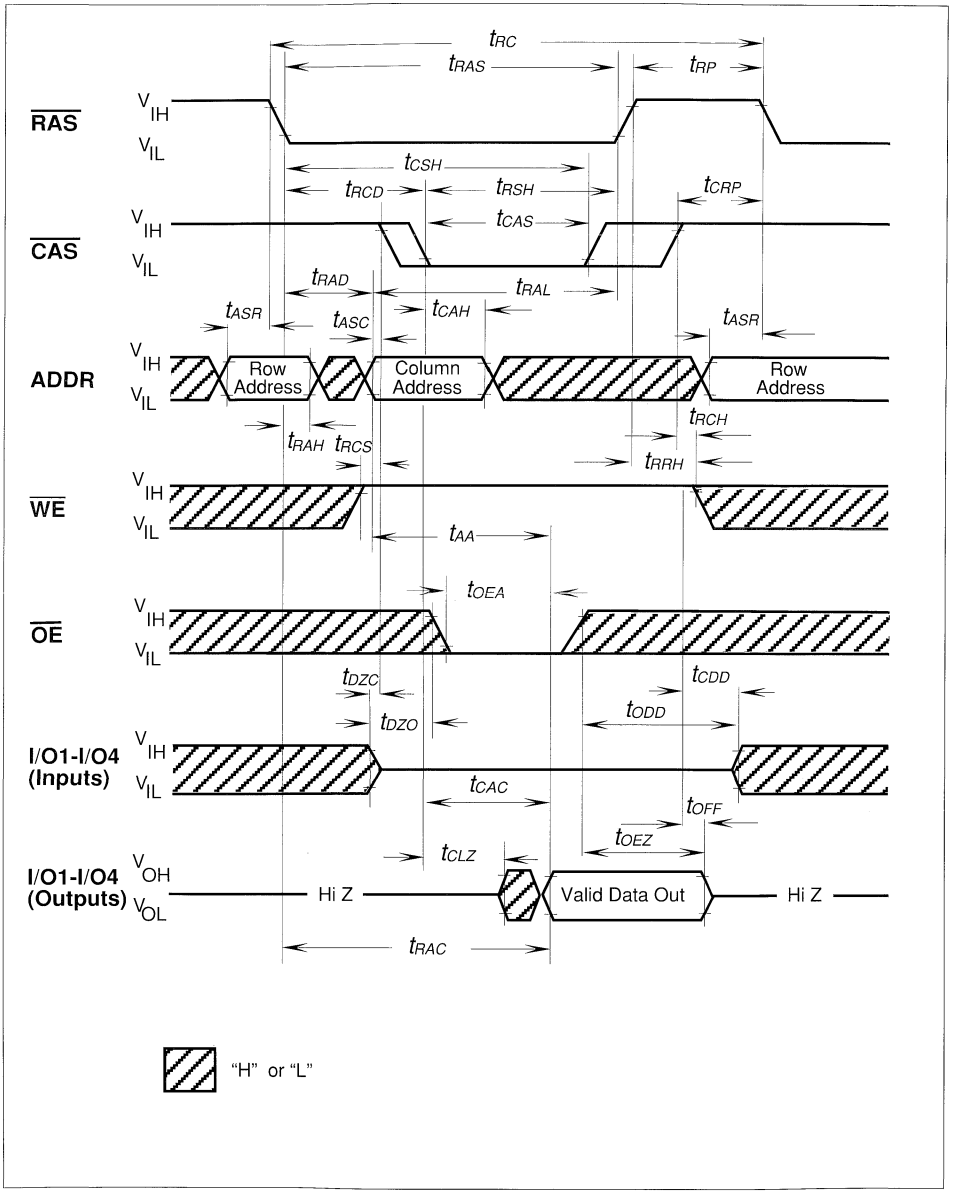
14) AC measurements assume t_T = 5 ns.

15) Either t_{DZC} or t_{DZO} must be satisfied.

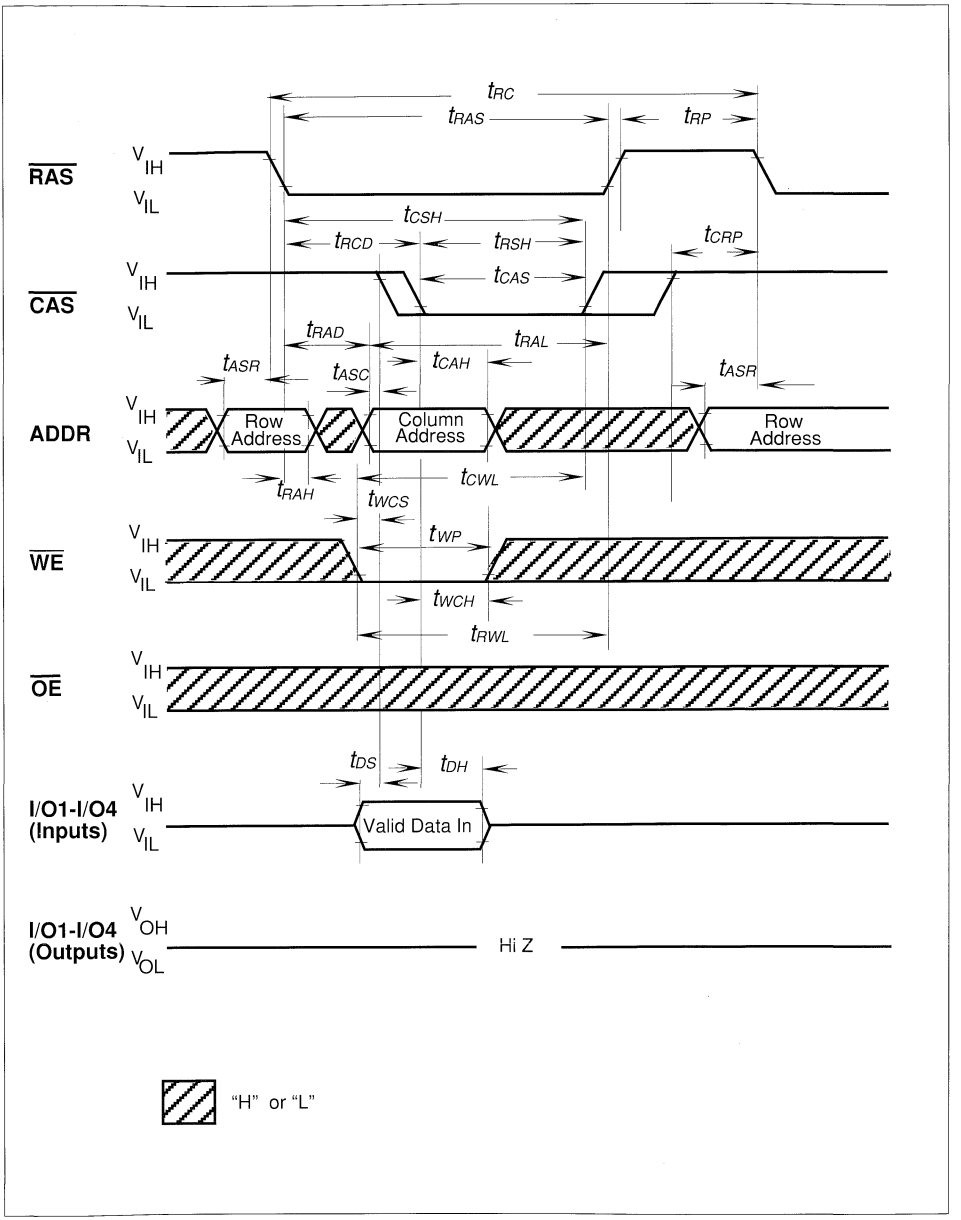
16) Either t_{CDD} or t_{ODD} must be satisfied.

17) Self Refresh occurs when a CBR cycle is initiated which $\overline{RAS}$ and $\overline{CAS}$ are kept active for an indefinite time that exceeds the DRAM active specification. The part then will internally cycle through all refresh addresses at a rate defined by the internal design of the part. The mode is exited by $\overline{RAS}$ going inactive.

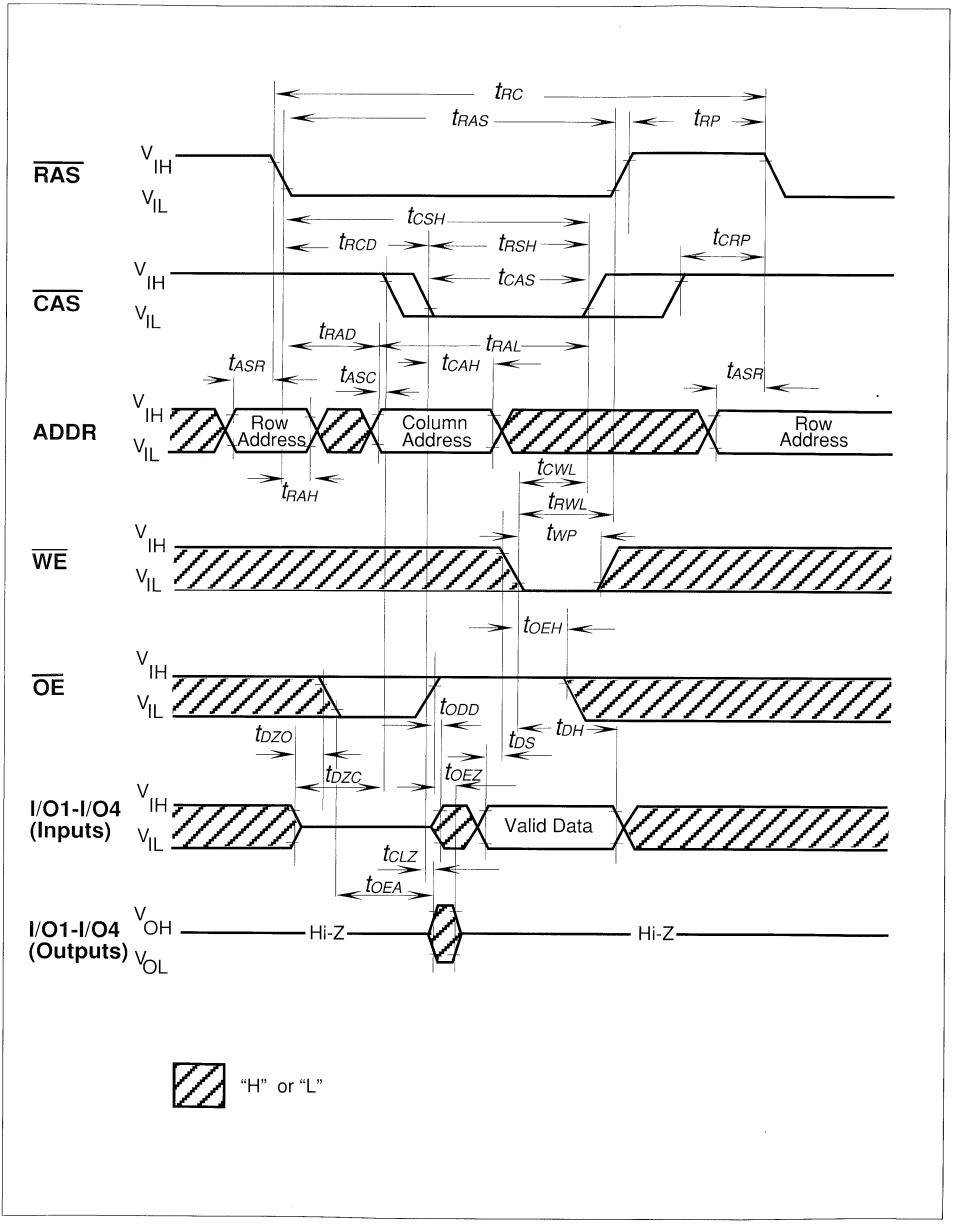
Waveforms



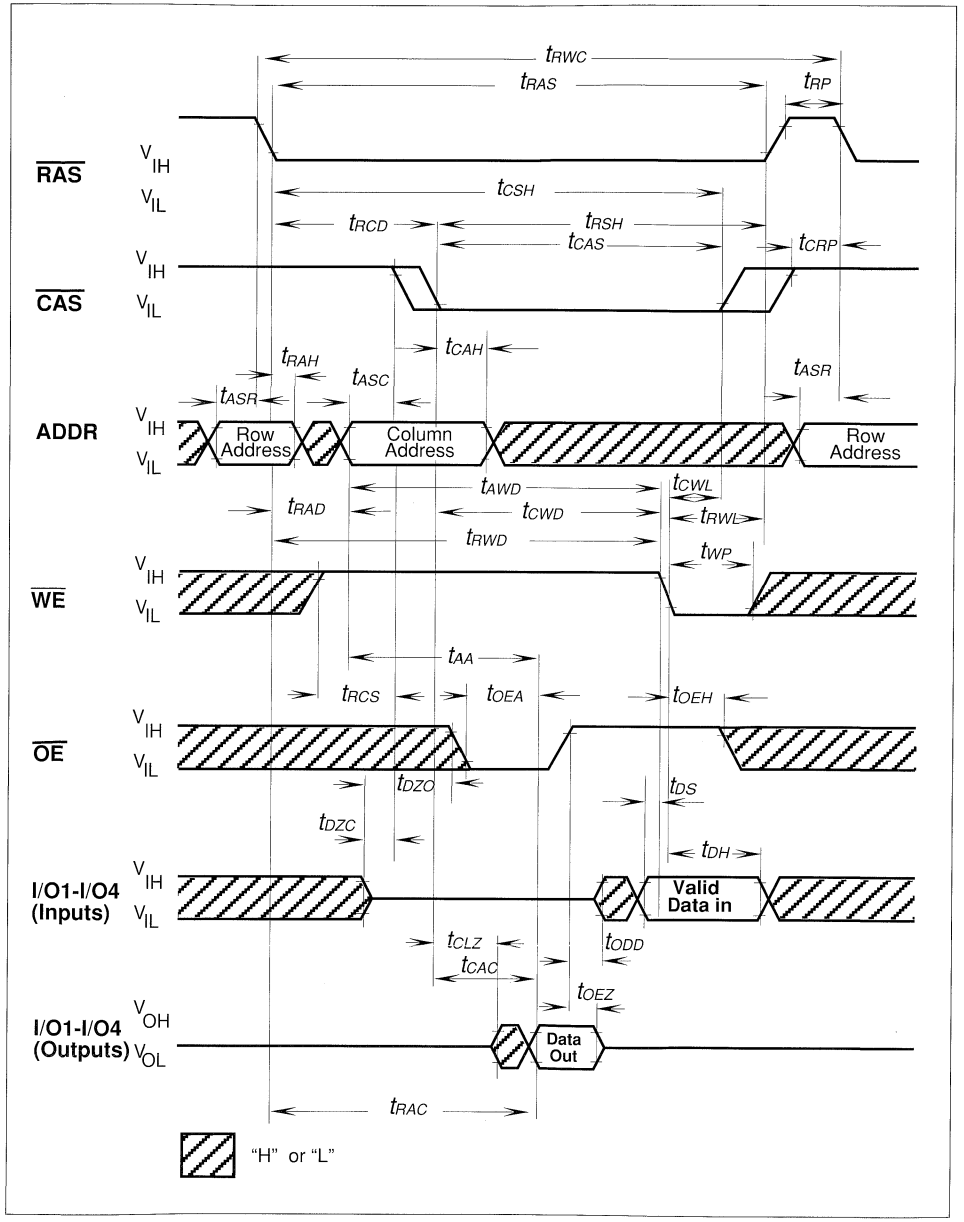
Read Cycle



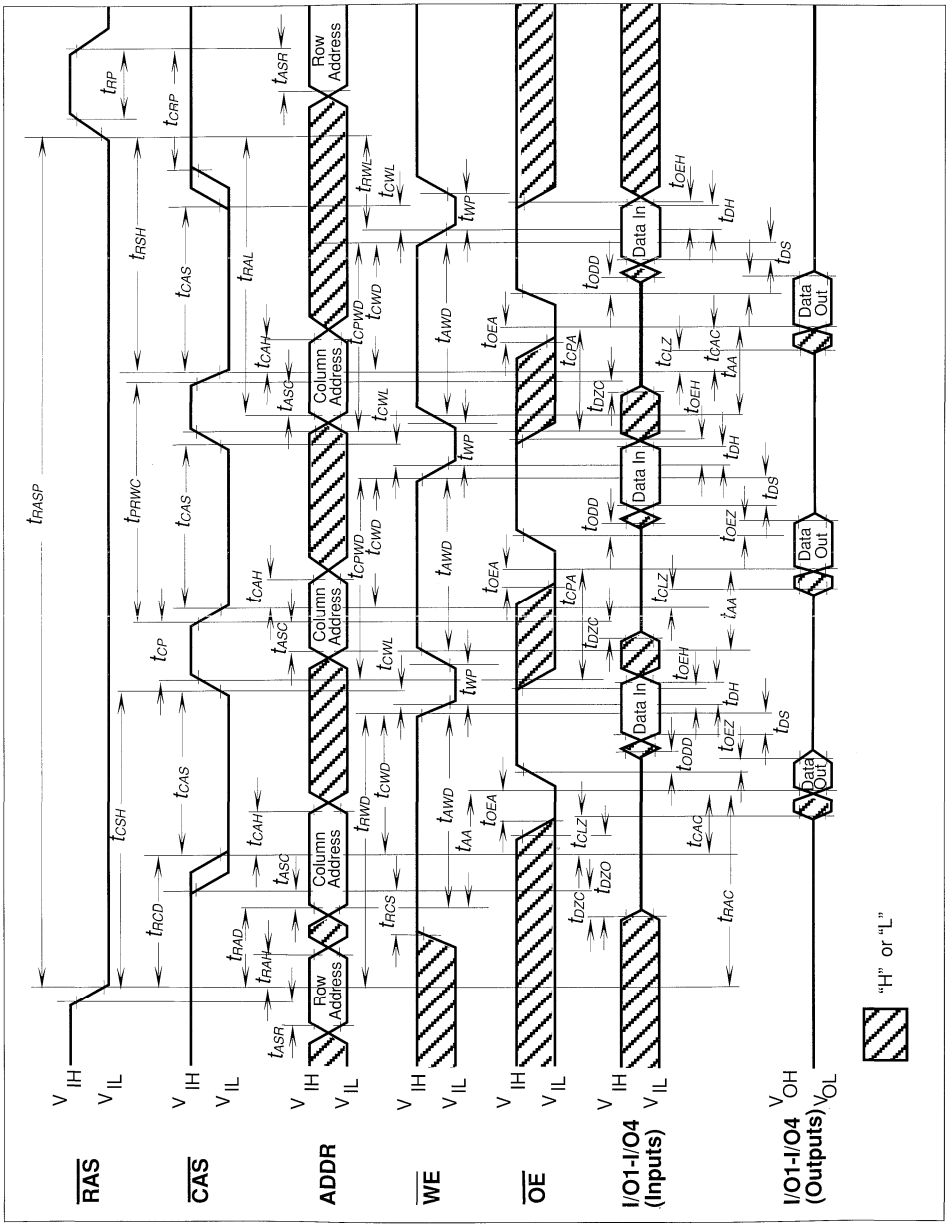
Write Cycle (Early Write)



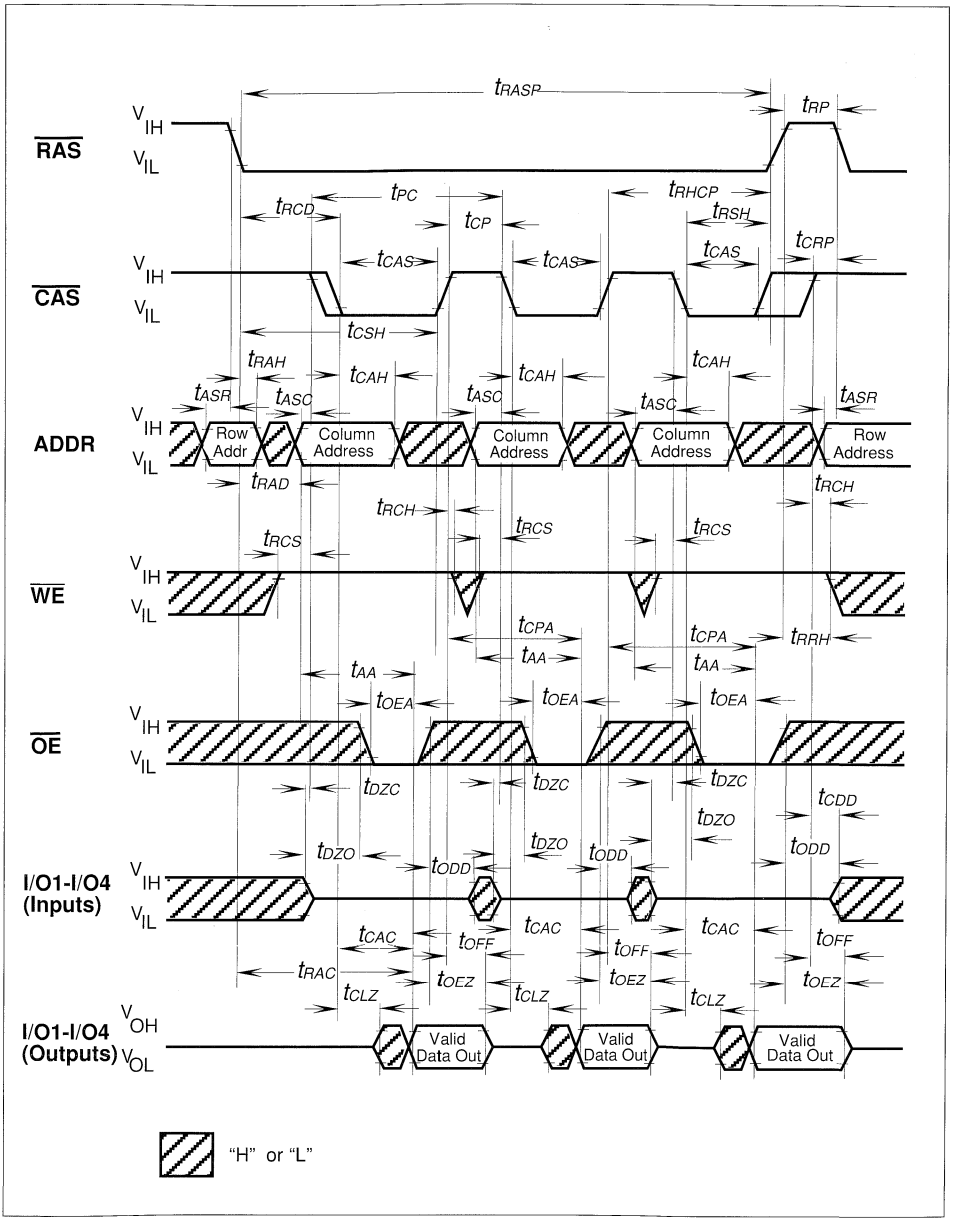
Write Cycle ($\overline{OE}$ Controlled Write)



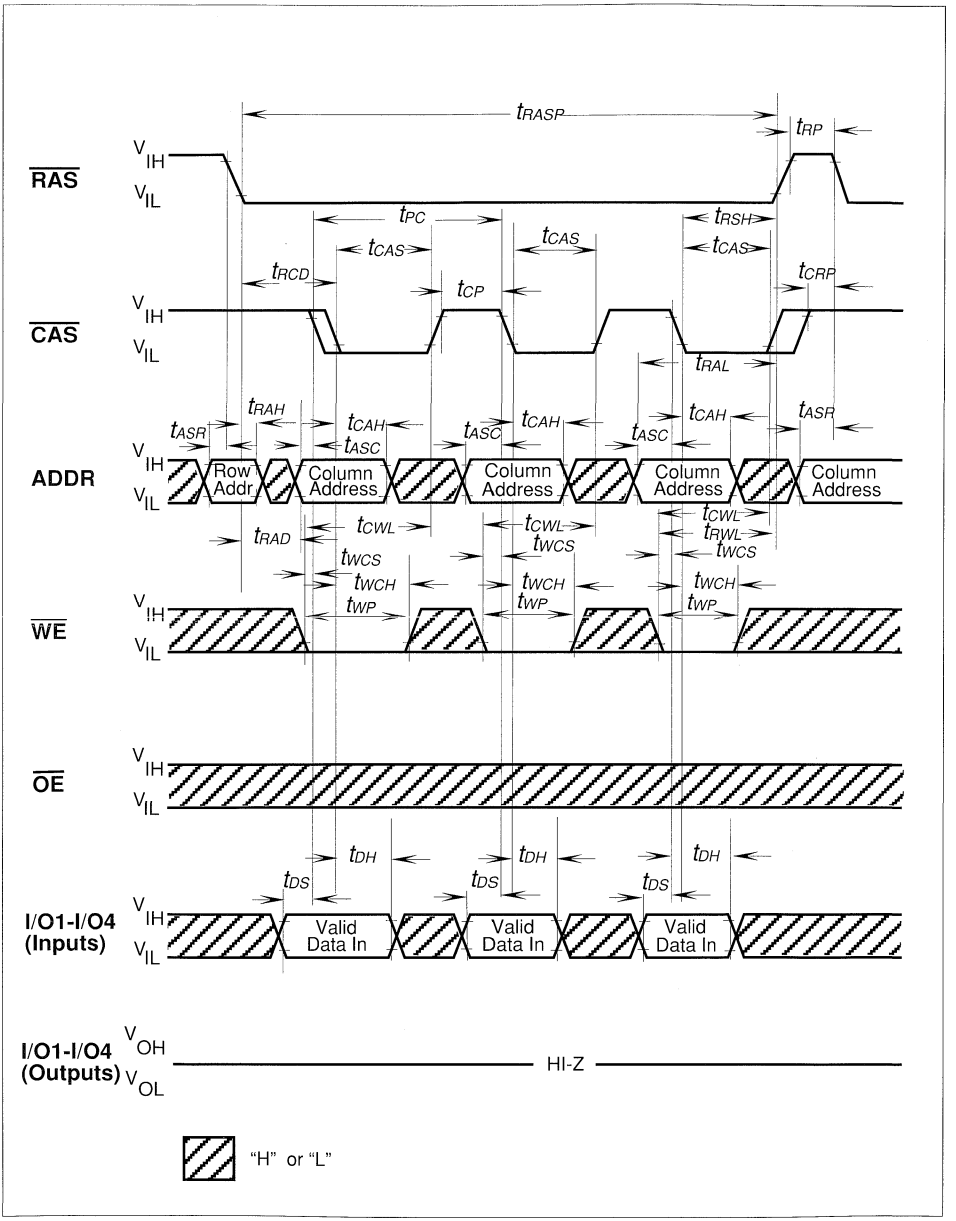
Read-Write (Read-Modify-Write) Cycle



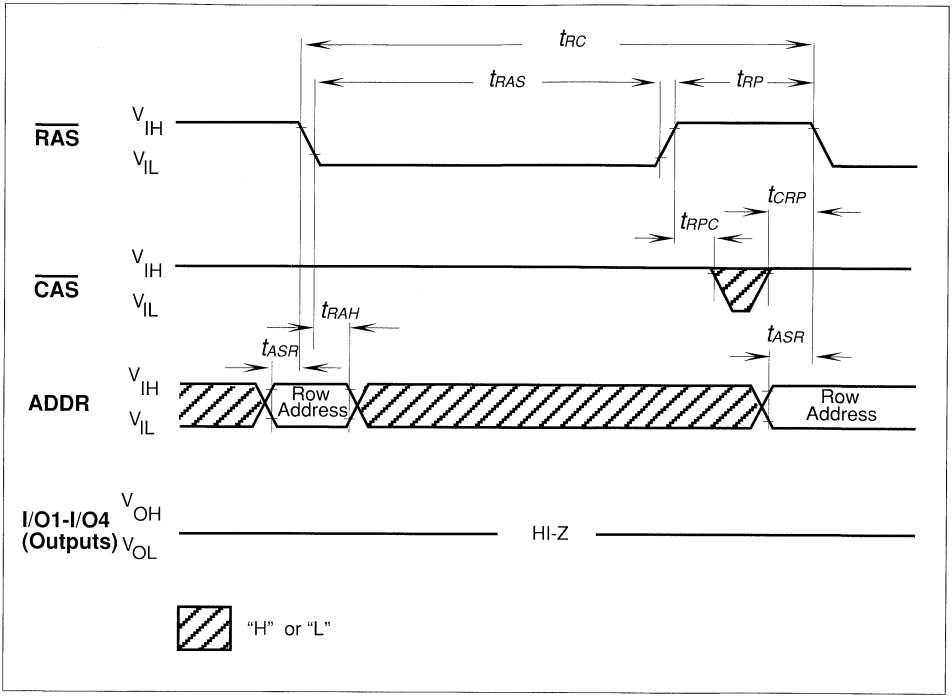
Fast Page Mode Read-Modify-Write Cycle



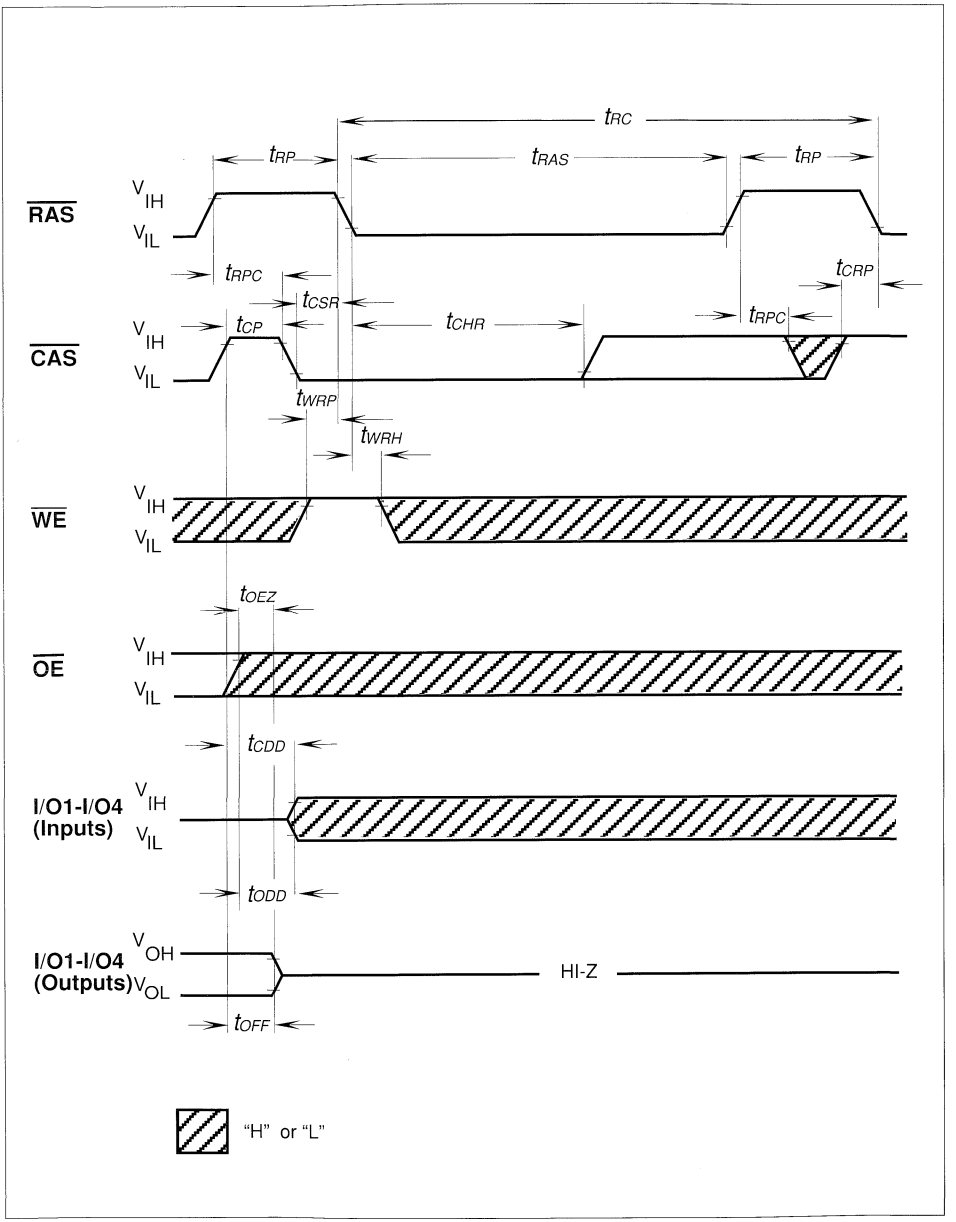
Fast Page Mode Read Cycle



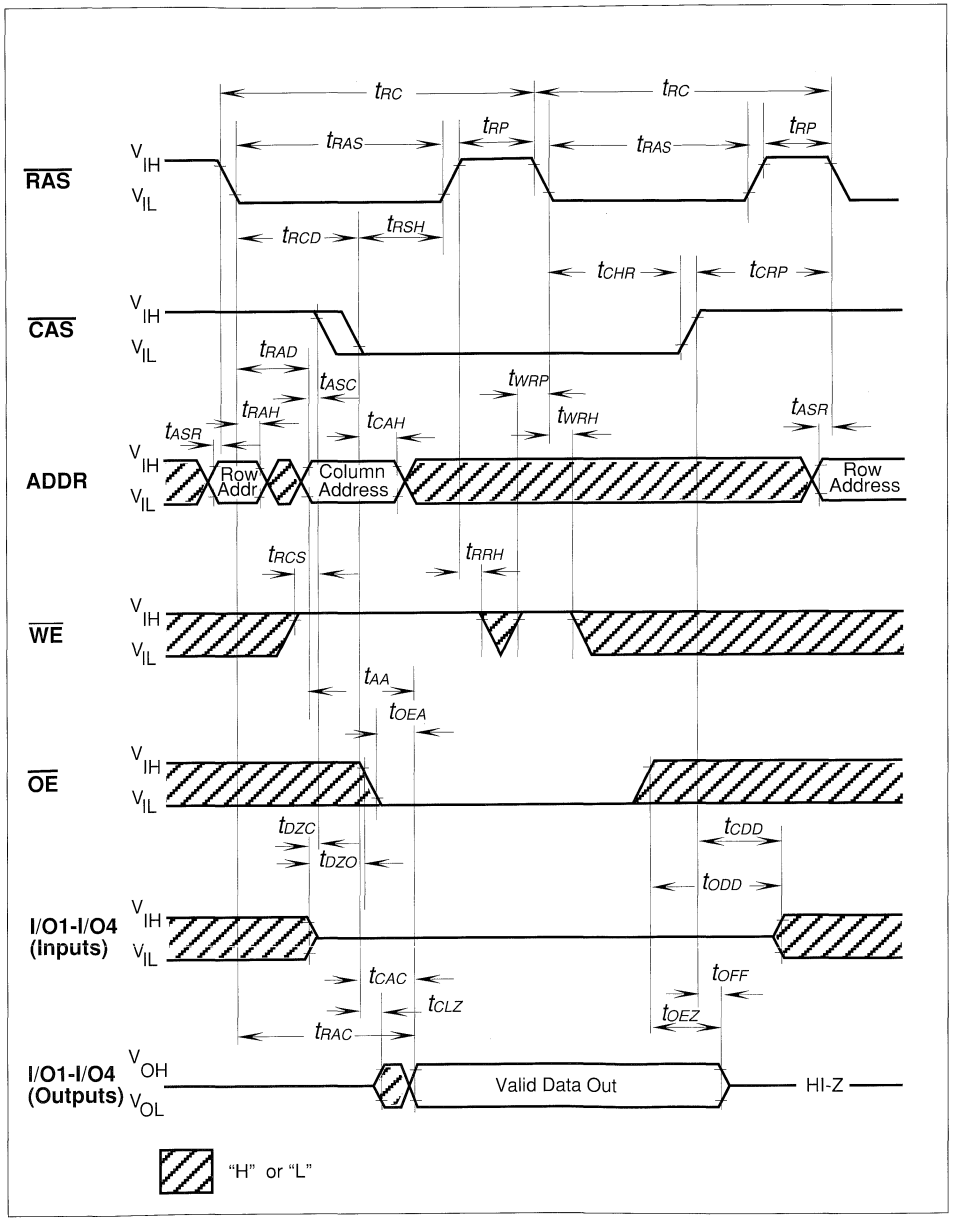
Fast Page Mode Early Write Cycle



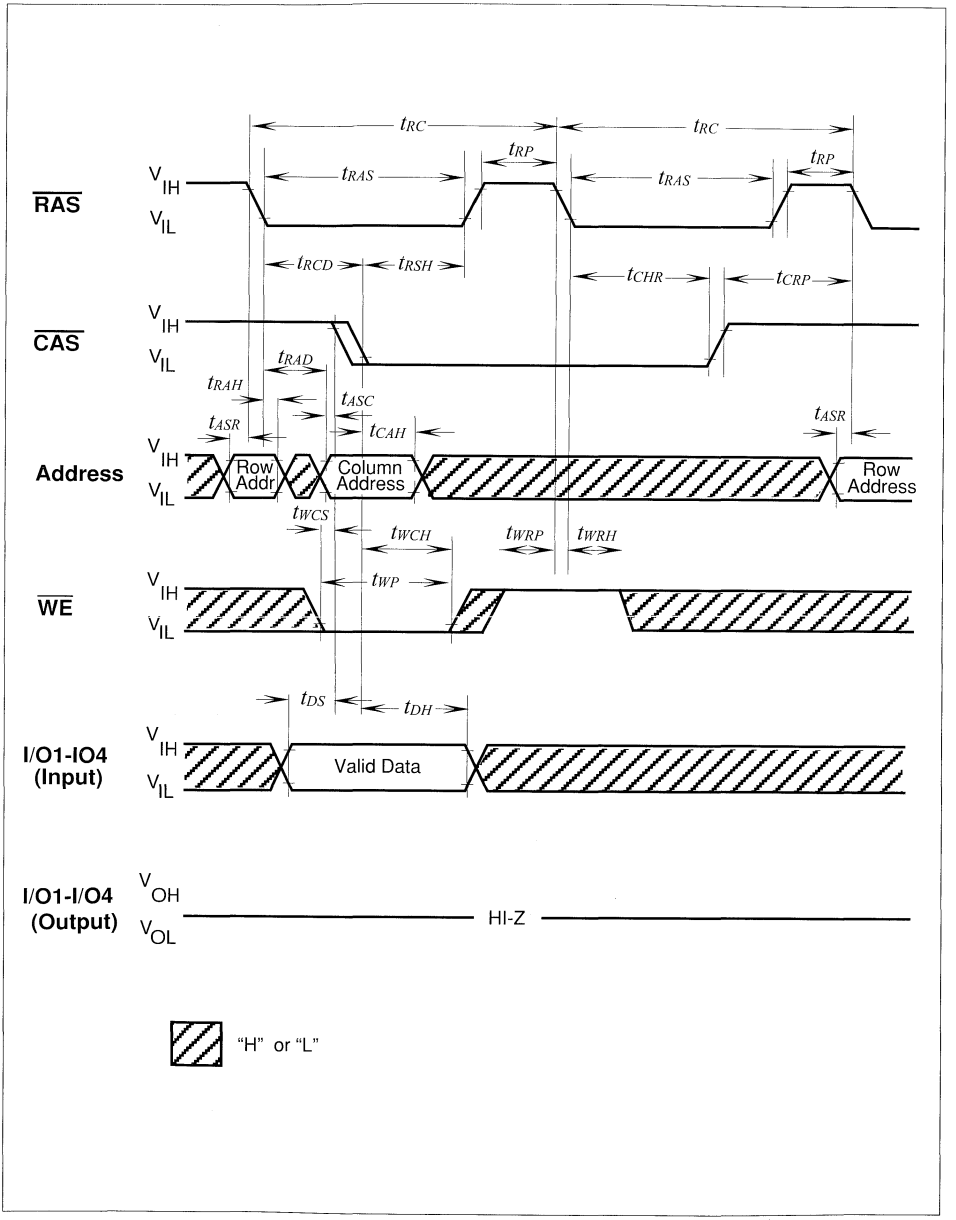
RAS-Only Refresh Cycle



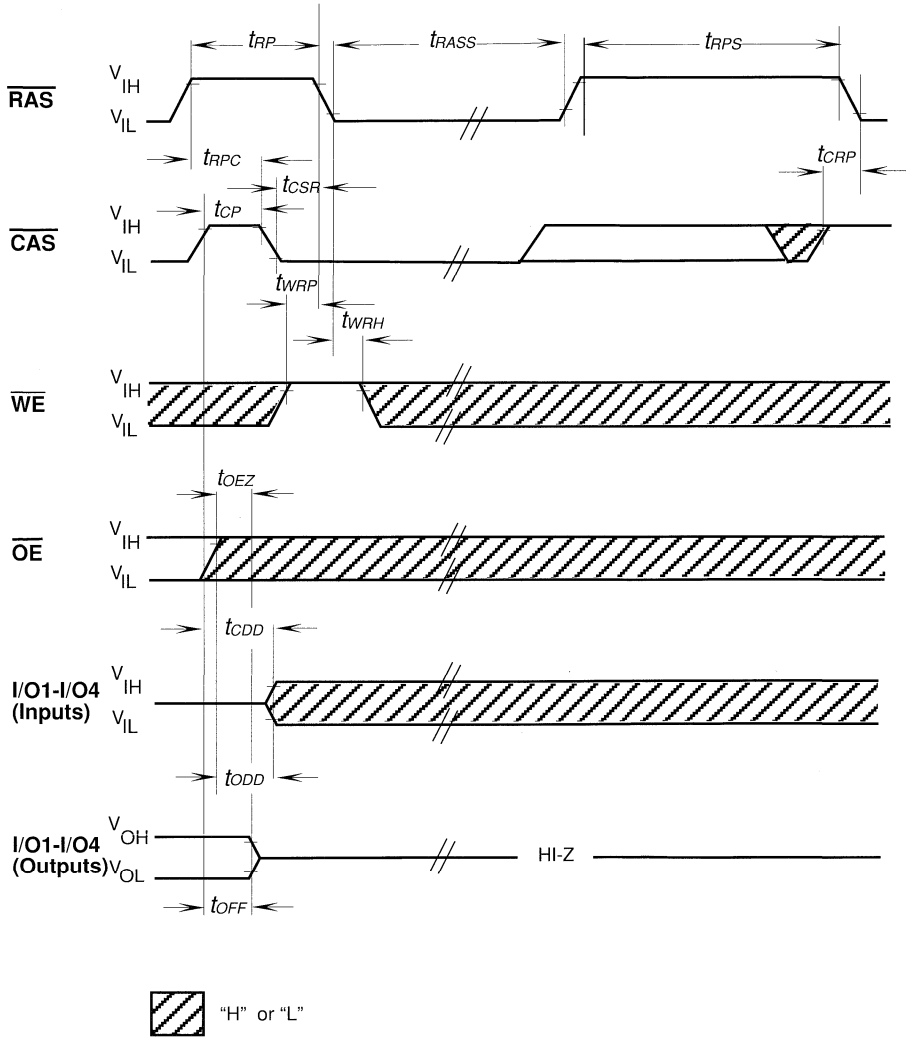
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



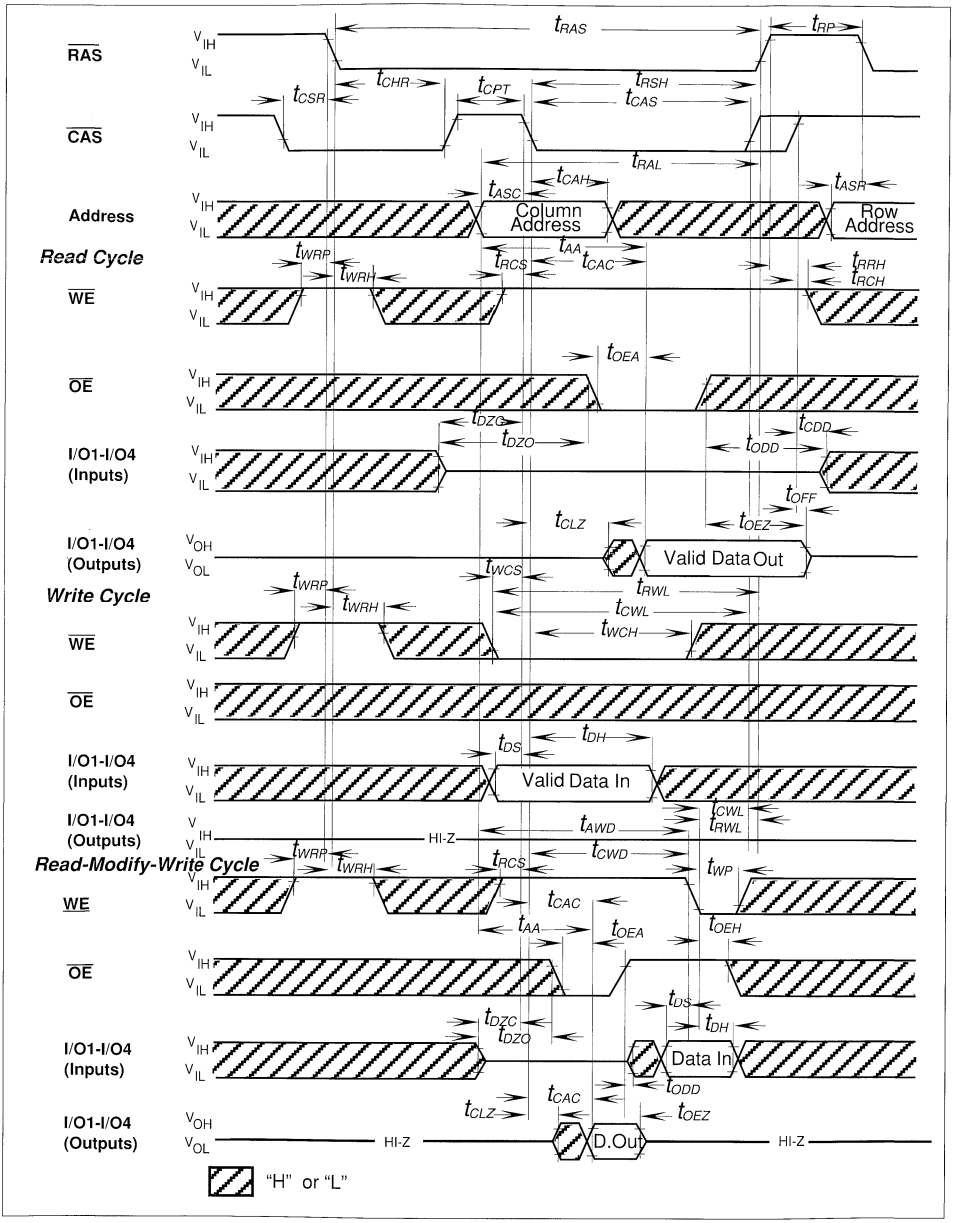
Hidden Refresh Cycle (Read)



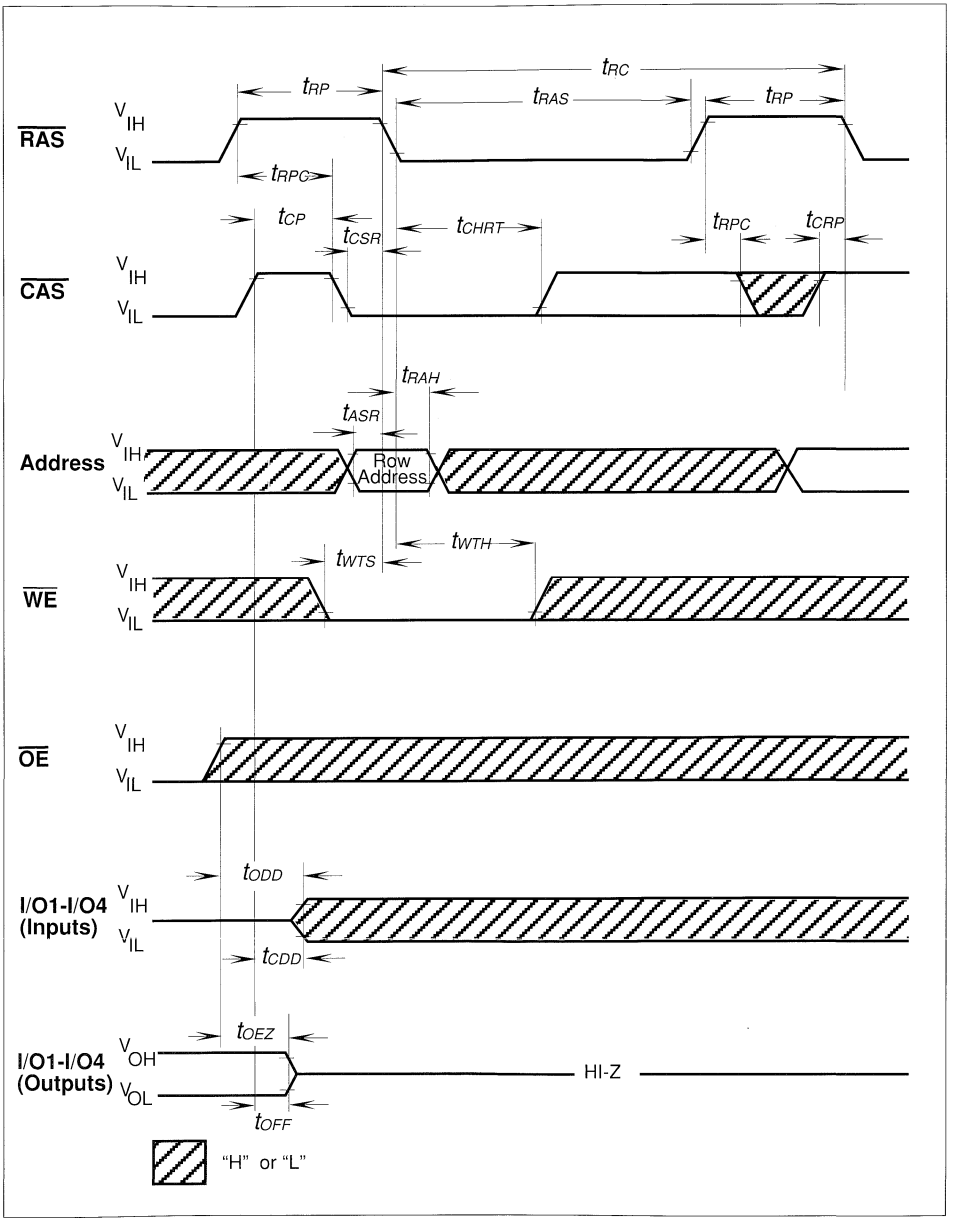
Hidden Refresh Cycle (Early Write)



Self Refresh



CAS-Before-RAS Refresh Counter Test Cycle



Test Mode Entry

4M x 4-Bit Dynamic RAM (3.3 V, 2k-refresh)

HYB 3117400BJ/BT -50/-60/-70

Preliminary Information

- 4 194 304 words by 4-bit organization
- 0 to 70 °C operating temperature
- Fast access and cycle time
  $\overline{RAS}$ access time:
  50 ns (-50 version)
  60 ns (-60 version)
  70 ns (-70 version)
  Cycle time:
  95 ns (-50 version)
  110 ns (-60 version)
  130 ns (-70 version)
  $\overline{CAS}$ access time:
  15 ns (-50,-60 version)
  20 ns (-70 version)
- Fast page mode cycle time
  35 ns (-50 version)
  40 ns (-60 version)
  45 ns (-70 version)
- Single + 3.3 V (± 0.3 V) supply
- Low power dissipation
  max. 396 active mW (-50 version)
  max. 363 active mW (-60 version)
  max. 330 active mW (-70 version)
  6.6 mW standby (TTL)
  3.3 mW standby (MOS)
- Output unlatched at cycle end allows two-dimensional chip selection
- Read, write, read-modify-write, $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, hidden refresh, Self Refresh and test mode
- Fast page mode capability
- All inputs, outputs and clocks fully TTL-compatible
- 2048 refresh cycles / 32 ms
- Plastic Package: P-SOJ-26/24-1 (300 mil)
  P-TSOPII-26/24-1 (300 mil)

Ordering Information

Type	Ordering Code	Package	Descriptions
HYB 3117400BJ-50	on request	P-SOJ-26/24-1 300 mil	DRAM (access time 50 ns)
HYB 3117400BJ-60	on request	P-SOJ-26/24-1 300 mil	DRAM (access time 60 ns)
HYB 3117400BJ-70	on request	P-SOJ-26/24-1 300 mil	DRAM (access time 70 ns)
HYB 3117400BT-50	on request	P-TSOPII-26/24-1 300 mil	DRAM (access time 50 ns)
HYB 3117400BT-60	on request	P-TSOPII-26/24-1 300 mil	DRAM (access time 60 ns)
HYB 3117400BT-70	on request	P-TSOPII-26/24-1 300 mil	DRAM (access time 70 ns)

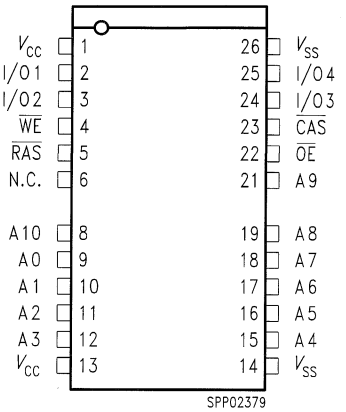
The HYB 3117400BJ/BT is the third generation dynamic RAM organized as 4194304 words by 4-bits. The HYB 3117400BJ/BT utilizes a submicron CMOS silicon gate process technology, as well as advanced circuit techniques to provide wide operating margins, both internally and for the system user. Multiplexed address inputs permit the HYB 3117400BJ/BT to be packaged in a standard SOJ-26/24 300 mil or TSOPII-26/24 300 mil wide plastic package. These packages provide high system bit densities and are compatible with commonly used automatic testing and insertion equipment. System-oriented features include single + 3.3 V (± 0.3 V) power supply, direct interfacing with high-performance logic device families.

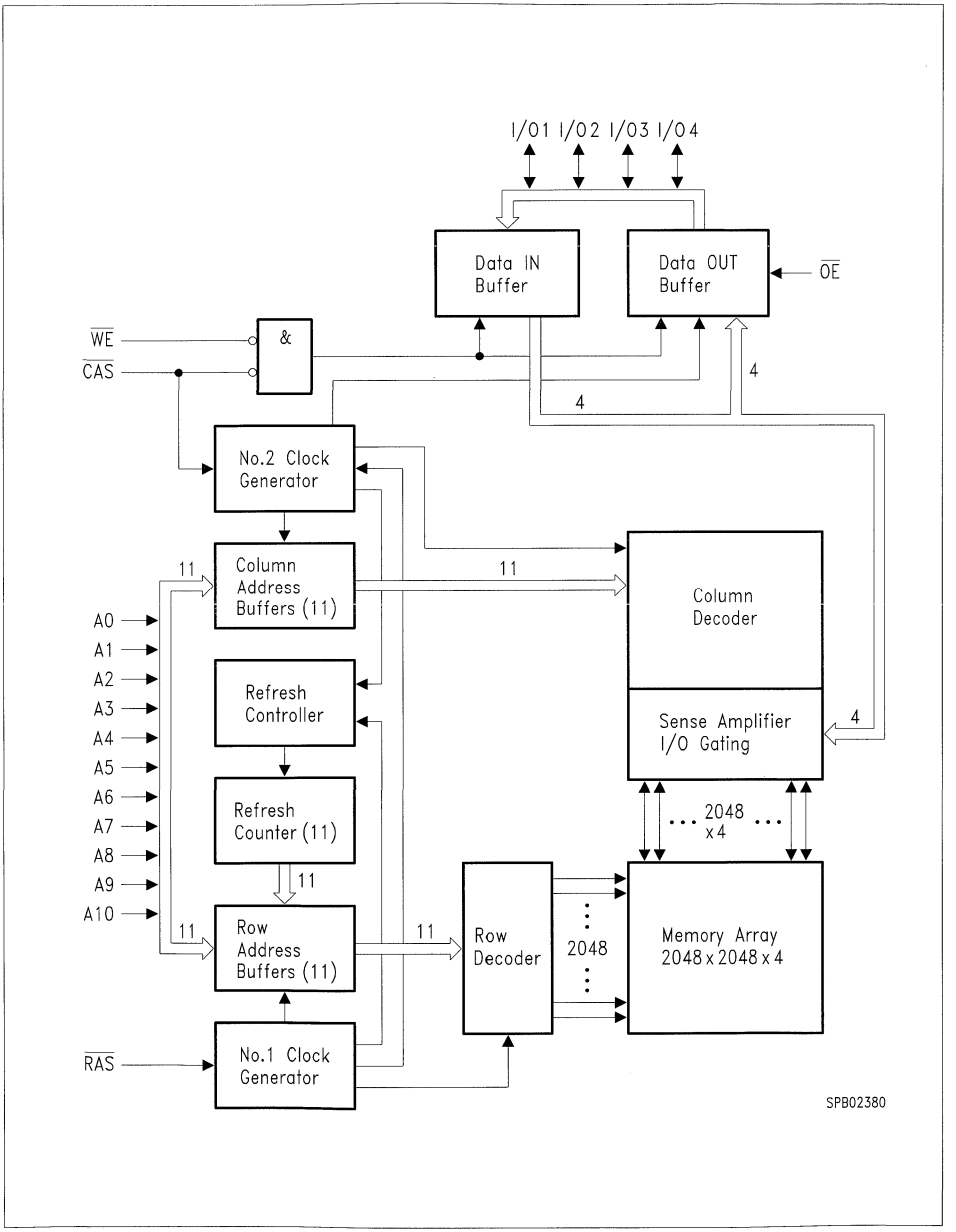
Pin Definitions and Functions

Pin No.	Function
A0 to A10	Row Address Inputs
A0 to A10	Column Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{OE}$	Output Enable
I/O1 - I/O4	Data Input/Output
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power Supply (+ 3.3 V)
V_{SS}	Ground (0 V)
N.C.	not connected

Pin Configuration
(top view)

P-SOJ-26/24-1 (300 mil)
P-TSOPII-26/24-1 (300 mil)





Block Diagram

Absolute Maximum Ratings

Operating temperature range ..... 0 to 70 °C
Storage temperature range ..... – 55 to 150 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 0.5 to min (V_{CC} + 0.5, 4.6) V
Power supply voltage ..... – 0.5 V to 4.6 V
Power dissipation ..... 0.5 W
Data out current (short circuit) ..... 50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 3.3 V ± 0.3 V, t_T = 5 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.0	V_{CC} + 0.5	V	1)
Input low voltage	V_{IL}	– 0.5	0.8	V	1)
TTL Output high voltage (I_{OUT} = – 2 mA)	V_{OH}	2.4	–	V	1)
TTL Output low voltage (I_{OUT} = 2 mA)	V_{OL}	–	0.4	V	1)
CMOS Output high voltage (I_{OUT} = – 100 uA)	V_{OH}	V_{CC} – 0.2	–	V	
CMOS Output low voltage (I_{OUT} = 100 uA)	V_{OL}	–	0.2	V	
Input leakage current (0 V ≤ V_{IH} ≤ V_{CC} + 0.3 V, all other pins = 0 V)	$I_{I(L)}$	– 10	10	µA	1)
Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ V_{CC} + 0.3 V)	$I_{O(L)}$	– 10	10	µA	1)
Average V_{CC} supply current:	I_{CC1}				
-50 ns version		–	120	mA	2) 3) 4)
-60 ns version		–	110	mA	2) 3) 4)
-70 ns version		–	100	mA	2) 3) 4)
($\overline{RAS}$, $\overline{CAS}$, address cycling, t_{RC} = $t_{RC\ min.}$)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	2	mA	–

DC Characteristics (cont'd)

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 3.3 V ± 0.3 V, t_T = 5 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current, during $\overline{RAS}$-only refresh cycles: -50 ns version	I_{CC3}	–	120	mA	2) 4)
-60 ns version		–	110	mA	2) 4)
-70 ns version		–	100	mA	2) 4)
($\overline{RAS}$ cycling: $\overline{CAS}$ = V_{IH}, t_{RC} = $t_{RC\ min.}$)					
Average V_{CC} supply current, during fast page mode: -50 ns version	I_{CC4}	–	90	mA	2) 3) 4)
-60 ns version		–	80	mA	2) 3) 4)
-70 ns version		–	70	mA	2) 3) 4)
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling, t_{PC} = t_{PC} min.)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	–	1	mA	1)
Average V_{CC} supply current, during $\overline{CAS}$-before-RAS refresh mode: -50 ns version	I_{CC6}	–	120	mA	2) 4)
-60 ns version		–	110	mA	2) 4)
-70 ns version		–	100	mA	2) 4)
($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min.)					
Average Self Refresh Current	I_{CC7}	–	1	mA	
(CBR cylce with t_{RAS} > t_{RASS} min., $\overline{CAS}$ held low, $\overline{WE}$ = V_{CC} – 0.2 V, Address and Din = V_{CC} – 0.2 V or 0.2 V)					

AC Characteristics [5]

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3 V, t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		HYB 3117400BJ/BT -50		HYB 3117400BJ/BT -60		HYB 3117400BJ/BT -70		
		min.	max.	min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	95	–	110	–	130	–	ns
Read-write cycle time	t_{RWC}	135	–	150	–	180	–	ns
Fast page mode cycle time	t_{PC}	35	–	40	–	45	–	ns
Fast page mode read-write cycle time	t_{PRWC}	75	–	80	–	95	–	ns
Access time from $\overline{RAS}$ [7) 12)]	t_{RAC}	–	50	–	60	–	70	ns
Access time from $\overline{CAS}$ [7) 12)]	t_{CAC}	–	15	–	15	–	20	ns
Access time from column address [7) 13)]	t_{AA}	–	25	–	30	–	35	ns
Access time from $\overline{CAS}$ precharge [7)]	t_{CPA}	–	30	–	35	–	40	ns
$\overline{CAS}$ to output in low-Z [7)]	t_{CLZ}	0	–	0	–	0	–	ns
Output buffer turn-off delay [8)]	t_{OFF}	0	15	0	15	0	20	ns
Transition time (rise and fall) [6)]	t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	35	–	40	–	50	–	ns
$\overline{RAS}$ pulse width	t_{RAS}	50	10k	60	10k	70	10k	ns
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	50	200k	60	200k	70	200k	ns
$\overline{CAS}$ precharge to $\overline{RAS}$ Delay	t_{RHCP}	30	–	35	–	40	–	ns
$\overline{CAS}$ precharge to $\overline{WE}$ (FPMR RMW)	t_{CPWD}	50	–	55	–	65	–	ns
$\overline{RAS}$ hold time	t_{RSH}	15		15	–	20	–	ns
$\overline{CAS}$ hold time	t_{CSH}	50		60	–	70	–	ns
$\overline{CAS}$ pulse width	t_{CAS}	15	10k	15	10k	20	10k	ns

AC Characteristics (cont'd) [5]

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3 V, t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		HYB 3117400BJ/BT -50		HYB 3117400BJ/BT -60		HYB 3117400BJ/BT -70		
		min.	max.	min.	max.	min.	max.	
$\overline{RAS}$ to $\overline{CAS}$ delay time [12]	t_{RCD}	20	35	20	45	20	50	ns
$\overline{RAS}$ to column address delay time [13]	t_{RAD}	15	25	15	30	15	35	ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	5	–	ns
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns
Row address hold time	t_{RAH}	10	–	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns
Column address hold time	t_{CAH}	10	–	15	–	15	–	ns
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	–	30	–	35	–	ns
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns
Read command hold time [9]	t_{RCH}	0	–	0	–	0	–	ns
Read command hold time referenced to $\overline{RAS}$ [9]	t_{RRH}	0	–	0	–	0	–	ns
Write command hold time	t_{WCH}	10	–	15	–	15	–	ns
Write command pulse width	t_{WP}	10	–	15	–	15	–	ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	–	15	–	20	–	ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	–	15	–	20	–	ns
Data setup time [10]	t_{DS}	0	–	0	–	0	–	ns

AC Characteristics (cont'd) [5]

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3 V, t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		HYB 3117400BJ/BT -50		HYB 3117400BJ/BT -60		HYB 3117400BJ/BT -70		
		min.	max.	min.	max.	min.	max.	
Data hold time [10]	t_{DH}	10	–	15	–	15	–	ns
Refresh period	t_{REF}	–	32	–	32	–	32	ms
Write command setup time [11]	t_{WCS}	0	–	0	–	0	–	ns
$\overline{CAS}$ to $\overline{WE}$ delay time [11]	t_{CWD}	35	–	35	–	45	–	ns
$\overline{RAS}$ to $\overline{WE}$ delay time [11]	t_{RWD}	70	–	80	–	95	–	ns
Column address to $\overline{WE}$ delay time [11]	t_{AWD}	45	–	50	–	60	–	ns
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CSR}	10	–	10	–	10	–	ns
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CHR}	10	–	10	–	10	–	ns
$\overline{CAS}$ hold time (Test mode entry cycle)	t_{CHRT}	30	–	30	–	30	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5	–	5	–	5	–	ns
$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ counter test cycle)	t_{CPT}	35	–	40	–	40	–	ns
Write command setup time (in test mode entry cycle)	t_{WTS}	10	–	10	–	10	–	ns
Write command hold time (in test mode entry cycle)	t_{WTH}	10	–	10	–	10	–	ns
Write to $\overline{RAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{WRP}	10	–	10	–	10	–	ns
Write hold time referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{WRH}	10	–	10	–	10	–	ns

AC Characteristics (cont'd) [5]

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3 V, t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		HYB 3117400BJ/BT -50		HYB 3117400BJ/BT -60		HYB 3117400BJ/BT -70		
		min.	max.	min.	max.	min.	max.	
$\overline{OE}$ command hold time	t_{OEH}	15	–	15	–	20	–	ns
$\overline{OE}$ access time	t_{OEA}	–	15	–	15	–	20	ns
Output buffer turn-off delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	ns
Data to $\overline{CAS}$ low delay [15]	t_{DZC}	0	–	0	–	0	–	ns
Data to $\overline{OE}$ low delay [15]	t_{DZO}	0	–	0	–	0	–	ns
$\overline{CAS}$ high to data delay [16]	t_{CDD}	15	–	15	–	20	–	ns
$\overline{OE}$ high to data delay [16]	t_{ODD}	15	–	15	–	20	–	ns
$\overline{RAS}$ pulse width during self refresh [17]	t_{RASS}	100	–	100	–	100	–	s
$\overline{RAS}$ precharge time during self refresh [17]	t_{RPS}	95	–	110	–	130	–	ns
$\overline{CAS}$ hold time during self refresh	t_{CHS}	– 50	–	– 50	–	– 50	–	ns

Capacitance

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3 V, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A10)	C_{I1}	–	5	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}	–	7	pF
I/O capacitance (I/O1 - I/O4)	C_{IO}	–	7	pF

Notes:

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.

4) Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{cc4} it can be changed once or less during a fast page mode cycle (t_{PC}).

5) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6) $V_{IH\ (min.)}$ and $V_{IL\ (max.)}$ are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.

7) Measured with a load equivalent to 100 pF and at V_{oh} = 2.0 V (I_{oh} = – 2mA), V_{ol} = 0.8 V (I_{ol} = 2 mA).

8) $t_{OFF\ (max.)}$ and $t_{OEZ\ (max.)}$ define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.

9) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

10) These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.

11) t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS\ (min.)}$, the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} \geq t_{RWD\ (min.)}$, $t_{CWD} \geq t_{CWD\ (min.)}$, $t_{AWD} > t_{AWD\ (min.)}$ and $t_{CPWD} \geq t_{CPWD\ (min.)}$, the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.

12) Operation within the $t_{RCD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RCD\ (max.)}$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD\ (max.)}$ limit, then access time is controlled by t_{CAC}.

13) Operation within the $t_{RAD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RAD\ (max.)}$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD\ (max.)}$ limit, then access time is controlled by t_{AA}.

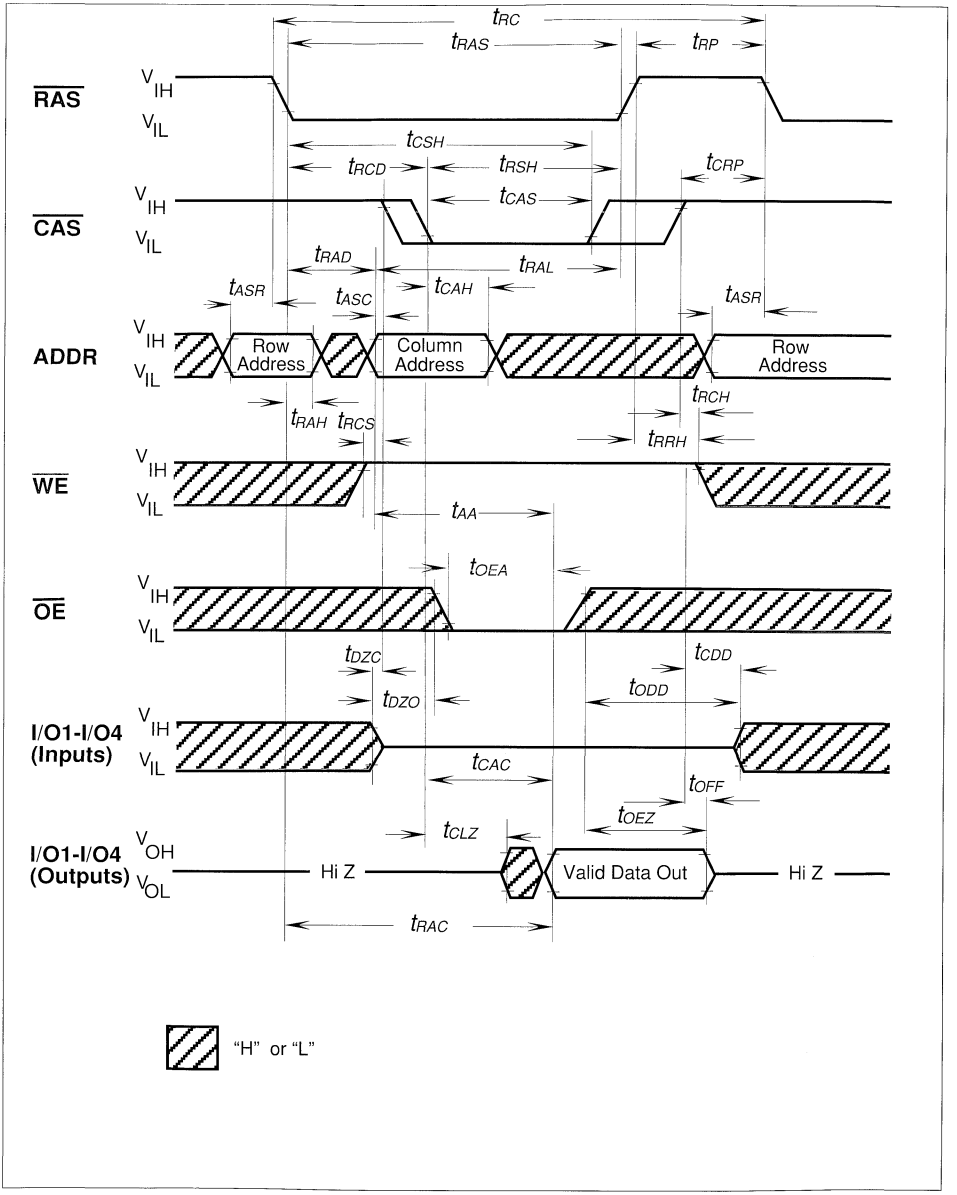
14) AC measurements assume t_T = 5 ns.

15) Either t_{DZC} or t_{DZO} must be satisfied.

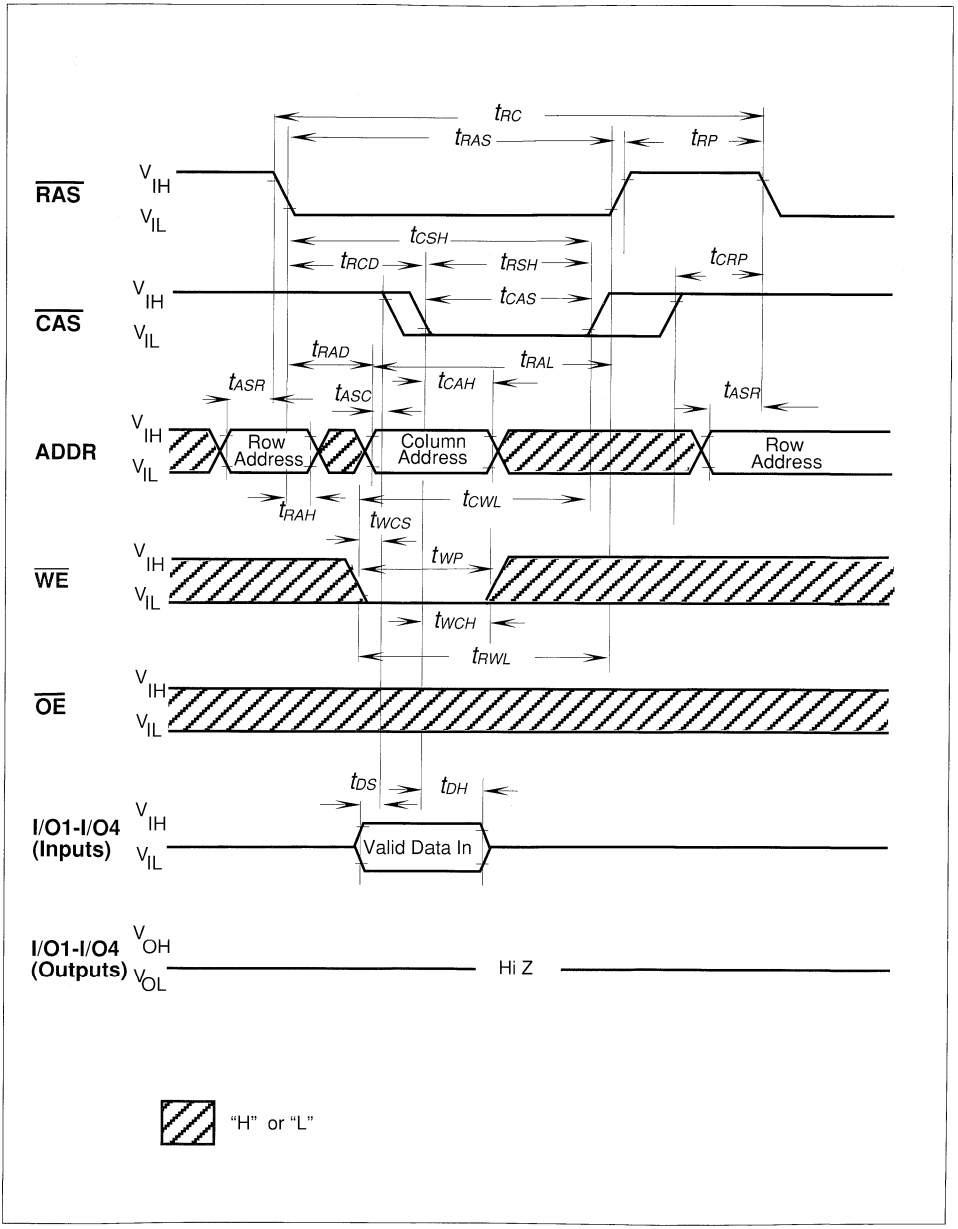
16) Either t_{CDD} or t_{ODD} must be satisfied.

17) Self Refresh occurs when a CBR cycle is initiated which $\overline{RAS}$ and $\overline{CAS}$ are kept active for an indefinite time that exceeds the DRAM active specification. The part then will internally cycle through all refresh addresses at a rate defined by the internal design of the part. The mode is exited by $\overline{RAS}$ going inactive.

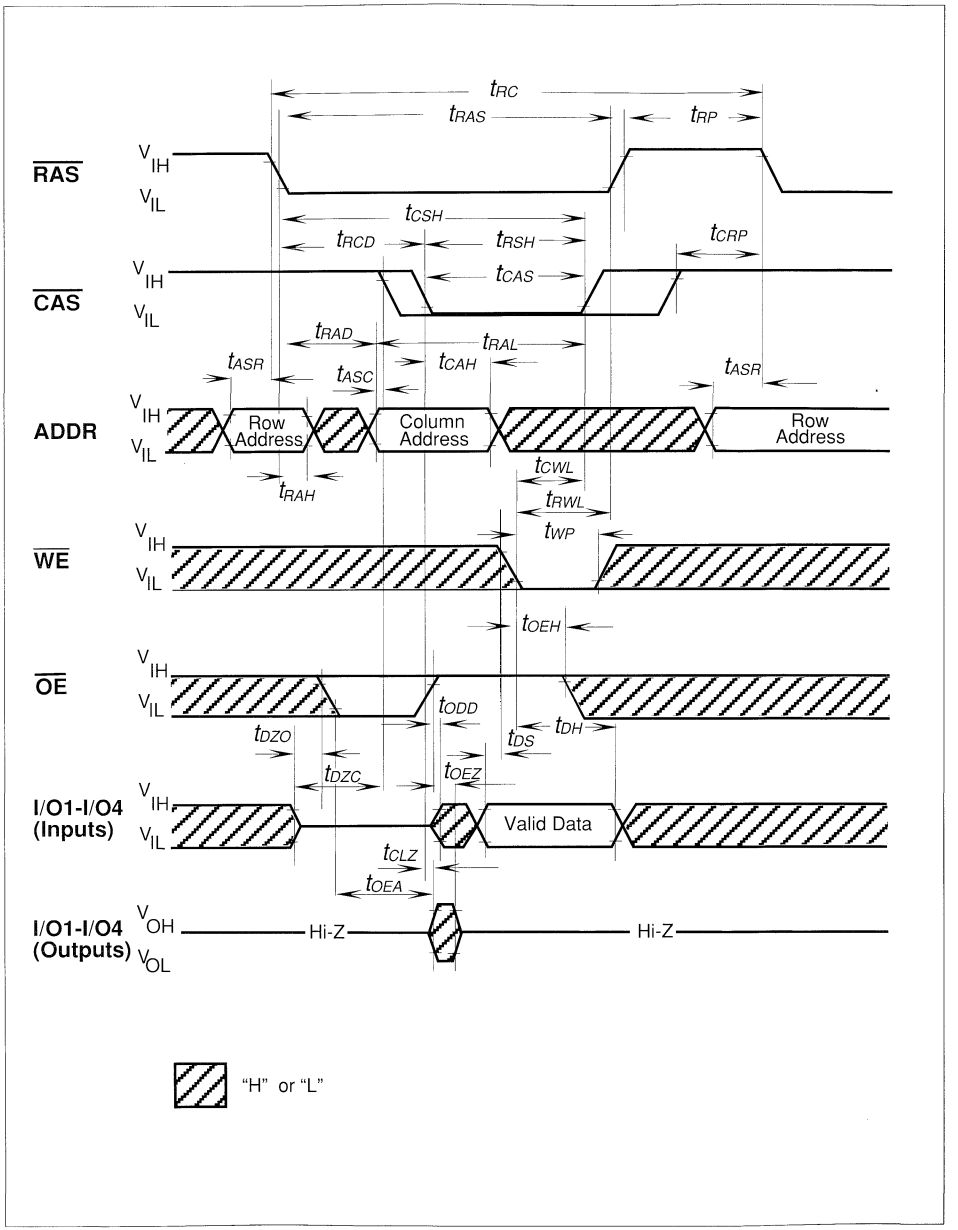
Waveforms



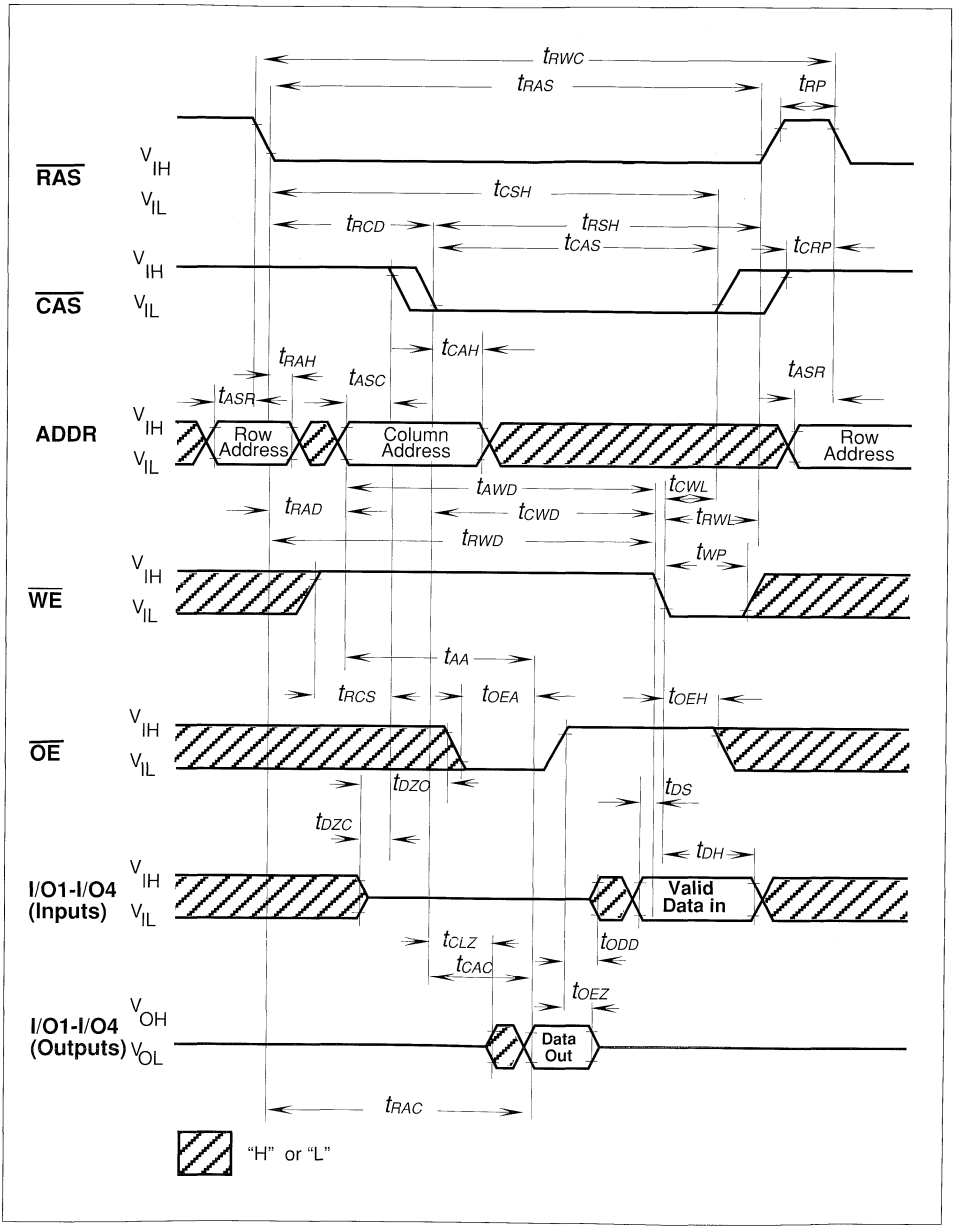
Read Cycle



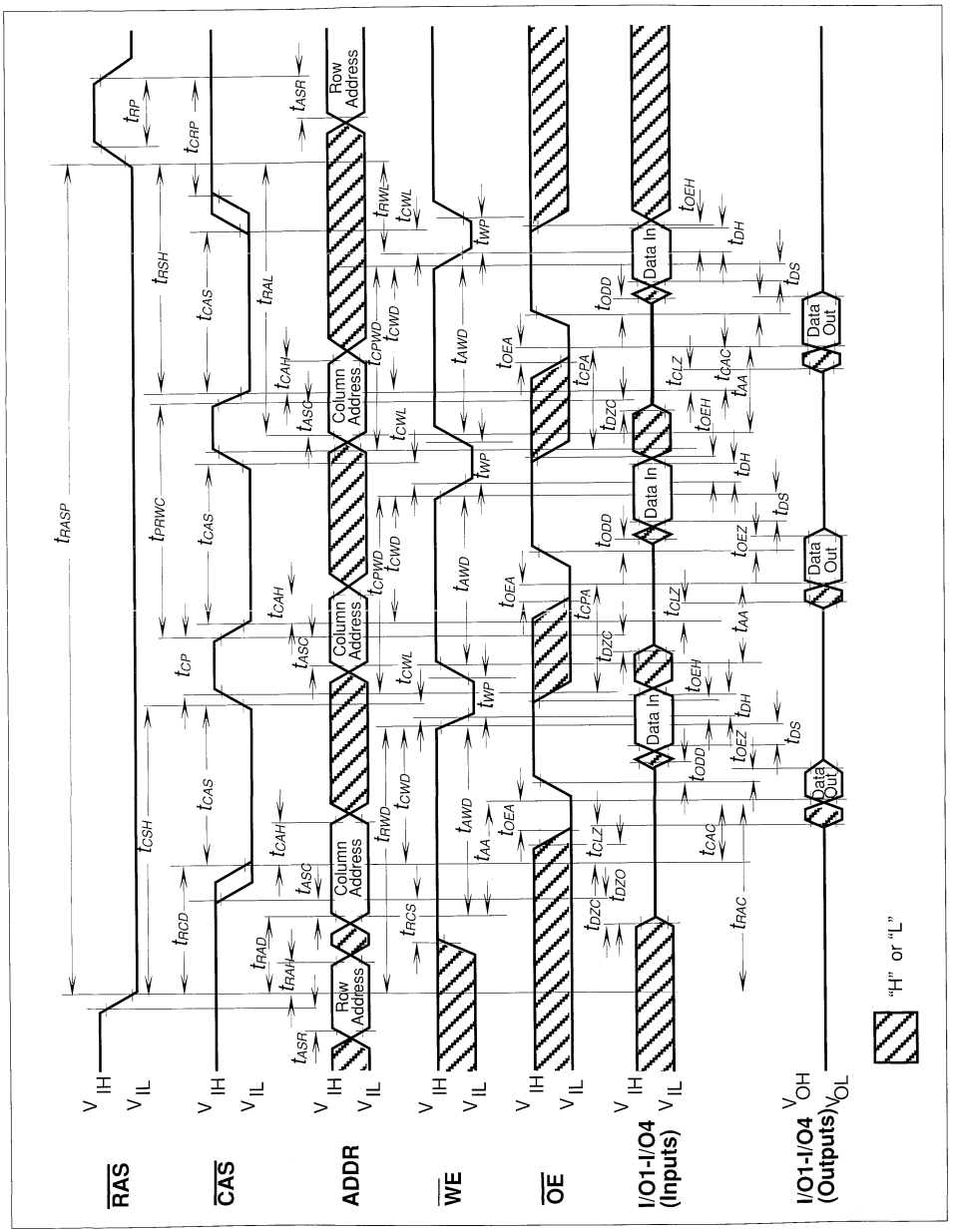
Write Cycle (Early Write)



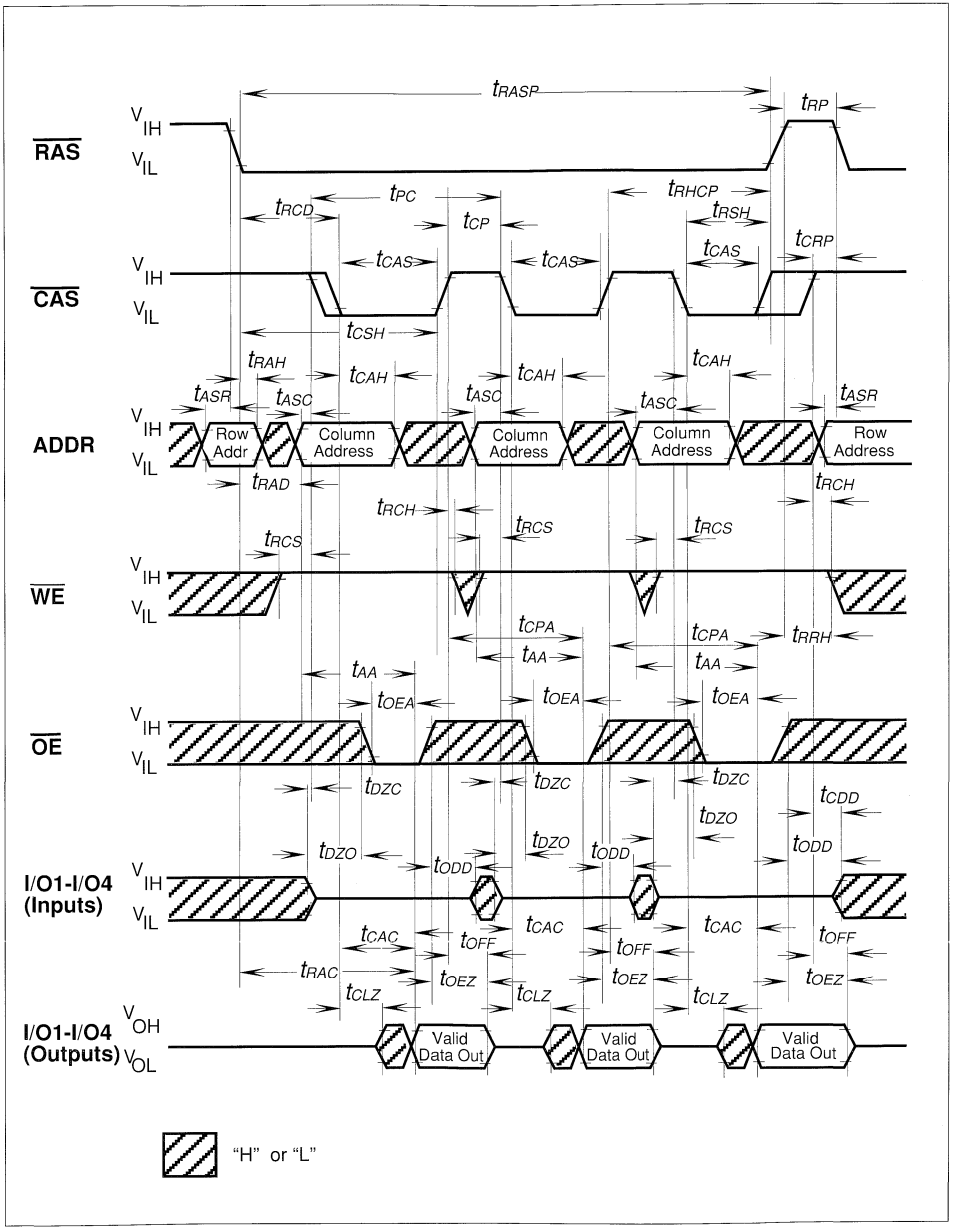
Write Cycle ($\overline{OE}$ Controlled Write)



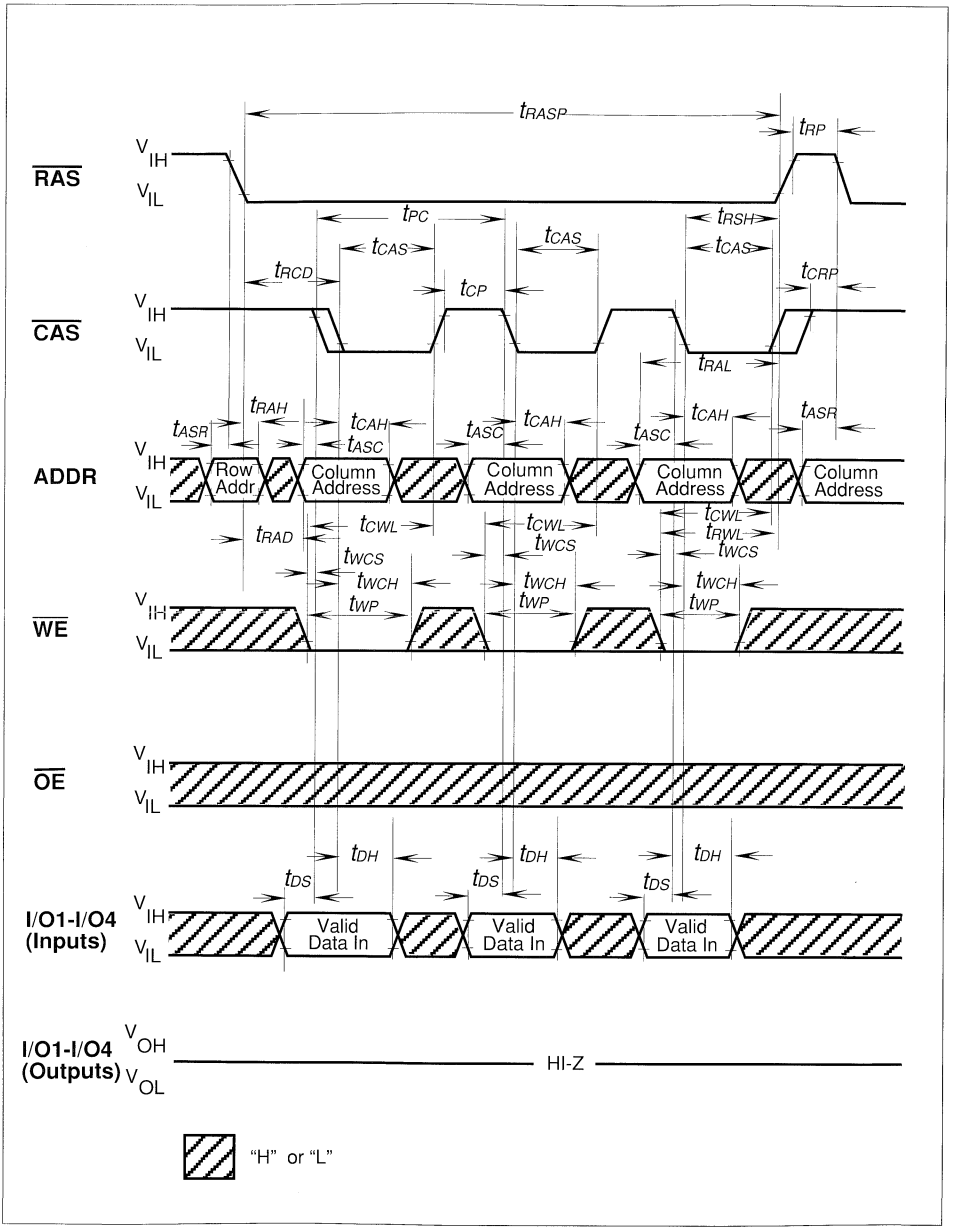
Read-Write (Read-Modify-Write) Cycle



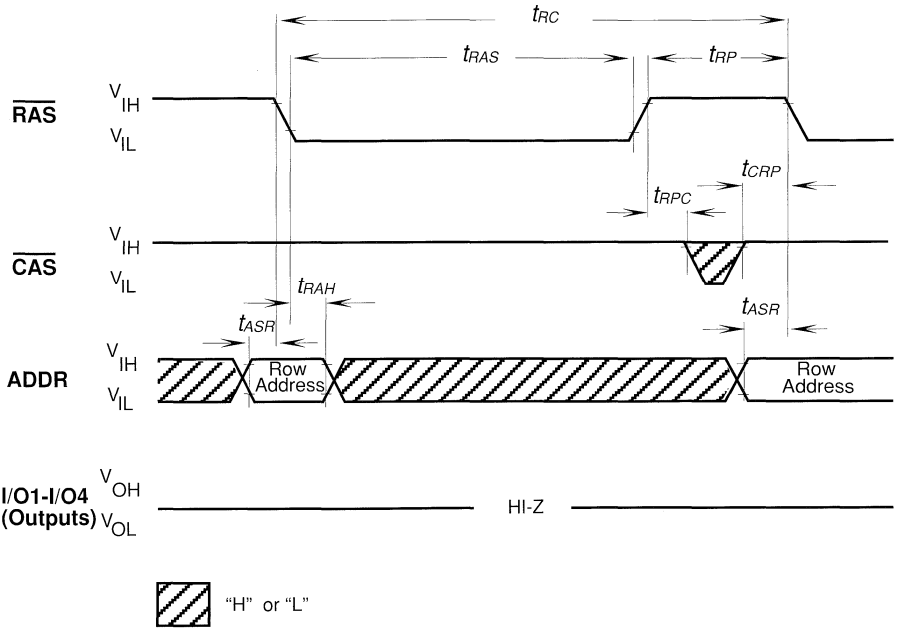
Fast Page Mode Read-Modify-Write Cycle



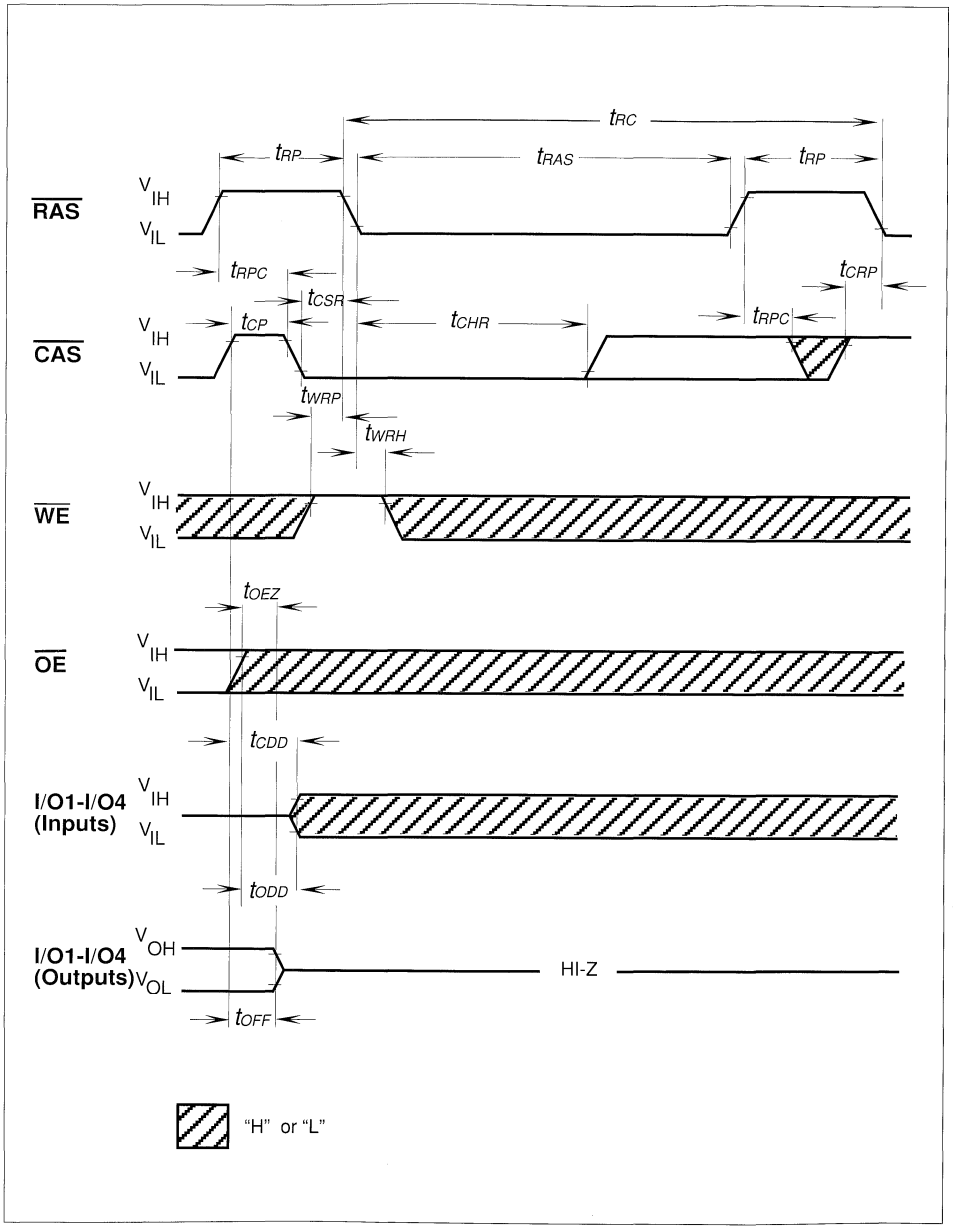
Fast Page Mode Read Cycle



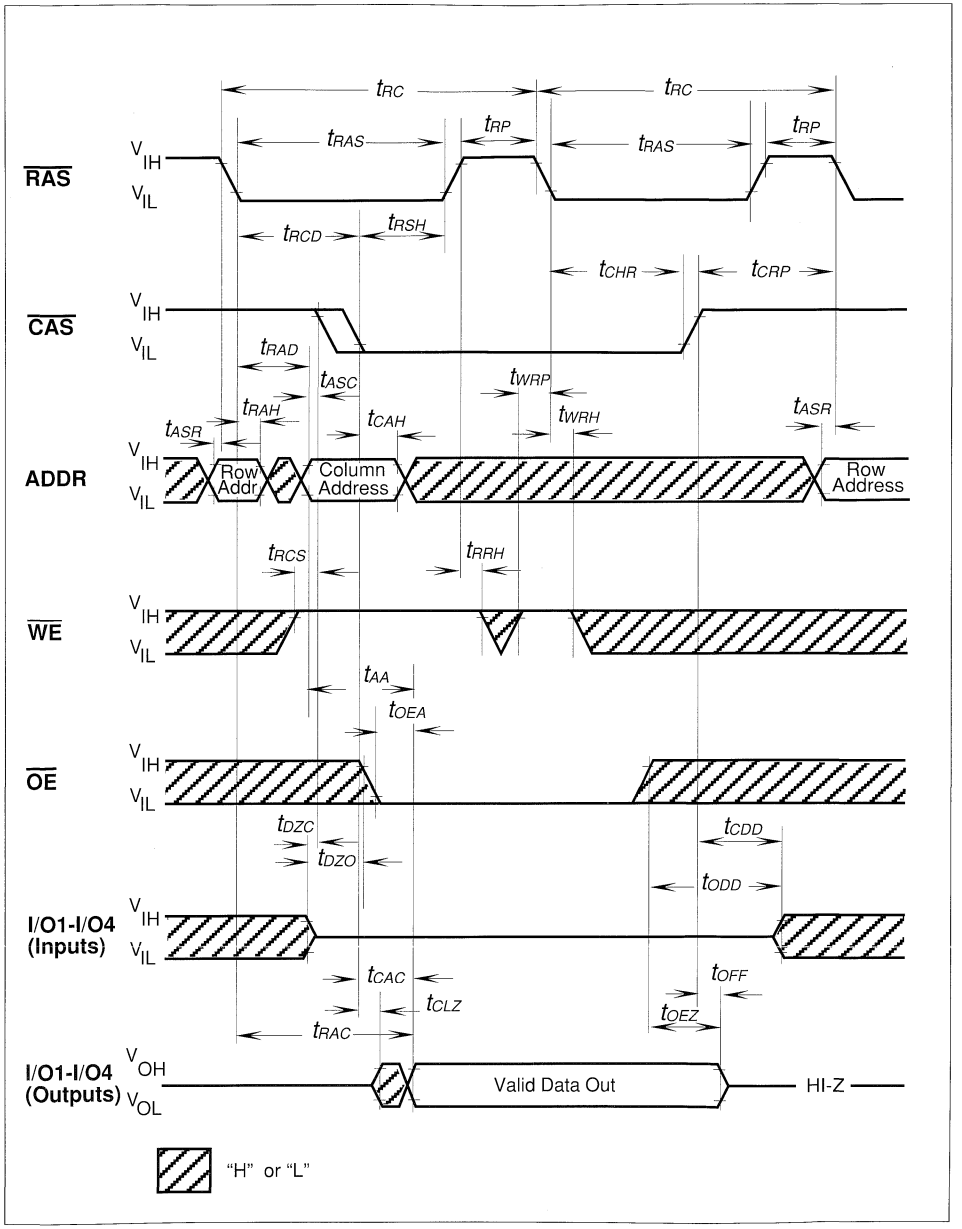
Fast Page Mode Early Write Cycle



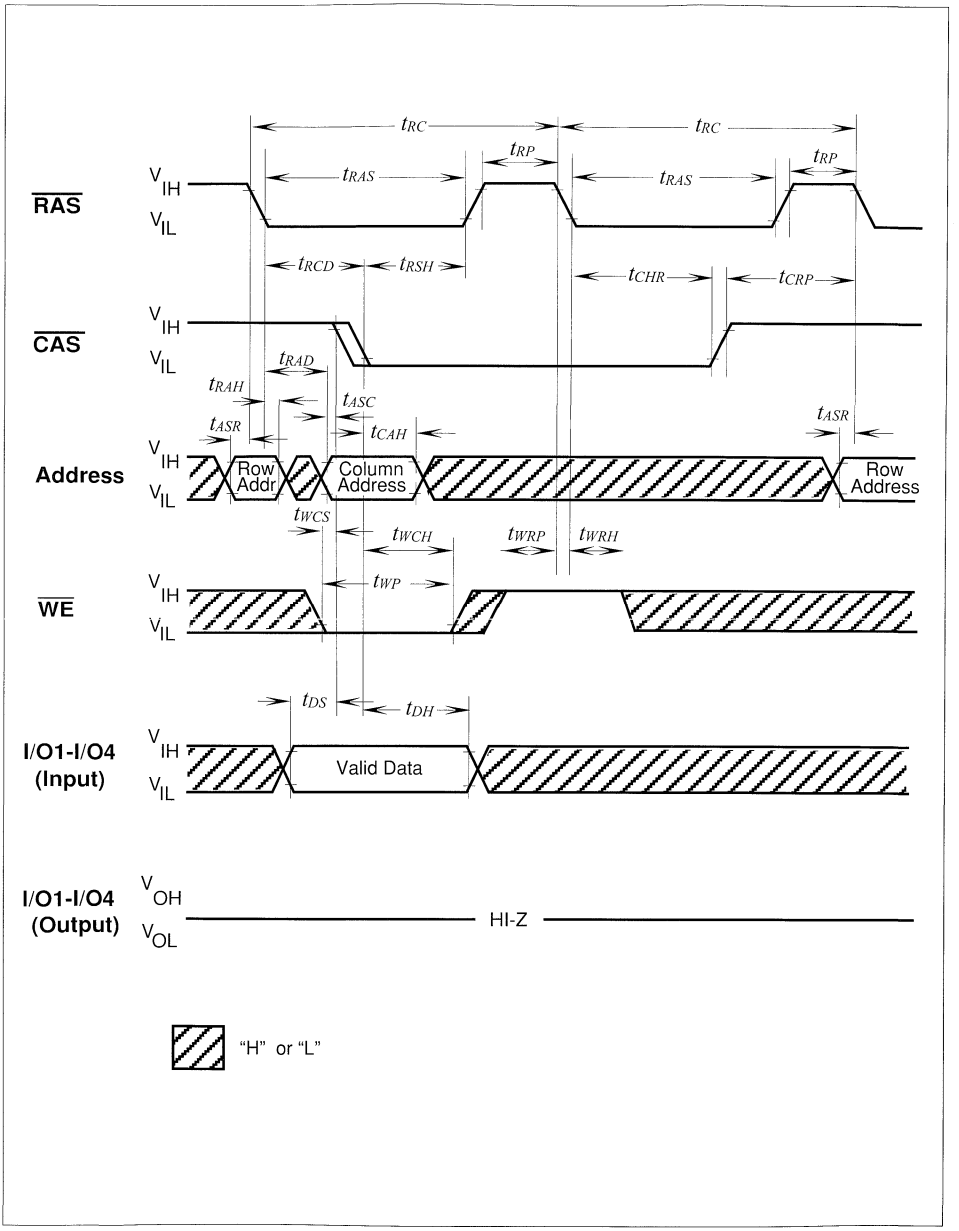
$\overline{RAS}$-Only Refresh Cycle



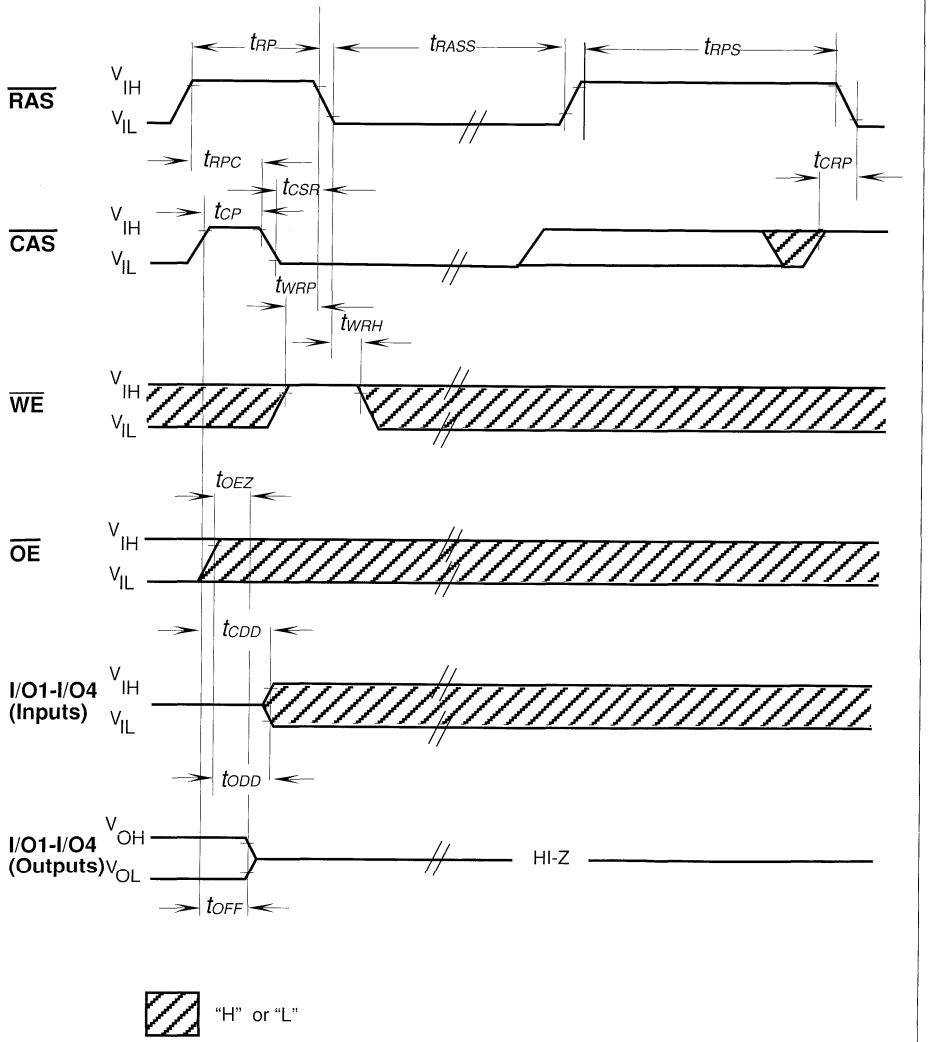
CAS-Before-RAS Refresh Cycle



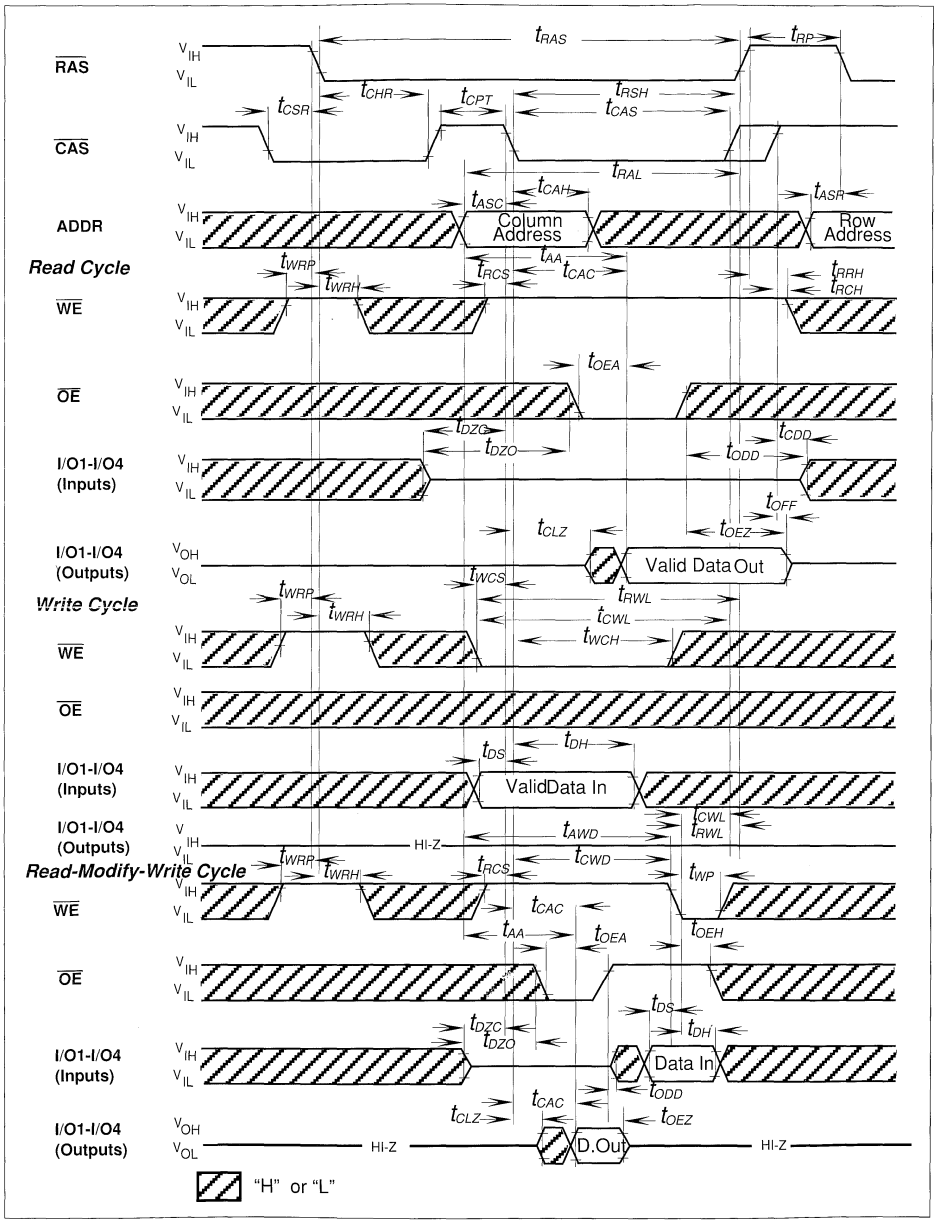
Hidden Refresh Cycle (Read)



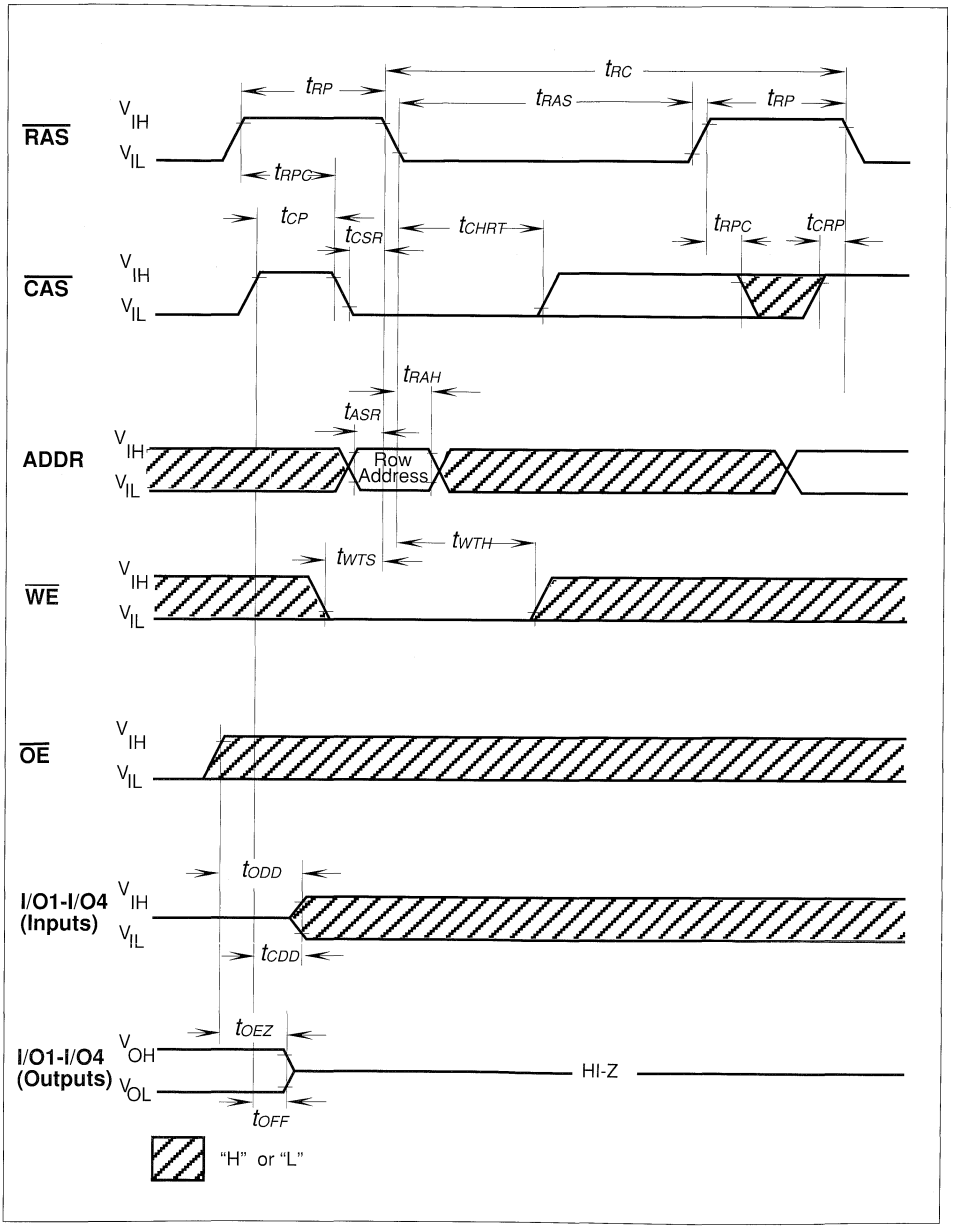
Hidden Refresh Cycle (Early Write)



Self Refresh



CAS-Before-RAS Refresh Counter Test Cycle



Test Mode Entry

4M x 4-Bit Dynamic RAM
2k & 4k Refresh
(Hyper Page Mode - EDO)

HYB 5116405BJ/BT -50/-60/-70
HYB 5117405BJ/BT -50/-60/-70

Preliminary Information

- 4 194 304 words by 4-bit organization
- 0 to 70 °C operating temperature
- Fast access and cycle time
  RAS access time:
  50 ns (-50 version)
  60 ns (-60 version)
  70 ns (-70 version)
  Cycle time:
  89 ns (-50 version)
  104 ns (-60 version)
  124 ns (-70 version)
  CAS access time:
  12 ns (-50 version)
  15 ns (-60 version)
  20 ns (-70 version)
- Hyper page mode (EDO) cycle time
  20 ns (-50 version)
  25 ns (-60 version)
  30 ns (-70 version)
- Single + 5 V (± 10 %) supply
- Low power dissipation
  max. 550 mW active
  (HYB 5116405BJ/BT-50)
  max. 660 mW active
  (HYB 5117405BJ/BT-50)
  max. 605 mW active
  (HYB 5117405BJ/BT-60)
  max. 550 mW active
  (HYB 5117405BJ/BT-70)
  11 mW standby (TTL)
  5.5 mW standby (MOS)
- Output unlatched at cycle end allows two-dimensional chip selection
- Read, write, read-modify-write, CAS-before-RAS refresh, RAS-only refresh, hidden refresh, Self Refresh and test mode
- Hyper page mode (EDO) capability
- All inputs, outputs and clocks fully TTL-compatible
- 4096 refresh cycles / 64 ms for HYB5116405BJ/BT (4k-Refresh)
- 2048 refresh cycles / 32 ms for HYB5117405BJ/BT (2k-Refresh)
- Plastic Package: P-SOJ-26/24 300 mil
  P TSOPII-26/24 300 mil

Ordering Information

Type	Ordering Code	Package	Descriptions
HYB 5116405BJ-50	Q67100-Q1098	P-SOJ-26/24-1 300 mil	DRAM (access time 50 ns)
HYB 5116405BJ-60	Q67100-Q1099	P-SOJ-26/24-1 300 mil	DRAM (access time 60 ns)
HYB 5116405BJ-70	Q67100-Q1100	P-SOJ-26/24-1 300 mil	DRAM (access time 70 ns)
HYB 5116405BT-50	on request	P-TSOPII-26/24-1 300mil	DRAM (access time 50 ns)
HYB 5116405BT-60	on request	P-TSOPII-26/24-1 300mil	DRAM (access time 60 ns)
HYB 5116405BT-70	on request	P-TSOPII-26/24-1 300mil	DRAM (access time 70 ns)
HYB 5117405BJ-50	Q67100-Q1101	P-SOJ-26/24-1 300 mil	DRAM (access time 50 ns)
HYB 5117405BJ-60	Q67100-Q1102	P-SOJ-26/24-1 300 mil	DRAM (access time 60 ns)
HYB 5117405BJ-70	Q67100-Q1103	P-SOJ-26/24-1 300 mil	DRAM (access time 70 ns)
HYB 5117405BT-50	on request	P-TSOPII-26/24-1 300mil	DRAM (access time 50 ns)
HYB 5117405BT-60	on request	P-TSOPII-26/24-1 300mil	DRAM (access time 60 ns)
HYB 5117405BT-70	on request	P-TSOPII-26/24-1 300mil	DRAM (access time 70 ns)

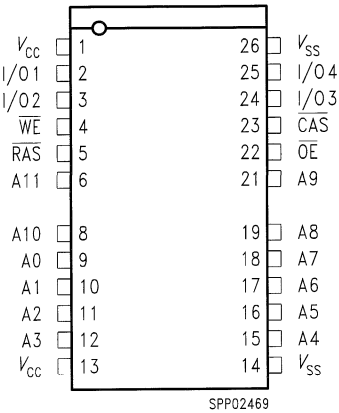
The HYB 5116(7)405BJ/BT is the new generation dynamic RAM organized as 4194304 words by 4-bits. The HYB 5116(7)405BJ/BT utilizes a submicron CMOS silicon gate process technology, as well as advanced circuit techniques to provide wide operating margins, both internally and for the system user. Multiplexed address inputs permit the HYB 5116(7)405BJ/BT to be packaged in a standard SOJ 26/24 or TSOPII-26/24 plastic package, both with 300 mil width. These packages provide high system bit densities and are compatible with commonly used automatic testing and insertion equipment. System-oriented features include single + 5 V (± 10 %) power supply, direct interfacing with high-performance logic device families such as Schottky TTL.

Pin Definitions and Functions

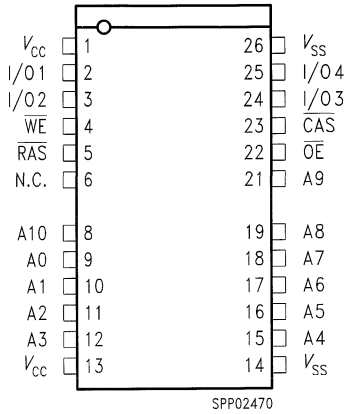
Pin No.	Function
A0-A11	Row Address Inputs for HYB5116405
A0-A9	Column Address Inputs for HYB5116405
A0-A10	Row and Column Address Inputs for HYB5117405
$\overline{RAS}$	Row Address Strobe
$\overline{OE}$	Output Enable
I/O1-I/O4	Data Input/Output
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground (0 V)
N.C.	not connected

Pin Configuration
(top view)

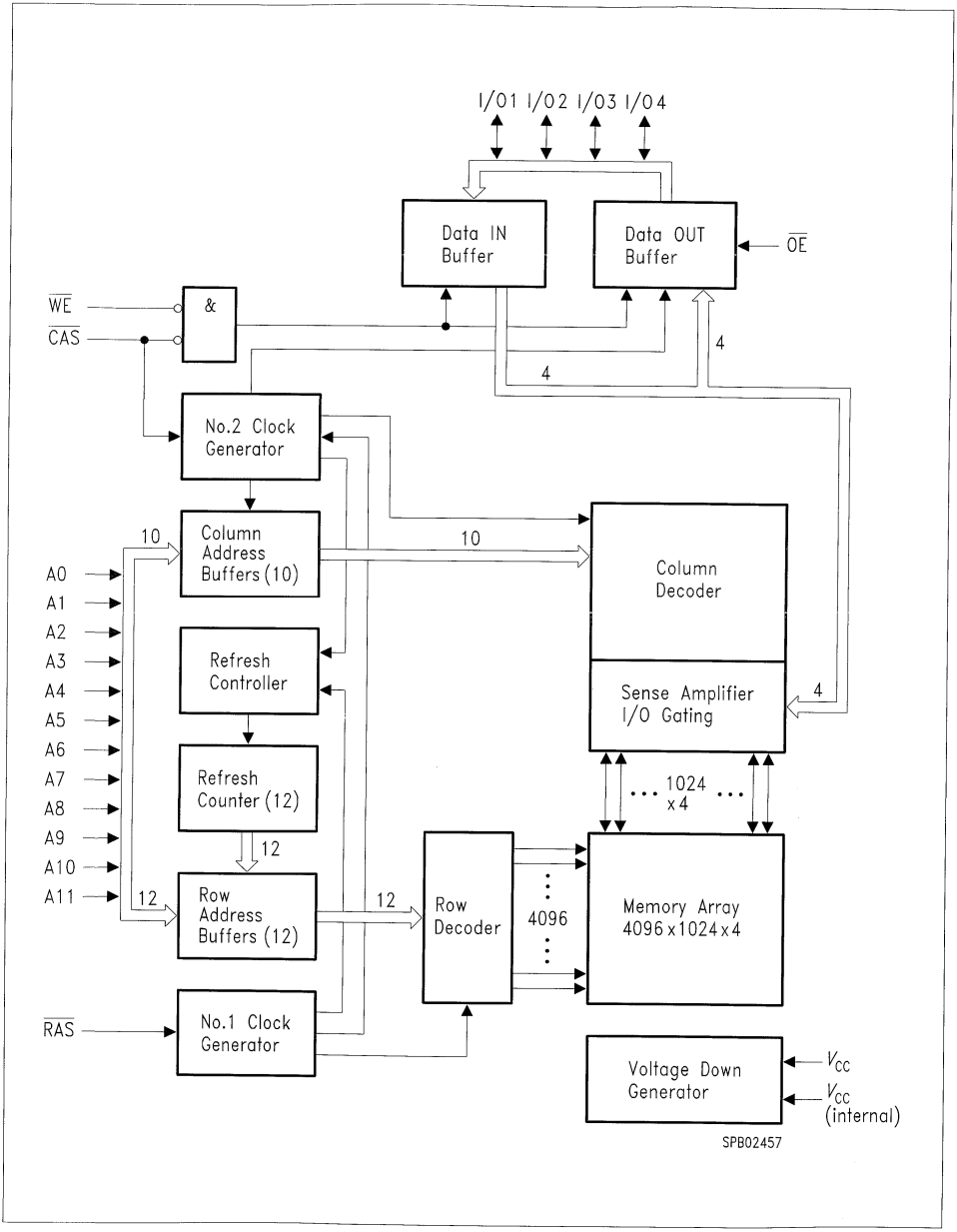
P-SOJ-26/24 300 mil
P-TSOPII-26/24 300 mil



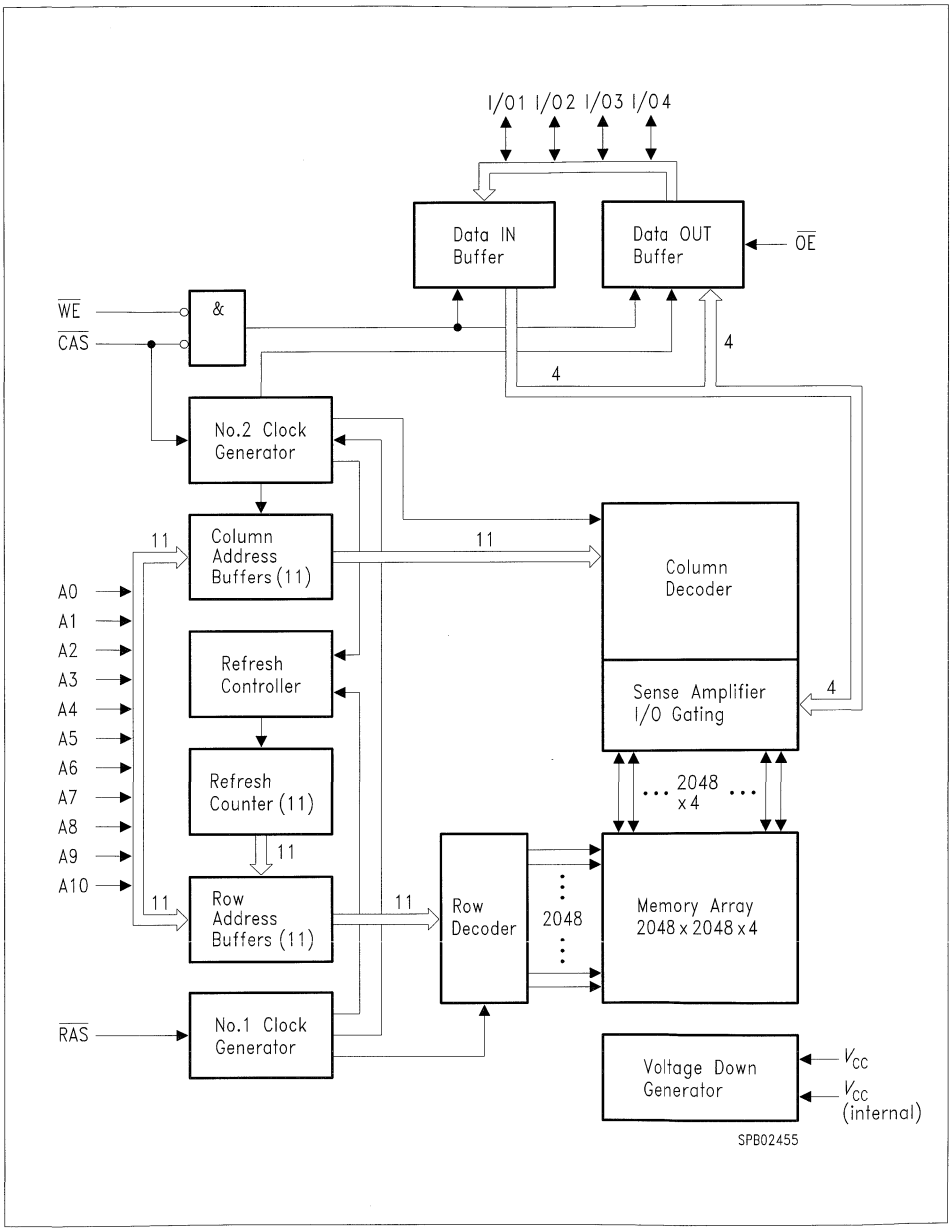
HYB 5116405 BJ/BT



HYB 5117405 BJ/BT



Block Diagram for HYB 5116405



Block Diagram for HYB 5117405 BJ/BT

Absolute Maximum Ratings

Operating temperature range ..... 0 to 70 °C
Storage temperature range ..... – 55 to 150 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 0.5 to min (V_{CC} + 0.5, 7.0) V
Power supply voltage ..... – 1.0 V to 7.0 V
Power dissipation ..... 1.0 W
Data out current (short circuit) ..... 50 mA

Note:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics (note : values in brackets for HYB 5117405 BJ/BT)
T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 5 V ± 10 %; t_T = 2 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	V_{CC} + 0.5	V	1)
Input low voltage	V_{IL}	– 0.5	0.8	V	1)
Output high voltage (I_{OUT} = – 5 mA)	V_{OH}	2.4	–	V	1)
Output low voltage (I_{OUT} = 4.2 mA)	V_{OL}	–	0.4	V	1)
Input leakage current (0 V ≤ V_{IH} ≤ V_{CC} + 0.3 V, all other pins = 0 V)	$I_{I(L)}$	– 10	10	µA	1)
Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ V_{CC} + 0.3 V)	$I_{O(L)}$	– 10	10	µA	1)
Average V_{CC} supply current:	I_{CC1}				
-50 ns version		–	100(120)	mA	2) 3) 4)
-60 ns version		–	90 (110)	mA	2) 3) 4)
-70 ns version		–	80 (100)	mA	2) 3) 4)
($\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = t_{RC} min.)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	2	mA	–
Average V_{CC} supply current, during $\overline{RAS}$-only refresh cycles:	I_{CC3}				
-50 ns version		–	100(120)	mA	2) 4)
-60 ns version		–	90 (110)	mA	2) 4)
-70 ns version		–	80 (100)	mA	2) 4)
($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)					

DC Characteristics (note : values in brackets for HYB 5117405 BJ/BT) (cont'd)
T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 5 V ± 10 %; t_T = 2 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current, during hyper page mode: -50 ns version	I_{CC4}	–	85 (90)	mA	2) 3) 4)
-60 ns version		–	75 (80)	mA	2) 3) 4)
-70 ns version		–	65 (70)	mA	2) 3) 4)
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling: t_{PC} = t_{PC} min.)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	–	1	mA	1)
Average V_{CC} supply current, during $\overline{CAS}$-before-RAS refresh mode: -50 ns version	I_{CC6}	–	100(120)	mA	2) 4)
-60 ns version		–	90 (110)	mA	2) 4)
-70 ns version		–	80 (100)	mA	2) 4)
($\overline{RAS}$, $\overline{CAS}$ cycling: t_{RC} = t_{RC} min.)					
Average Self Refresh Current (CBR cycle with t_{RAS}>t_{RASS}min., $\overline{CAS}$ held low, $\overline{WE}$ = V_{CC} – 0.2 V, Address and Din = V_{CC} - 0.2 V or 0.2V)	I_{CC7}	–	1	mA	

AC Characteristics [5)7)]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 2 ns

Parameter	Symbol	Limit Values						Unit
		HYB 5116(7)405BJ/BT-50		HYB 5116(7)405BJ/BT-60		HYB 5116(7)405BJ/BT-70		
		min.	max.	min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	89	–	104	–	124	–	ns
Read-write cycle time	t_{RWC}	117	–	138	–	162	–	ns
Hyper page mode (EDO) cycle time	t_{HPC}	20	–	25	–	30	–	ns
Hyper page mode (EDO) read-write cycle time	t_{PRWC}	57	–	68	–	77	–	ns
Access time from $\overline{RAS}$ [7) 12)]	t_{RAC}	–	50	–	60	–	70	ns
Access time from $\overline{CAS}$ [7) 12)]	t_{CAC}	–	12	–	15	–	17	ns
Access time from column address [7) 13)]	t_{AA}	–	25	–	30	–	35	ns
Access time from $\overline{CAS}$ precharge [7)]	t_{CPA}	–	27	–	32	–	37	ns
$\overline{CAS}$ to output in low-Z [7)]	t_{CLZ}	0	–	0	–	0	–	ns
Output buffer turn-off delay [8) 18)]	t_{OFF}	0	15	0	15	0	20	ns
Transition time (rise and fall) [6)]	t_T	1	50	1	50	1	50	ns
$\overline{RAS}$ precharge time	t_{RP}	35	–	40	–	50	–	ns
$\overline{RAS}$ pulse width	t_{RAS}	50	10k	60	10k	70	10k	ns
$\overline{RAS}$ pulse width (Hyper page mode- EDO)	t_{RASP}	50	200k	60	200k	70	200k	ns
$\overline{CAS}$ pulse width	t_{CAS}	7	10k	10	10k	12	10k	ns
$\overline{CAS}$ precharge to $\overline{RAS}$ Delay (Hyper Page Mode)	t_{RHCP}	27	–	32	–	37	–	ns
$\overline{CAS}$ precharge to $\overline{WE}$ (HPM RMW)	t_{CPWD}	41	–	49	–	56	–	ns
$\overline{RAS}$ hold time	t_{RSH}	12		15	–	17	–	ns
$\overline{CAS}$ hold time	t_{CSH}	50		60	–	70	–	ns

AC Characteristics (cont'd) [5)7)]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 2 ns

Parameter	Symbol	Limit Values						Unit
		HYB 5116(7)405BJ/ BT-50		HYB 5116(7)405BJ/ BT-60		HYB 5116(7)405BJ/ BT-70		
		min.	max.	min.	max.	min.	max.	
$\overline{RAS}$ to $\overline{CAS}$ delay time [12)]	t_{RCD}	12	38	14	45	14	53	
$\overline{RAS}$ to column address delay time [13)]	t_{RAD}	10	25	12	30	12	35	ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	5	–	ns
$\overline{CAS}$ precharge time	t_{CP}	9	–	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns
Row address hold time	t_{RAH}	8	–	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns
Column address hold time	t_{CAH}	5	–	7	–	10	–	ns
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	–	30	–	35	–	ns
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns
Read command hold time [9)]	t_{RCH}	0	–	0	–	0	–	ns
Read command hold time referenced to $\overline{RAS}$ [9)]	t_{RRH}	0	–	0	–	0	–	ns
Write command hold time	t_{WCH}	5	–	7	–	10	–	ns
Write command pulse width	t_{WP}	5	–	7	–	10	–	ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	12	–	15	–	17	–	ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	12	–	15	–	17	–	ns
Data setup time [10)]	t_{DS}	0	–	0	–	0	–	ns
Data hold time [10)]	t_{DH}	5	–	7	–	10	–	ns
Refresh period for HYB5116405	t_{REF}	–	64	–	64	–	64	ms
Refresh period for HYB5117405	t_{REF}	–	32	–	32	–	32	ms
Write command setup time [11)]	t_{WCS}	0	–	0	–	0	–	ns

AC Characteristics (cont'd) [5)7)]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 2 ns

Parameter	Symbol	Limit Values						Unit
		HYB 5116(7)405BJ/ BT-50		HYB 5116(7)405BJ/ BT-60		HYB 5116(7)405BJ/ BT-70		
		min.	max.	min.	max.	min.	max.	
$\overline{CAS}$ to $\overline{WE}$ delay time [11)]	t_{CWD}	26	–	32	–	36	–	ns
$\overline{RAS}$ to WE delay time [11)]	t_{RWD}	64	–	77	–	89	–	ns
Column address to $\overline{WE}$ delay time [11)]	t_{AWD}	39	–	47	–	54	–	ns
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CSR}	10	–	10	–	10	–	ns
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CHR}	10	–	10	–	10	–	ns
$\overline{CAS}$ hold time (Test mode entry cycle)	t_{CHRT}	30	–	30	–	30	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5	–	5	–	5	–	ns
$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ counter test cycle)	t_{CPT}	35	–	40	–	40	–	ns
Write command setup time (in test mode entry cycle)	t_{WTS}	10	–	10	–	10	–	ns
Write command hold time (in test mode entry cycle)	t_{WTH}	10	–	10	–	10	–	ns
Write to $\overline{RAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{WRP}	10	–	10	–	10	–	ns
Write hold time referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{WRH}	10	–	10	–	10	–	ns
Output data hold time	t_{COH}	5	–	5	–	5	–	ns
$\overline{OE}$ command hold time	t_{OEH}	12	–	15	–	17	–	ns
$\overline{OE}$ access time	t_{OEA}	–	12	–	15	–	17	ns
Output buffer turn-off delay from $\overline{OE}$	t_{OEZ}	0	12	0	15	0	17	ns
Data to $\overline{CAS}$ low delay [15)]	t_{DZC}	0	–	0	–	0	–	ns
Data to $\overline{OE}$ low delay [15)]	t_{DZO}	0	–	0	–	0	–	ns

AC Characteristics (cont'd) [5)7)]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 2 ns

Parameter	Symbol	Limit Values						Unit
		HYB 5116(7)405BJ/ BT-50		HYB 5116(7)405BJ/ BT-60		HYB 5116(7)405BJ/ BT-70		
		min.	max.	min.	max.	min.	max.	
$\overline{CAS}$ high to data delay [16)]	t_{CDD}	12	–	15	–	17	–	ns
$\overline{OE}$ high to data delay [16)]	t_{ODD}	12	–	15	–	17	–	ns
$\overline{RAS}$ pulse width during self refresh	t_{RASS}	100k	–	100k	–	100k	–	ns
$\overline{RAS}$ precharge time during self refresh	t_{RPS}	95	–	110	–	130	–	ns
$\overline{CAS}$ hold time during self refresh	t_{CHS}	– 50	–	– 50	–	– 50	–	ns

Capacitance

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A10,A11)	C_{I1}	–	5	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}	–	7	pF
I/O capacitance (I/O1-I/O4)	C_{IO}	–	7	pF

Notes:

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.

4) Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4} it can be changed once or less during a hyper page mode cycle (t_{HPC}).

5) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6) $V_{IH\ (min.)}$ and $V_{IL\ (max.)}$ are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.

7) Measured with a load equivalent to 2 TTL gates and 50 pF (V_{ol} = 0.8 V and V_{oh} = 2.0 V).

8) $t_{OFF\ (max.)}$ and $t_{OEZ\ (max.)}$ define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.

9) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

10) These parameters are referenced to the CAS leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.

11) t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS\ (min.)}$, the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} > t_{RWD\ (min.)}$, $t_{CWD} > t_{CWD\ (min.)}$, $t_{AWD} > t_{AWD\ (min.)}$ and $t_{CPWD} > t_{CPWD\ (min.)}$, the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.

12) Operation within the $t_{RCD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RCD\ (max.)}$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD\ (max.)}$ limit, then access time is controlled by t_{CAC}.

13) Operation within the $t_{RAD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RAD\ (max.)}$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD\ (max.)}$ limit, then access time is controlled by t_{AA}.

14) AC measurements assume t_T = 2 ns.

15) Either t_{DZC} or t_{DZO} must be satisfied.

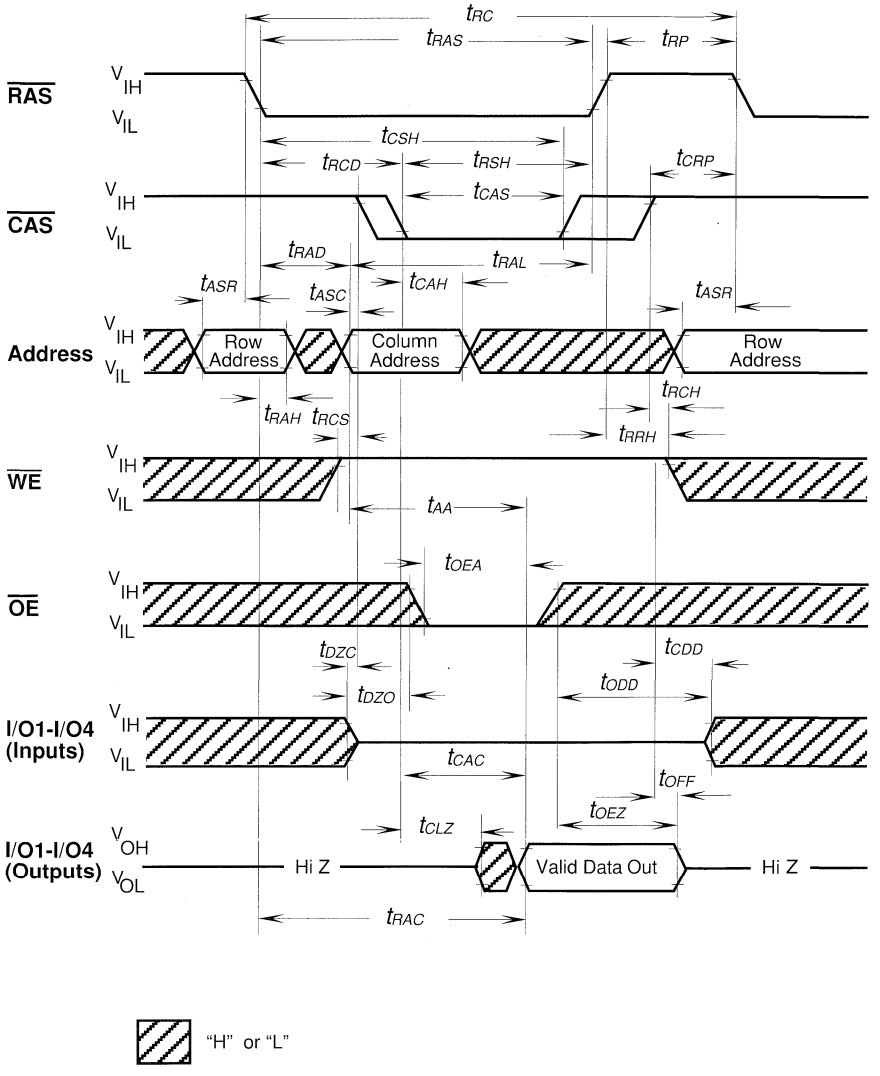
16) Either t_{CDD} or t_{ODD} must be satisfied.

17) When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:

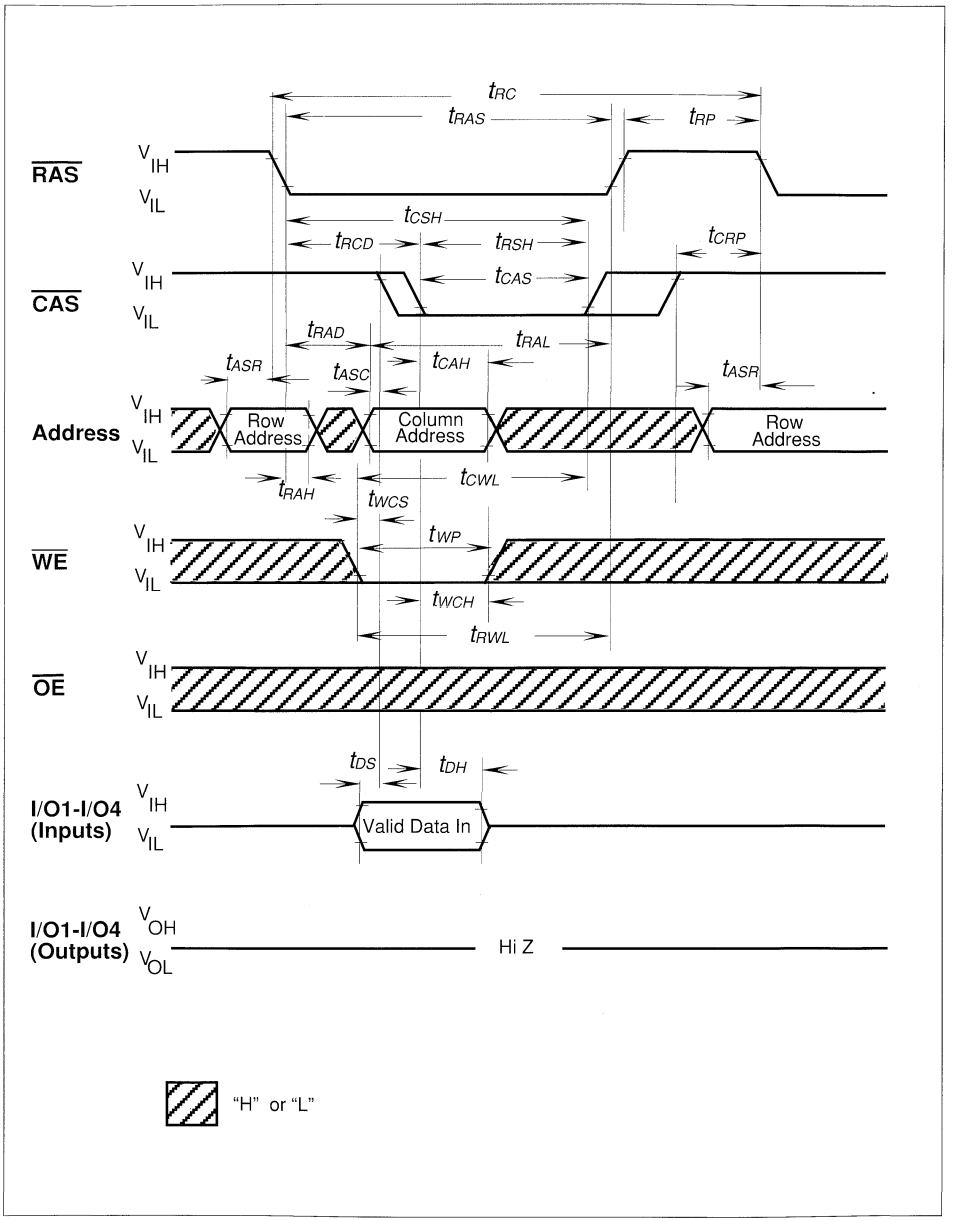
    If row addresses are being refreshed on an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh.

    If row addresses are being refreshed in any other manner (ROR - Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh.

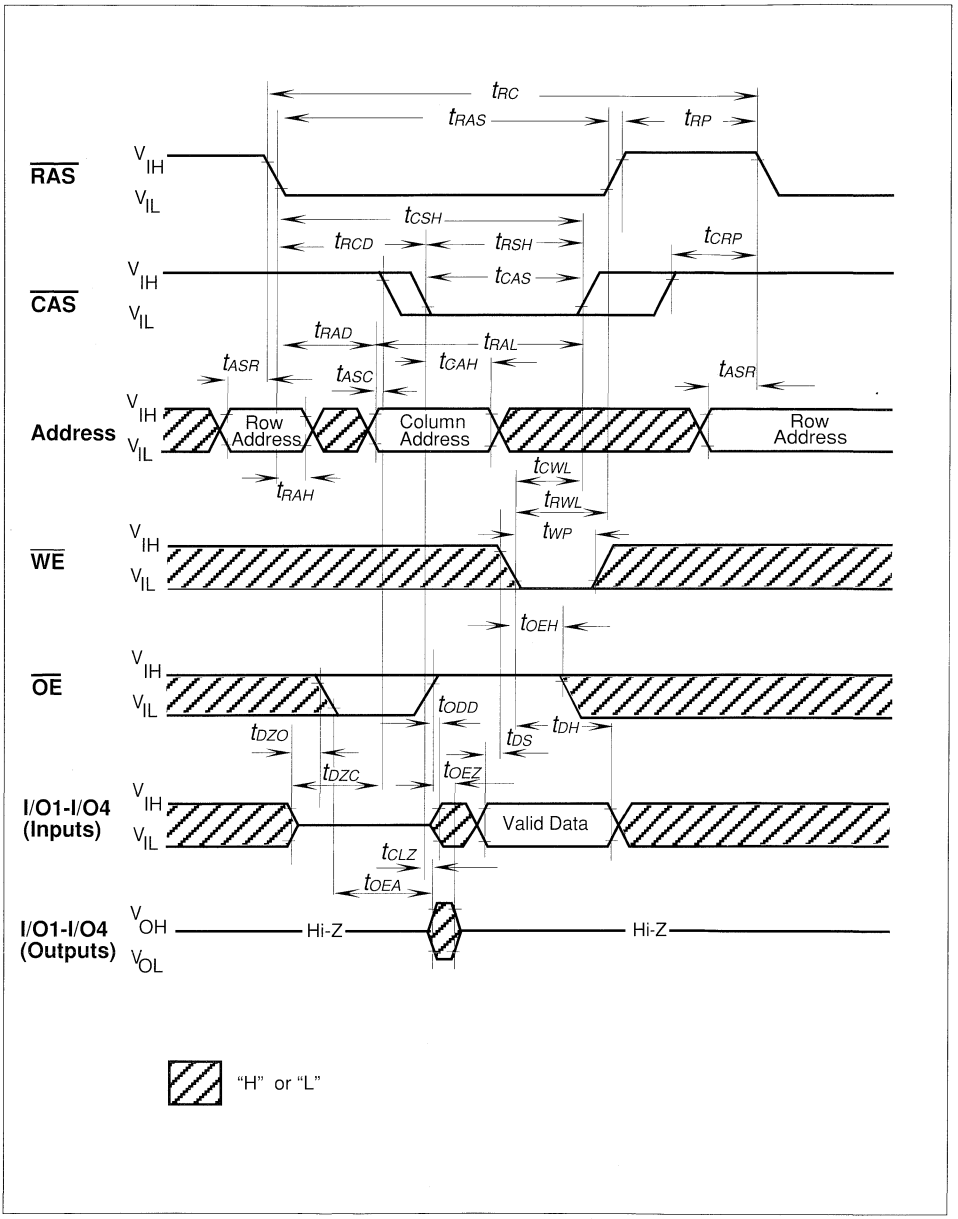
18) t_{off} is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tASR
tASC
tCAH
Address
Row Address
Column Address
Row Address
tRAH
tRCS
tRCH
tRRH
WE
tAA
tOEA
OE
tDZC
tDZO
tCDD
tODD
I/O1-I/O4 (Inputs)
tCAC
tOFF
tOEZ
tCLZ
I/O1-I/O4 (Outputs)
VOH
VOL
Hi Z
Valid Data Out
Hi Z
tRAC
"H" or "L"

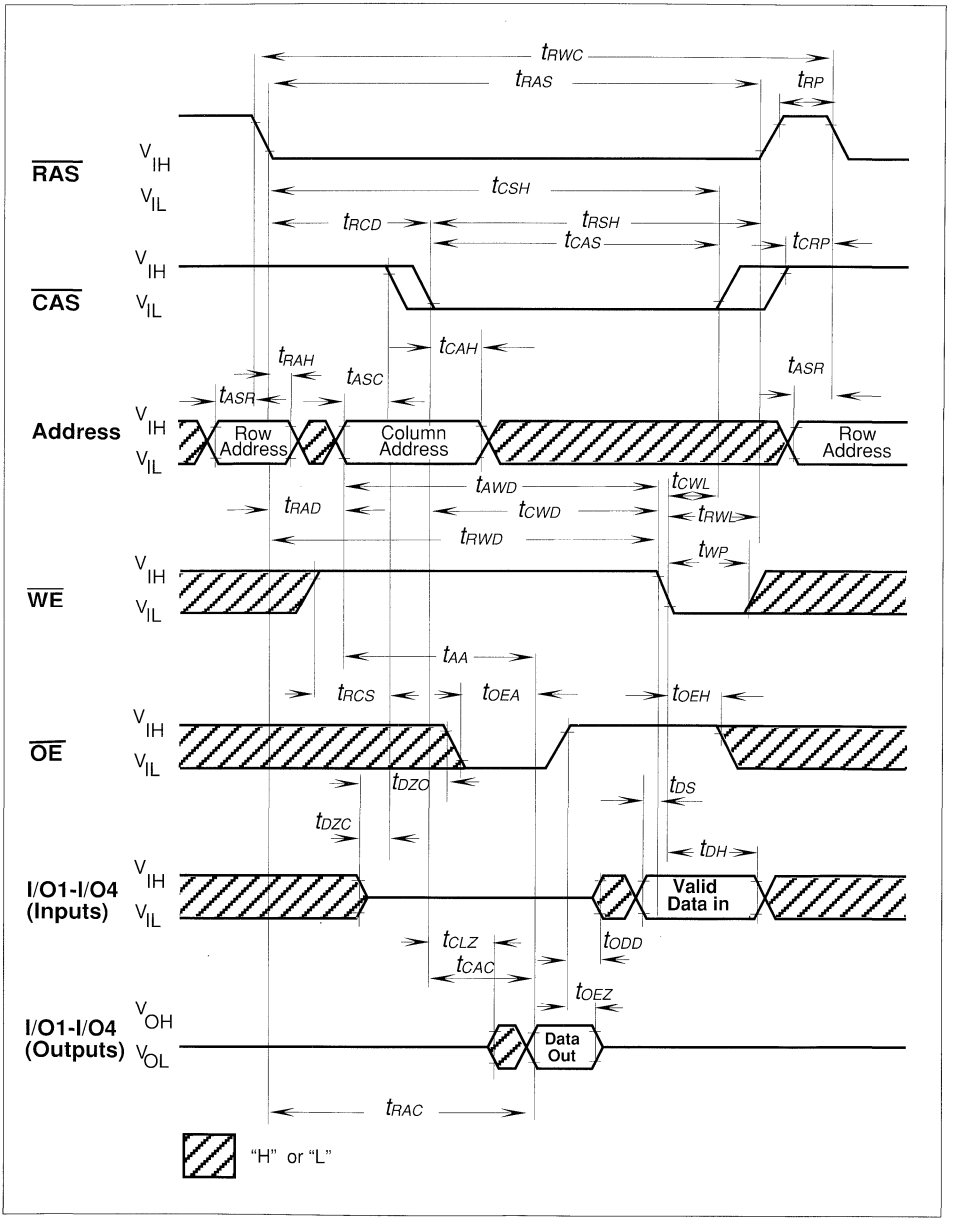
Read Cycle



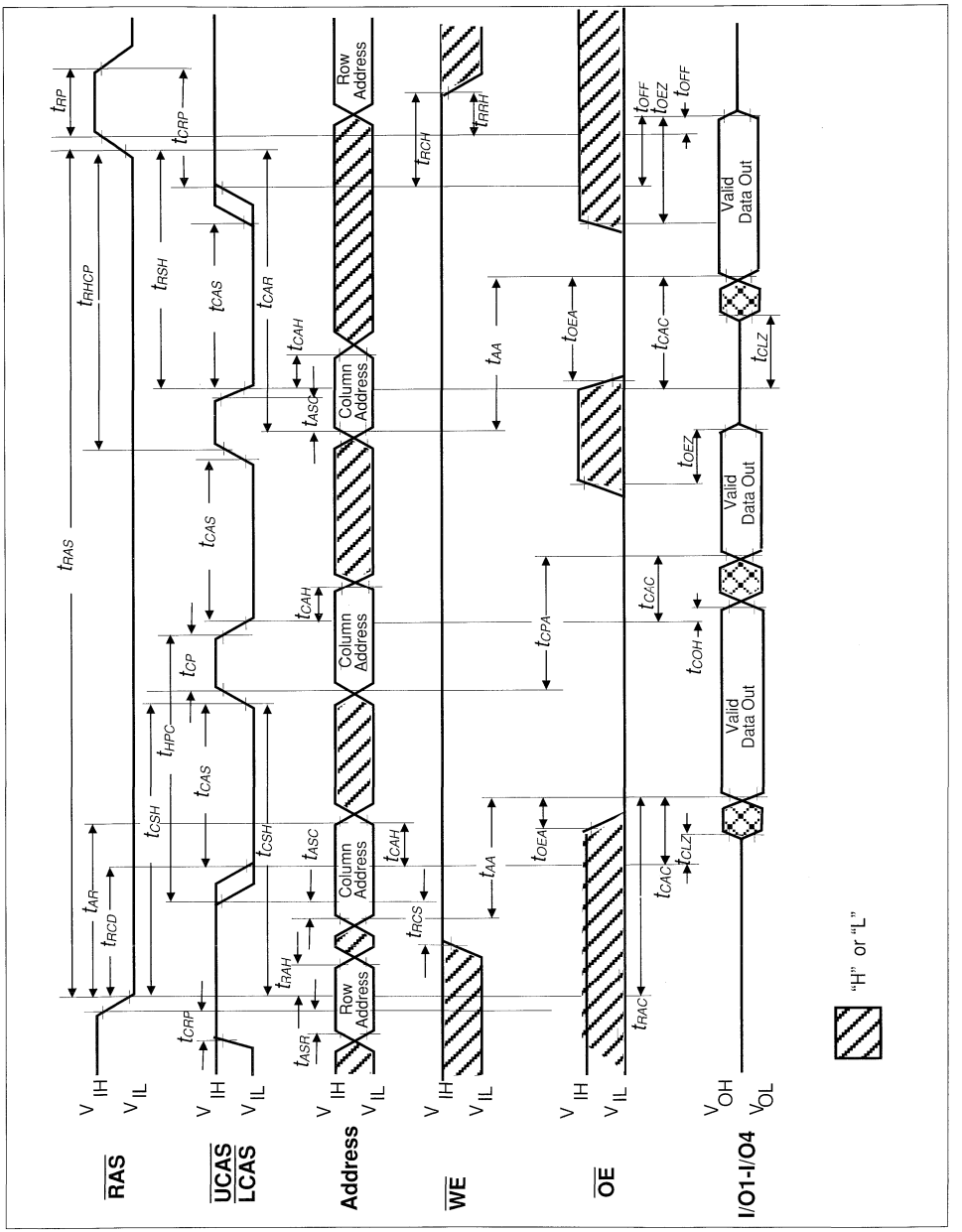
Write Cycle (Early Write)



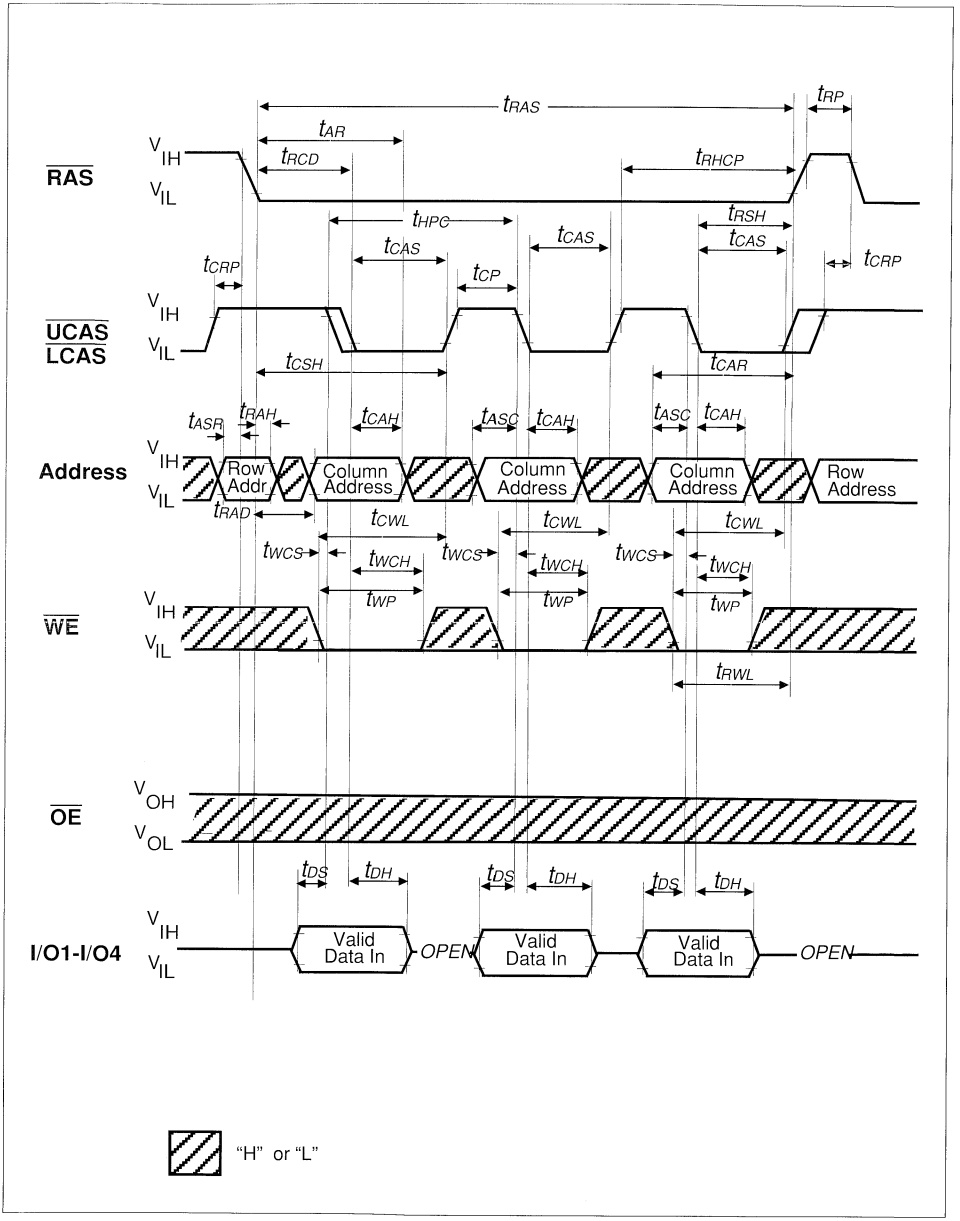
Write Cycle ($\overline{OE}$ Controlled Write)



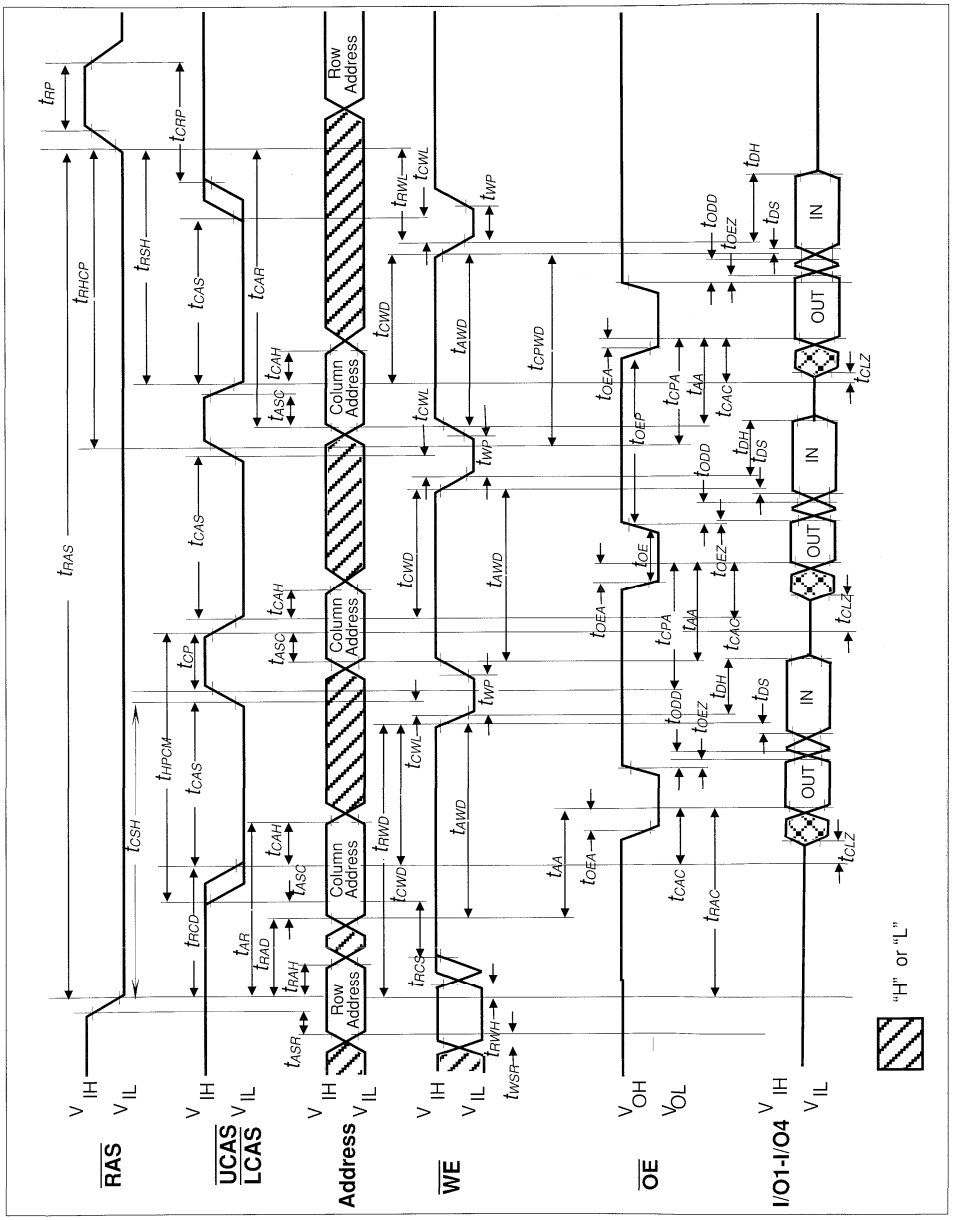
Read-Write (Read-Modify-Write) Cycle



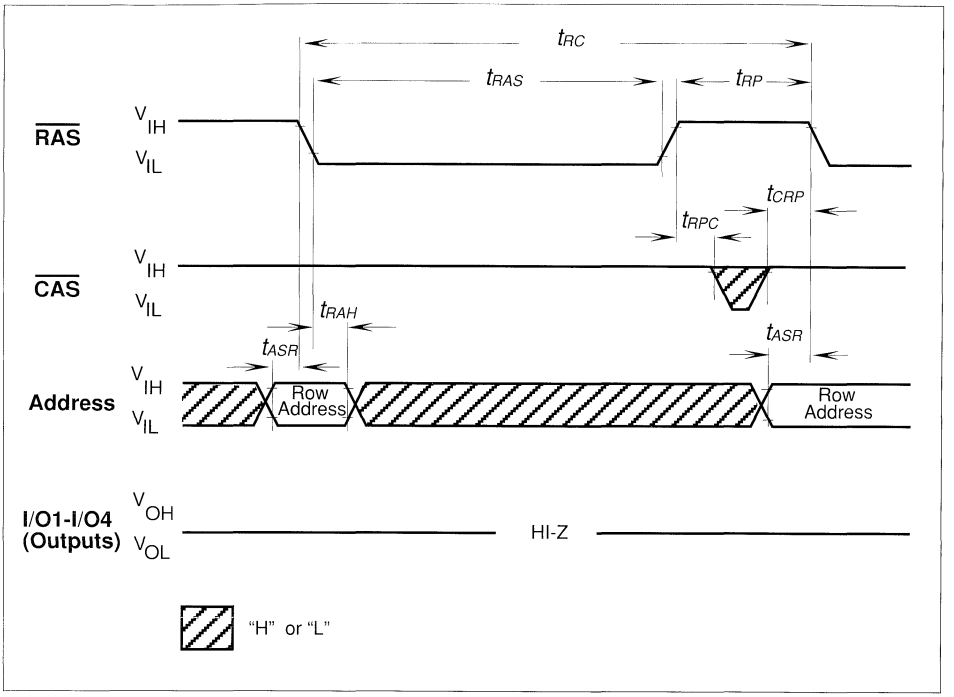
Hyper Page Mode (EDO) Read Cycle



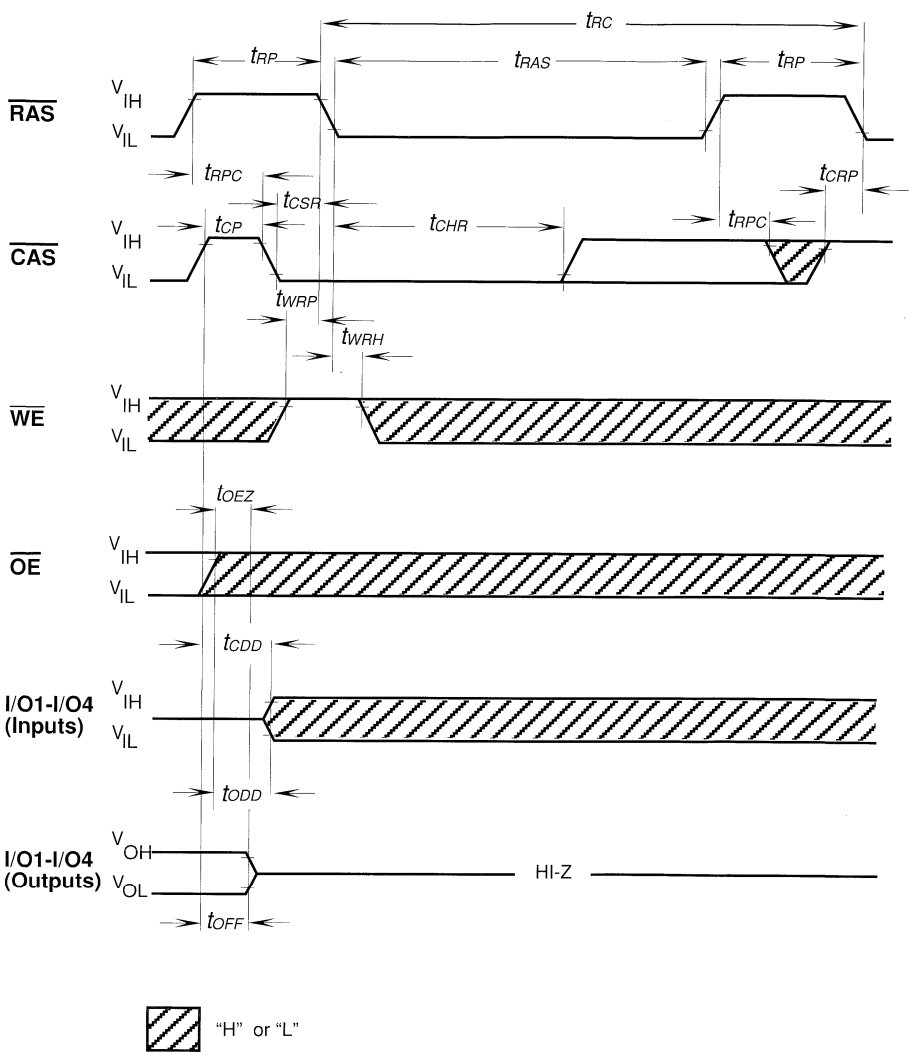
Hyper Page Mode (EDO) Write Cycle



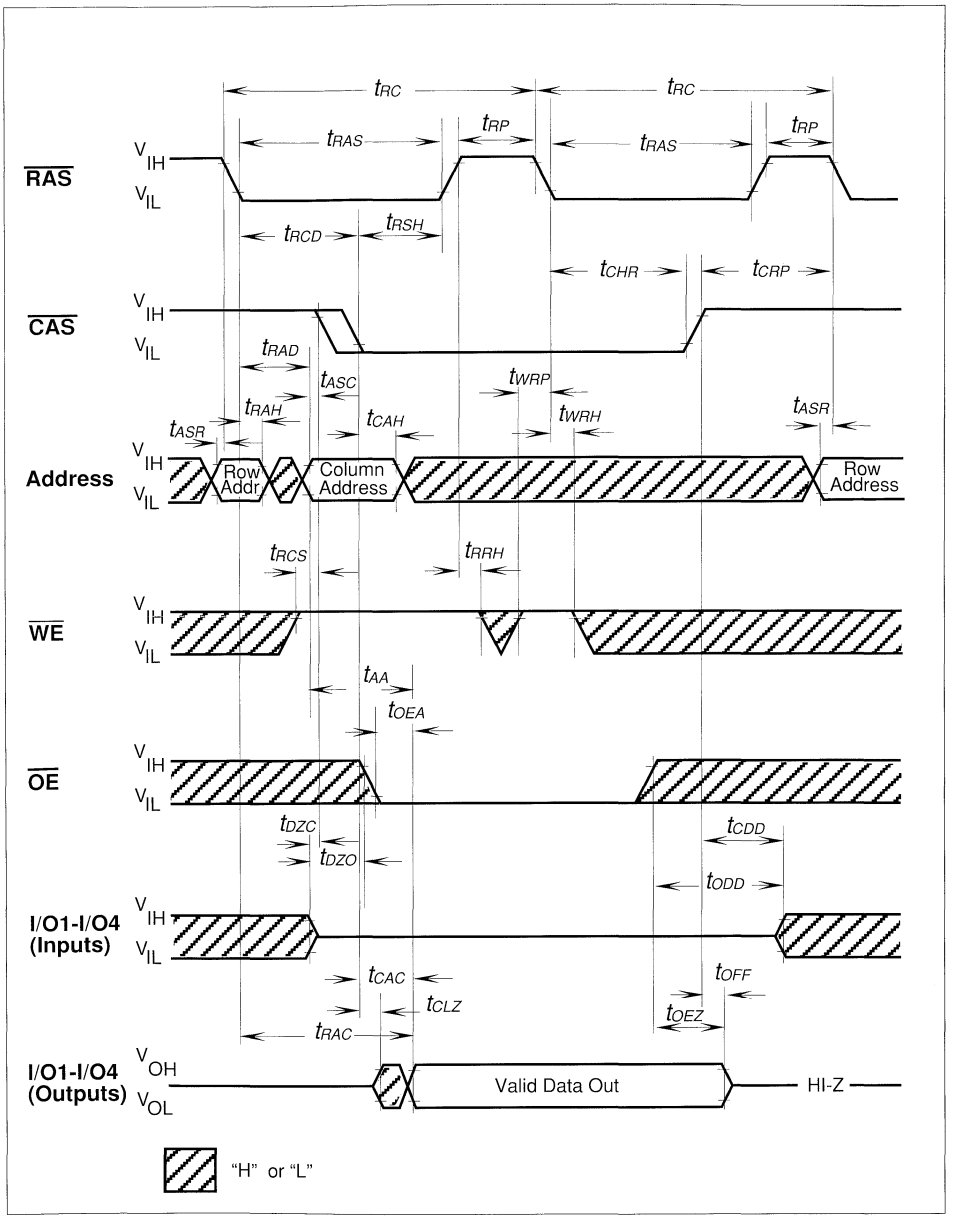
Hyper Page Mode (EDO) Late Write and Read-Modify Write Cycle



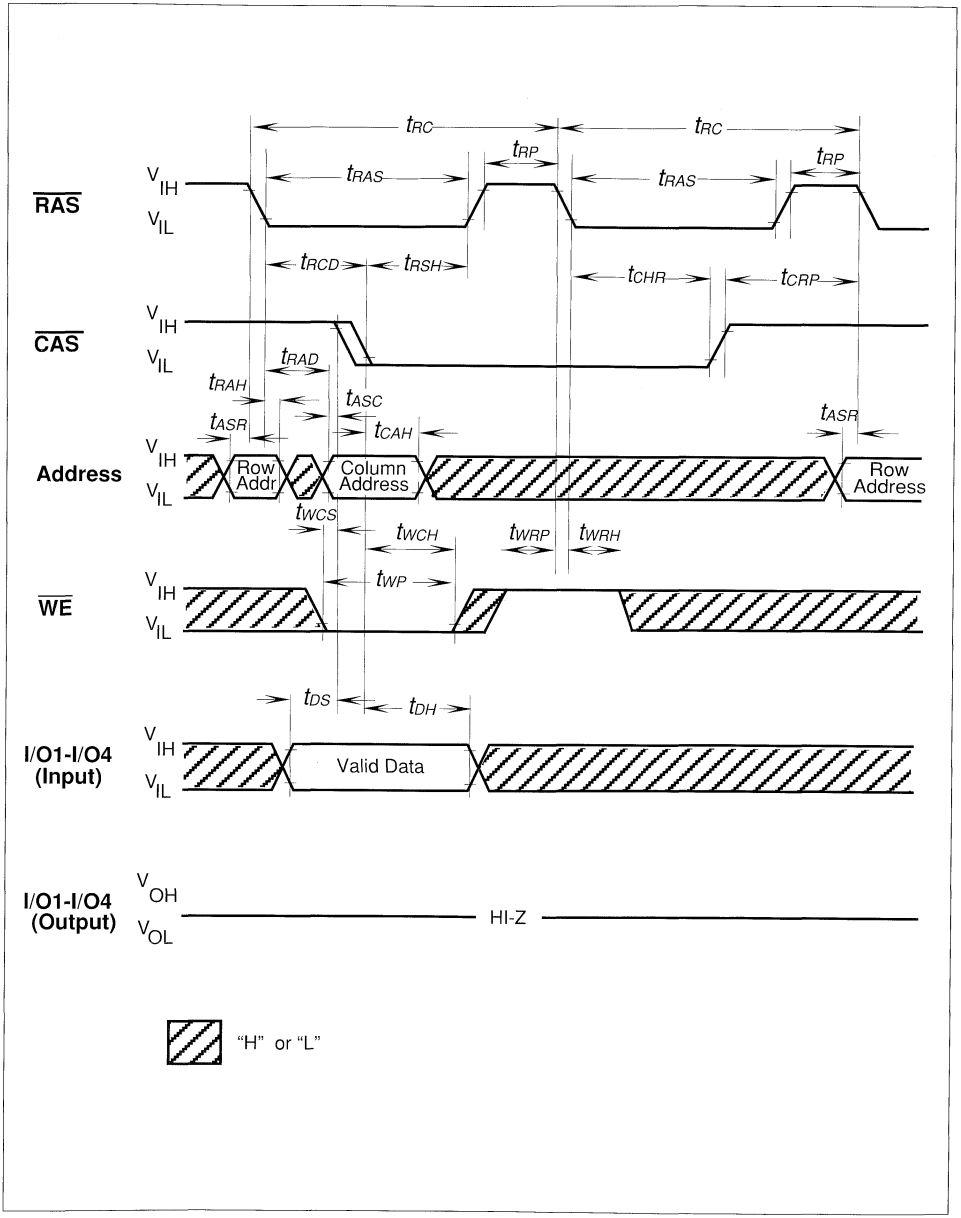
$\overline{RAS}$-Only Refresh Cycle



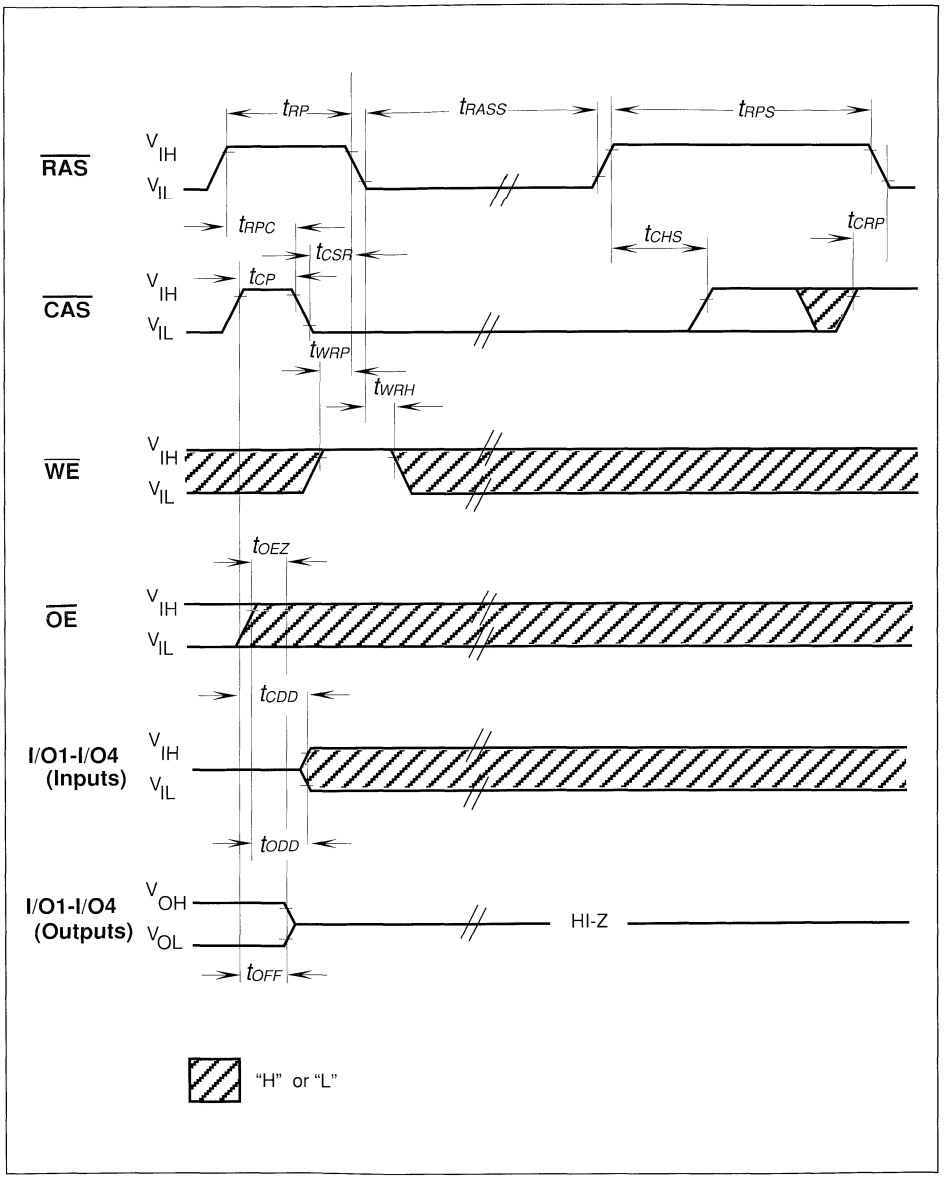
CAS-Before-RAS Refresh Cycle



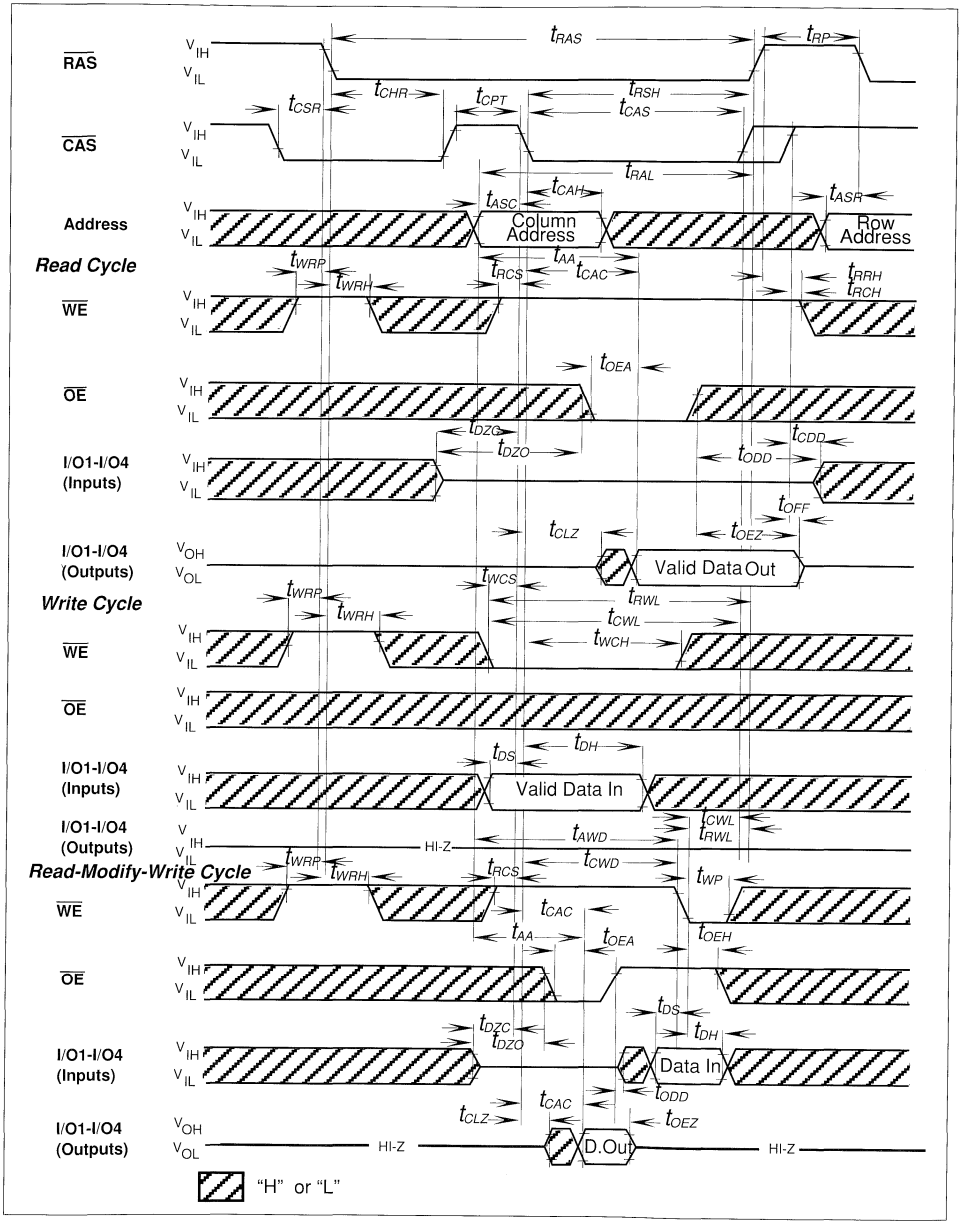
Hidden Refresh Cycle (Read)



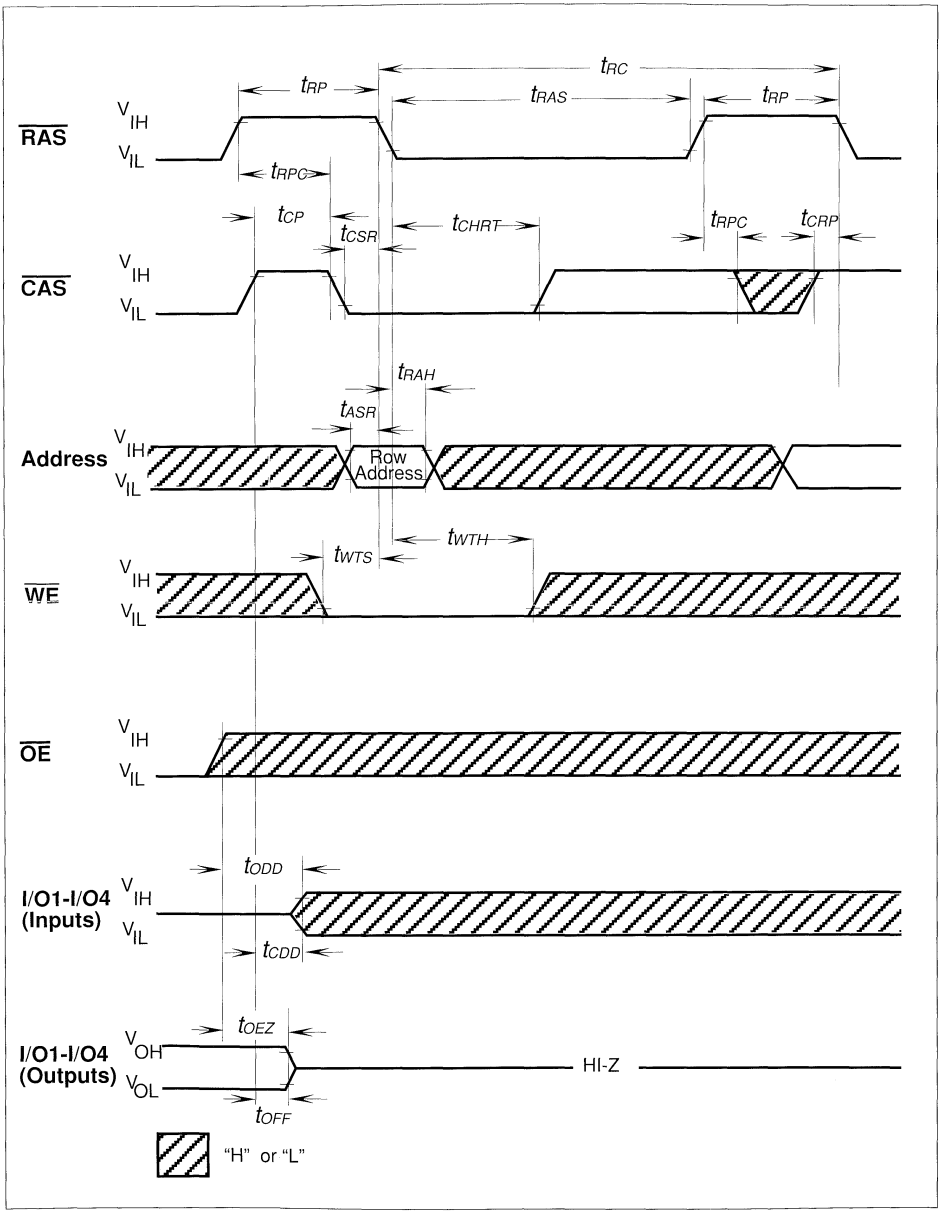
Hidden Refresh Cycle (Early Write)



CAS-before-RAS Self Refresh



CAS-Before-RAS Refresh Counter Test Cycle



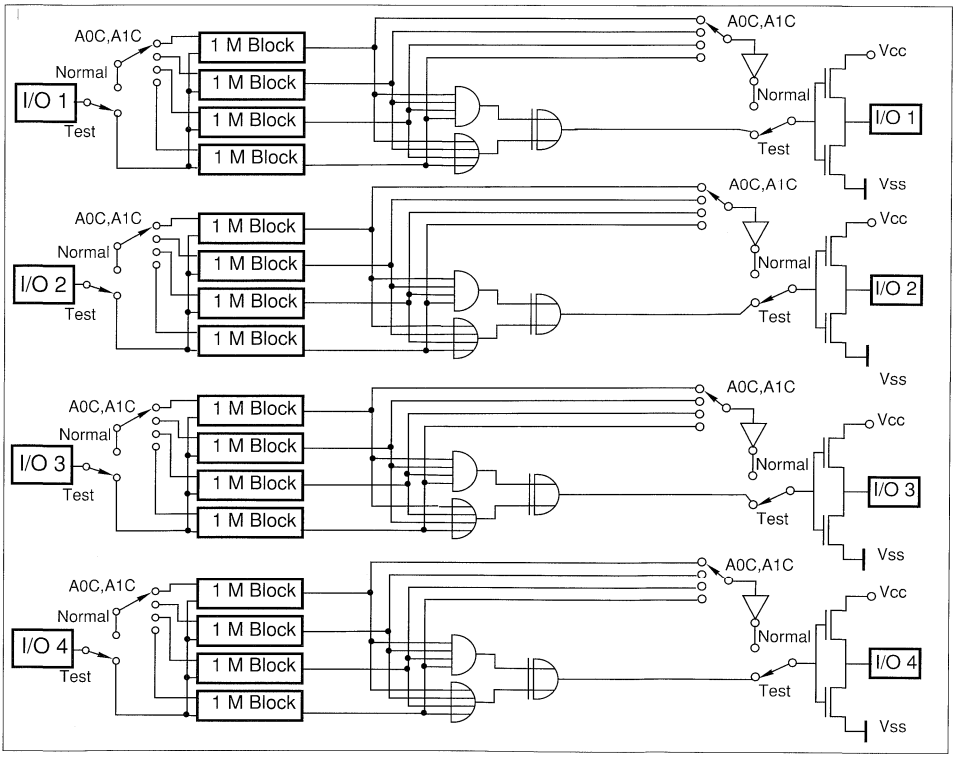
Test Mode Entry

Test Mode

As the HYB 5116(7)405BJ/BT is organized internally as 1M x 16-bits, a test mode cycle using 4:1 compression can be used to improve test time. Note that in the 4M x 4 version the test time is reduced by 1/4 for a N test pattern.

In a test mode "write" the data from each I/O pin is written into four 1M blocks simultaneously (all "1" s or all "0" s). In test mode "read" each I/O output is used for indicating the test mode result. If the internal four bits are equal, the I/O would indicate a "1". If they were not equal, the I/O would indicate a "0". The WCBR cycle ($\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$) puts the device into test mode. To exit from test mode, a "$\overline{CAS}$ before $\overline{RAS}$ refresh", "$\overline{RAS}$ only refresh" or "Hidden refresh" can be used.Refresh during test mode operation can be performed by normal read cylces or by WCBR refresh cycles.

Row addresses A0 through A9 have to kept high to perform a testmode entry cylce. All other addresses are don't care.



Block Diagram in Test Mode

2M x 8-Bit Dynamic RAM

HYB 5117800BSJ-50/-60/-70

Advanced Information

- 2 097 152 words by 8-bit organization
- 0 to 70 °C operating temperature
- Fast access and cycle time
  $\overline{RAS}$ access time:
  50 ns (-50 version)
  60 ns (-60 version)
  70 ns (-70 version)
  Cycle time:
  95 ns (-50 version)
  110 ns (-60 version)
  130 ns (-70 version)
  $\overline{CAS}$ access time:
  15 ns (-50,-60 version)
  20 ns (-70 version)
- Fast page mode cycle time
  35 ns (-50 version)
  40 ns (-60 version)
  45 ns (-70 version)
- Single + 5 V (± 10 %) supply
- Low power dissipation
  max. 660 active mW (-50 version)
  max. 605 active mW (-60 version)
  max. 550 active mW (-70 version)
  11 mW standby (TTL)
  5.5 mW standby (MOS)
- Output unlatched at cycle end allows two-dimensional chip selection
- Read, write, read-modify-write, $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, hidden refresh, self refresh and test mode
- Fast page mode capability
- All inputs, outputs and clocks fully TTL-compatible
- 2048 refresh cycles/ 32 ms
- Plastic Package: P-SOJ-28-3 400 mil

Ordering Information

Type	Ordering Code	Package	Descriptions
HYB 5117800BSJ-50	Q67100-Q1092	P-SOJ-28-3 400 mil	DRAM (access time 50 ns)
HYB 5117800BSJ-60	Q67100-Q1093	P-SOJ-28-3 400 mil	DRAM (access time 60 ns)
HYB 5117800BSJ-70	Q67100-Q1094	P-SOJ-28-3 400 mil	DRAM (access time 70 ns)

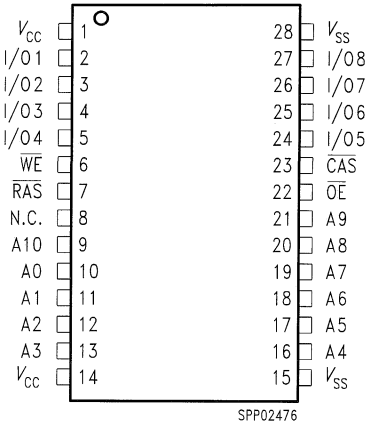
The HYB 5117800BSJ is the new generation dynamic RAM organized as 2097152 words by 8-bits. The HYB 5117800BSJ utilizes a submicron CMOS silicon gate process technology, as well as advanced circuit techniques to provide wide operating margins, both internally and for the system user. Multiplexed address inputs permit the HYB 5117800BSJ to be packaged in a standard SOJ 28 400 mil plastic package. These packages provide high system bit densities and are compatible with commonly used automatic testing and insertion equipment. System-oriented features include single + 5 V (± 10 %) power supply, direct interfacing with high-performance logic device families such as Schottky TTL.

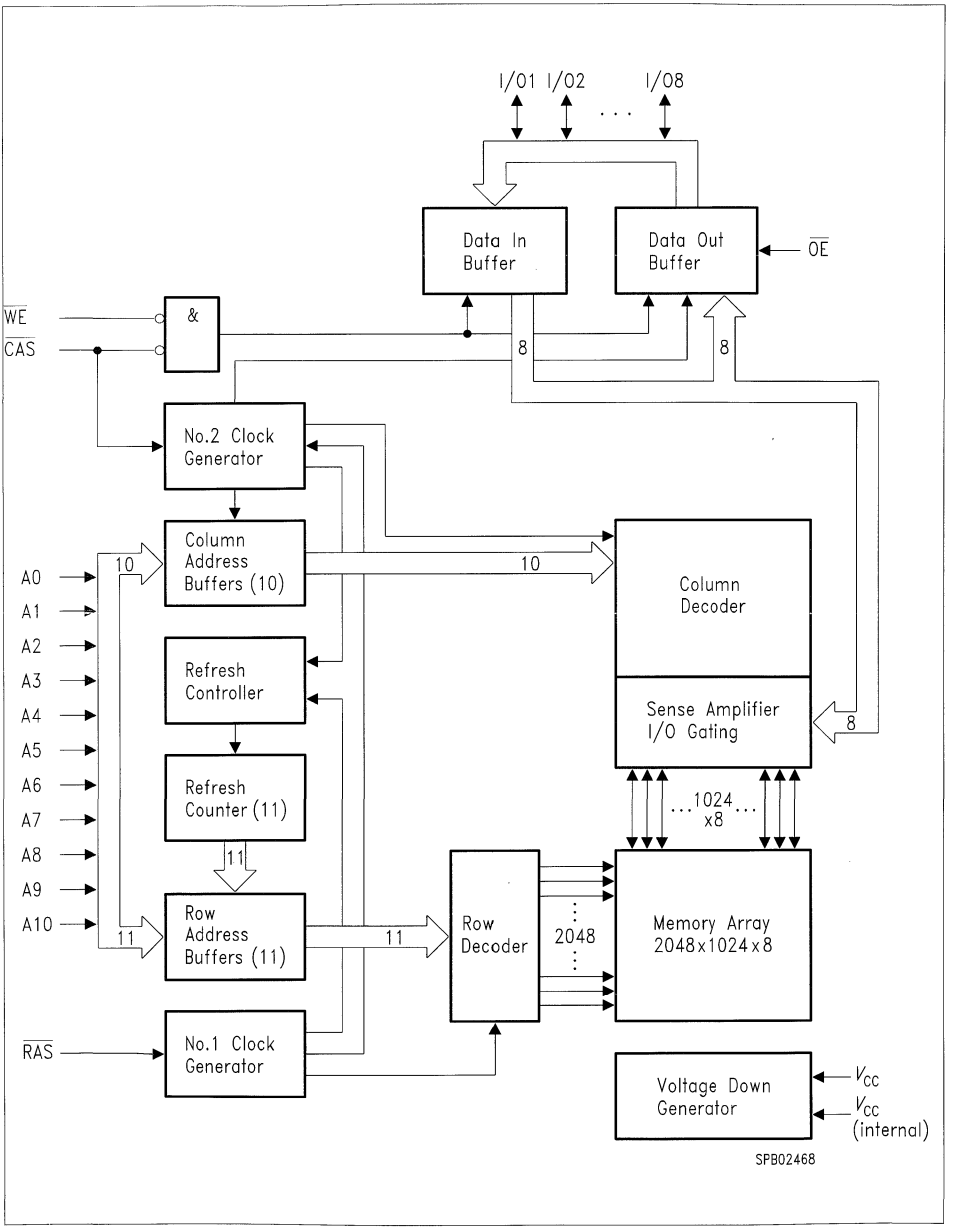
Pin Definitions and Functions

Pin No.	Function
A0 to A10	Row Address Inputs
A0 to A9	Column Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{OE}$	Output Enable
I/O1-I/O8	Data Input/Output
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground (0 V)
N.C.	not connected

Pin Configuration
(top view)

P-SOJ-28-3 (400mil)





Block Diagram

Absolute Maximum Ratings

Operating temperature range ..... 0 to 70 °C
Storage temperature range ..... – 55 to 150 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 0.5 to min (V_{CC} + 0.5, 7.0) V
Power supply voltage ..... – 1.0 V to 7.0 V
Power dissipation ..... 1.0 W
Data out current (short circuit) ..... 50 mA

Note:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	V_{CC} + 0.5	V	1)
Input low voltage	V_{IL}	– 0.5	0.8	V	1)
Output high voltage (I_{OUT} = – 5 mA)	V_{OH}	2.4	–	V	1)
Output low voltage (I_{OUT} = 4.2 mA)	V_{OL}	–	0.4	V	1)
Input leakage current,any input (0 V ≤ V_{IH} ≤ V_{CC} + 0.3 V, all other pins = 0 V)	$I_{I(L)}$	– 10	10	µA	1)
Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ V_{CC} + 0.3 V)	$I_{O(L)}$	– 10	10	µA	1)
Average V_{CC} supply current:	I_{CC1}				
-50 ns version		–	120	mA	2) 3) 4)
-60 ns version		–	110	mA	2) 3) 4)
-70 ns version		–	100	mA	2) 3) 4)
($\overline{RAS}$, $\overline{CAS}$, address cycling, t_{RC} = t_{RC} min.)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	2	mA	–
Average V_{CC} supply current, during $\overline{RAS}$-only refresh cycles:	I_{CC3}				
-50 ns version		–	120	mA	2) 4)
-60 ns version		–	110	mA	2) 4)
-70 ns version		–	100	mA	2) 4)
($\overline{RAS}$ cycling: $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)					

DC Characteristics (cont'd)

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current, during fast page mode: -50 ns version	I_{CC4}	–	90	mA	2) 3) 4)
-60 ns version		–	80	mA	2) 3) 4)
-70 ns version		–	70	mA	2) 3) 4)
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling, t_{PC} = t_{PC} min.)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	–	1	mA	1)
Average V_{CC} supply current, during $\overline{CAS}$-before-RAS refresh mode: -50 ns version	I_{CC6}	–	120	mA	2) 4)
-60 ns version		–	110	mA	2) 4)
-70 ns version		–	100	mA	2) 4)
($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min.)					
Average Self Refresh Current (CBR cycle with t_{RAS} > t_{RASS} min., $\overline{CAS}$ held low, $\overline{WE}$ = V_{CC} - 0.2 V, Address and Din = V_{CC} - 0.2 V or 0.2 V)	I_{CC7}	–	1	mA	

AC Characteristics [5]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		HYB 5117800 BSJ -50		HYB 5117800 BSJ -60		HYB 5117800 BSJ -70		
		min.	max.	min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	95	–	110	–	130	–	ns
Read-write cycle time	t_{RWC}	135	–	150	–	180	–	ns
Fast page mode cycle time	t_{PC}	35	–	40	–	45	–	ns
Fast page mode read-write cycle time	t_{PRWC}	75	–	80	–	95	–	ns
Access time from $\overline{RAS}$ [7) 12)]	t_{RAC}	–	50	–	60	–	70	ns
Access time from $\overline{CAS}$ [7) 12)]	t_{CAC}	–	15	–	15	–	20	ns
Access time from column address [7) 13)]	t_{AA}	–	25	–	30	–	35	ns
Access time from $\overline{CAS}$ precharge [7)]	t_{CPA}	–	30	–	35	–	40	ns
$\overline{CAS}$ to output in low-Z [7)]	t_{CLZ}	0	–	0	–	0	–	ns
Output buffer turn-off delay [8)]	t_{OFF}	0	15	0	15	0	20	ns
Transition time (rise and fall) [6)]	t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	35	–	40	–	50	–	ns
$\overline{RAS}$ pulse width	t_{RAS}	50	10k	60	10k	70	10k	ns
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	50	200k	60	200k	70	200k	ns
$\overline{CAS}$ precharge to $\overline{RAS}$ Delay	t_{RHCP}	30	–	35	–	40	–	ns
$\overline{CAS}$ precharge to $\overline{WE}$ (FPMR RMW)	t_{CPWD}	50	–	55	–	65	–	ns
$\overline{RAS}$ hold time	t_{RSH}	15		15	–	20	–	ns
$\overline{CAS}$ hold time	t_{CSH}	50		60	–	70	–	ns
$\overline{CAS}$ pulse width	t_{CAS}	15	10k	15	10k	20	10k	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time [12)]	t_{RCD}	20	35	20	45	20	50	
$\overline{RAS}$ to column address delay time [13)]	t_{RAD}	15	25	15	30	15	35	ns

AC Characteristics (cont'd) [5]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		HYB 5117800 BSJ -50		HYB 5117800 BSJ -60		HYB 5117800 BSJ -70		
		min.	max.	min.	max.	min.	max.	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	5	–	ns
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns
Row address hold time	t_{RAH}	10	–	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns
Column address hold time	t_{CAH}	10	–	15	–	15	–	ns
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	–	30	–	35	–	ns
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns
Read command hold time [9]	t_{RCH}	0	–	0	–	0	–	ns
Read command hold time referenced to $\overline{RAS}$ [9]	t_{RRH}	0	–	0	–	0	–	ns
Write command hold time	t_{WCH}	10	–	15	–	15	–	ns
Write command pulse width	t_{WP}	10	–	15	–	15	–	ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	–	15	–	20	–	ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	–	15	–	20	–	ns
Data setup time [10]	t_{DS}	0	–	0	–	0	–	ns
Data hold time [10]	t_{DH}	10	–	15	–	15	–	ns
Refresh period	t_{REF}	–	32	–	32	–	32	ms
Write command setup time [11]	t_{WCS}	0	–	0	–	0	–	ns
$\overline{CAS}$ to $\overline{WE}$ delay time [11]	t_{CWD}	35	–	35	–	45	–	ns
$\overline{RAS}$ to WE delay time [11]	t_{RWD}	70	–	80	–	95	–	ns
Column address to $\overline{WE}$ delay time [11]	t_{AWD}	45	–	50	–	60	–	ns
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CSR}	10	–	10	–	10	–	ns
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CHR}	10	–	10	–	10	–	ns

AC Characteristics (cont'd) [5]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		HYB 5117800 BSJ -50		HYB 5117800 BSJ -60		HYB 5117800 BSJ -70		
		min.	max.	min.	max.	min.	max.	
$\overline{CAS}$ hold time (Test mode entry cycle)	t_{CHRT}	30	–	30	–	30	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5	–	5	–	5	–	ns
$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ counter test cycle)	t_{CPT}	35	–	40	–	40	–	ns
Write command setup time (in test mode entry cycle)	t_{WTS}	10	–	10	–	10	–	ns
Write command hold time (in test mode entry cycle)	t_{WTH}	10	–	10	–	10	–	ns
Write to $\overline{RAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{WRP}	10	–	10	–	10	–	ns
Write hold time referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{WRH}	10	–	10	–	10	–	ns
$\overline{OE}$ command hold time	t_{OEH}	15	–	15	–	20	–	ns
$\overline{OE}$ access time	t_{OEA}	–	15	–	15	–	20	ns
Output buffer turn-off delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	ns
Data to $\overline{CAS}$ low delay [15]	t_{DZC}	0	–	0	–	0	–	ns
Data to $\overline{OE}$ low delay [15]	t_{DZO}	0	–	0	–	0	–	ns
$\overline{CAS}$ high to data delay [16]	t_{CDD}	15	–	15	–	20	–	ns
$\overline{OE}$ high to data delay [16]	t_{ODD}	15	–	15	–	20	–	ns
$\overline{RAS}$ pulse width during self refresh	t_{RASS}	100k	–	100k	–	100k	–	ns
$\overline{RAS}$ precharge time during self refresh	t_{RPS}	95	–	110	–	130	–	ns
$\overline{CAS}$ hold time during self refresh	t_{CHS}	– 50	–	– 50	–	– 50	–	ns

Capacitance

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A10)	C_{I1}	–	5	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}	–	7	pF
I/O capacitance (I/O1-I/O8)	C_{IO}	–	7	pF

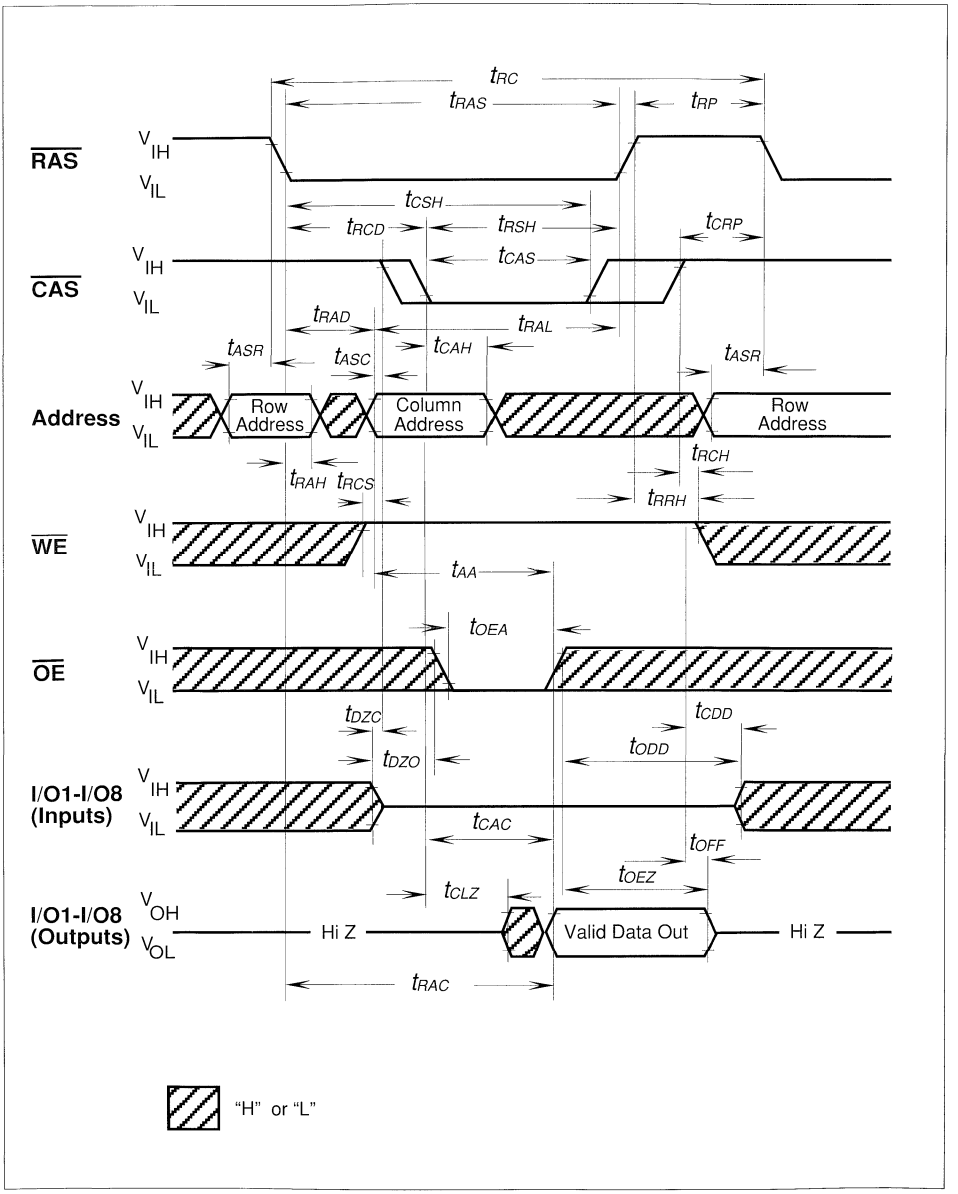
Notes:

1) All voltages are referenced to V_{SS}.
2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.
4) Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4} it can be changed once or less during a fast page mode cycle (t_{PC}).
5) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6) $V_{IH\ (min.)}$ and $V_{IL\ (max.)}$ are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.
7) Measured with a load equivalent to 2 TTL loads and 100 pF.
8) $t_{OFF\ (max.)}$ and $t_{OEZ\ (max.)}$ define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.
9) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10) These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.
11) t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS\ (min.)}$, the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} > t_{RWD\ (min.)}$, $t_{CWD} > t_{CWD\ (min.)}$, $t_{AWD} > t_{AWD\ (min.)}$ and $t_{CPWD} > t_{CPWD\ (min.)}$, the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.
12) Operation within the $t_{RCD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RCD\ (max.)}$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD\ (max.)}$ limit, then access time is controlled by t_{CAC}.
13) Operation within the $t_{RAD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RAD\ (max.)}$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD\ (max.)}$ limit, then access time is controlled by t_{AA}.
14) AC measurements assume t_T = 5 ns.
15) Either t_{DZC} or t_{DZO} must be satisfied.
16) Either t_{CDD} or t_{ODD} must be satisfied.
17) When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:

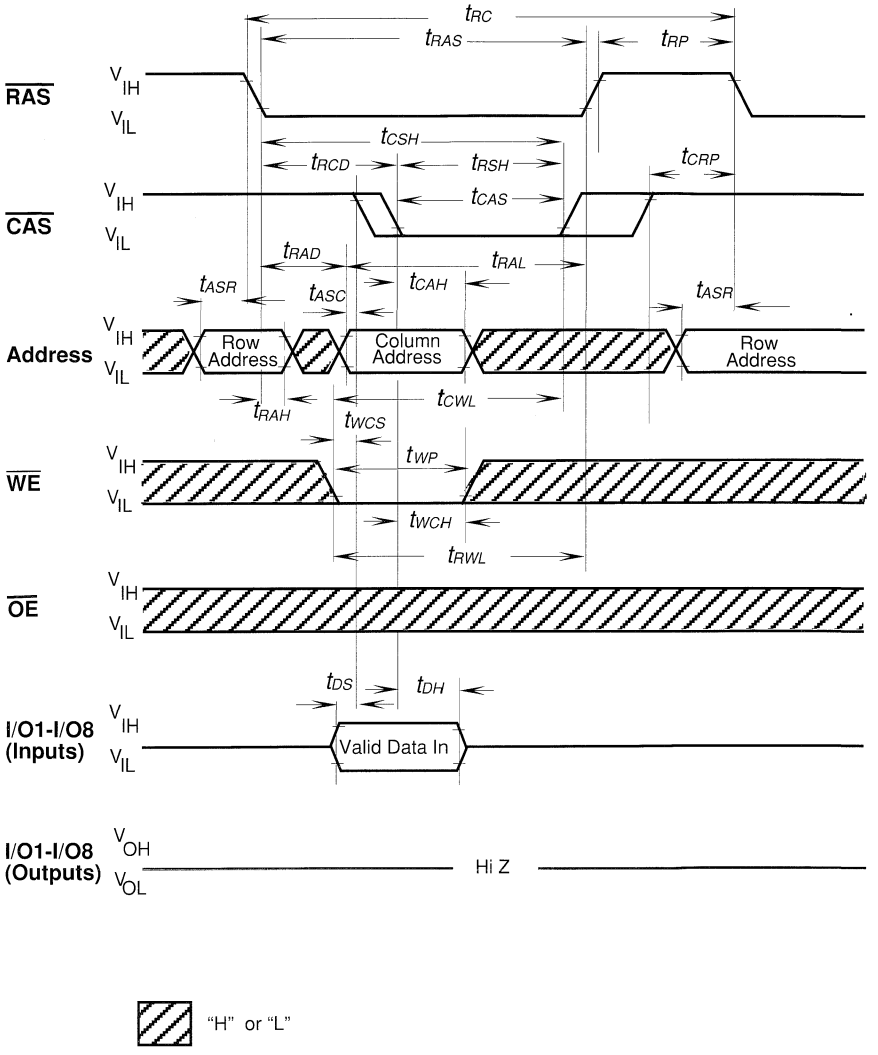
    If row addresses are being refreshed on an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh.

    If row addresses are being refreshed in any other manner (ROR - Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh.

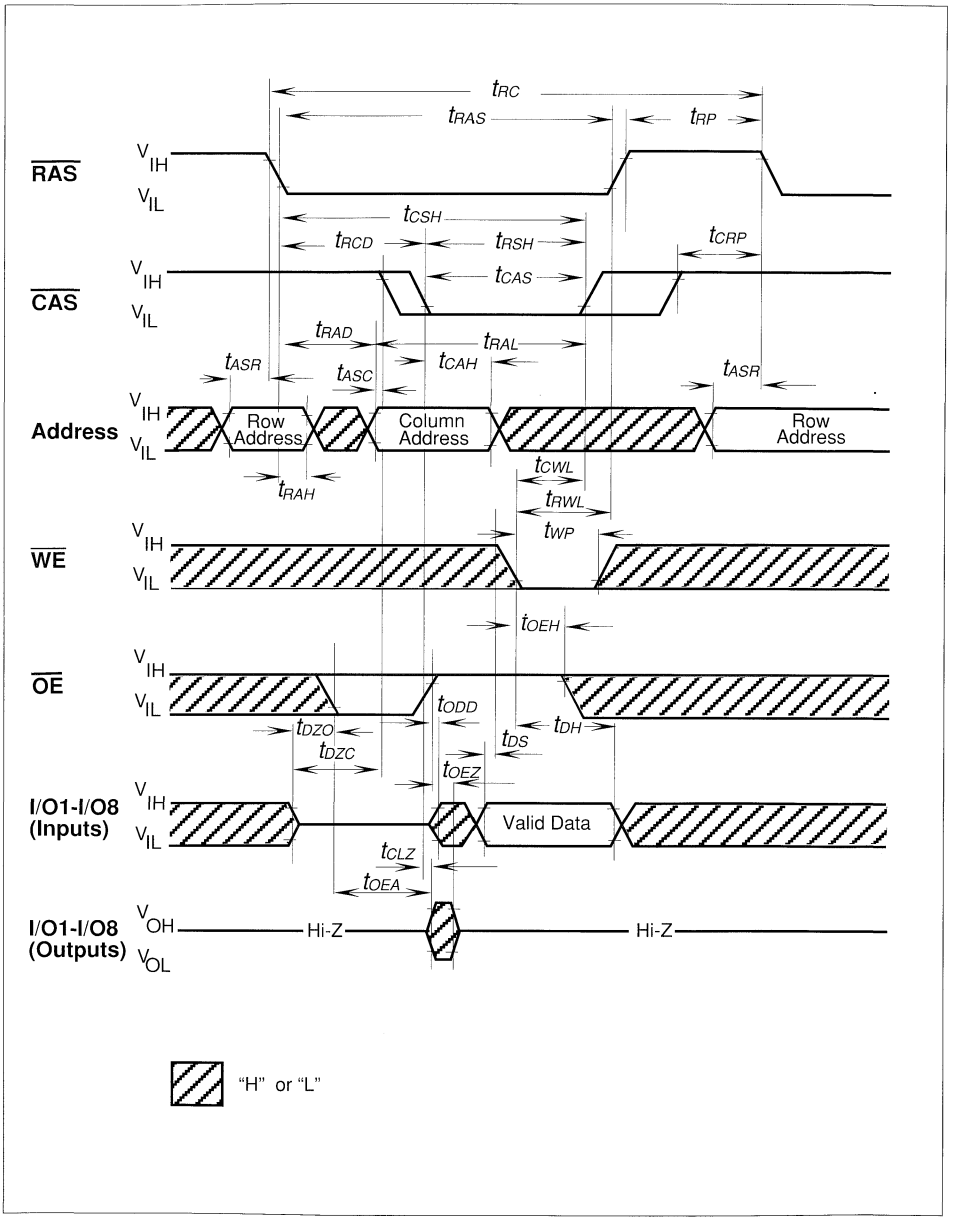
Waveforms



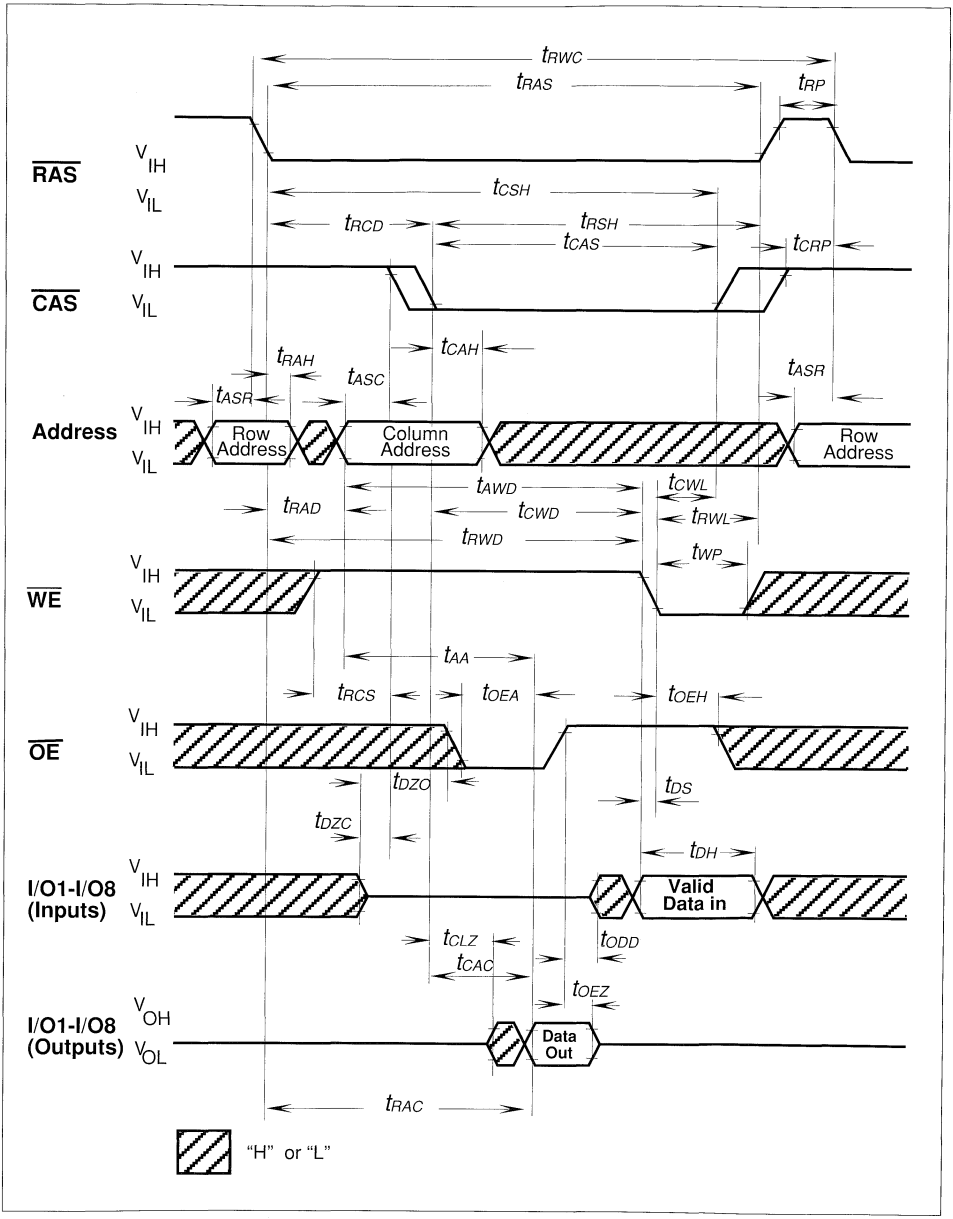
Read Cycle



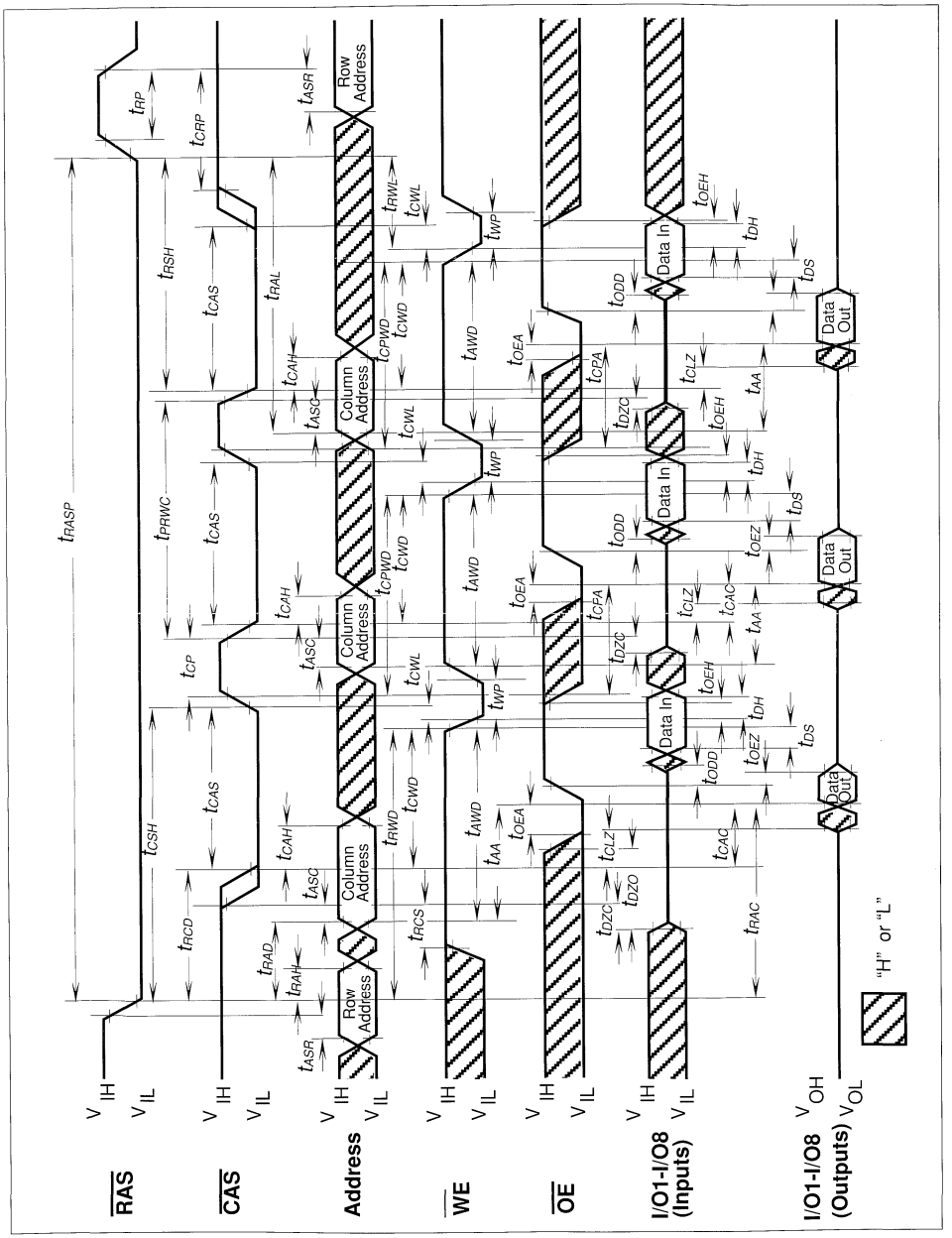
Write Cycle (Early Write)



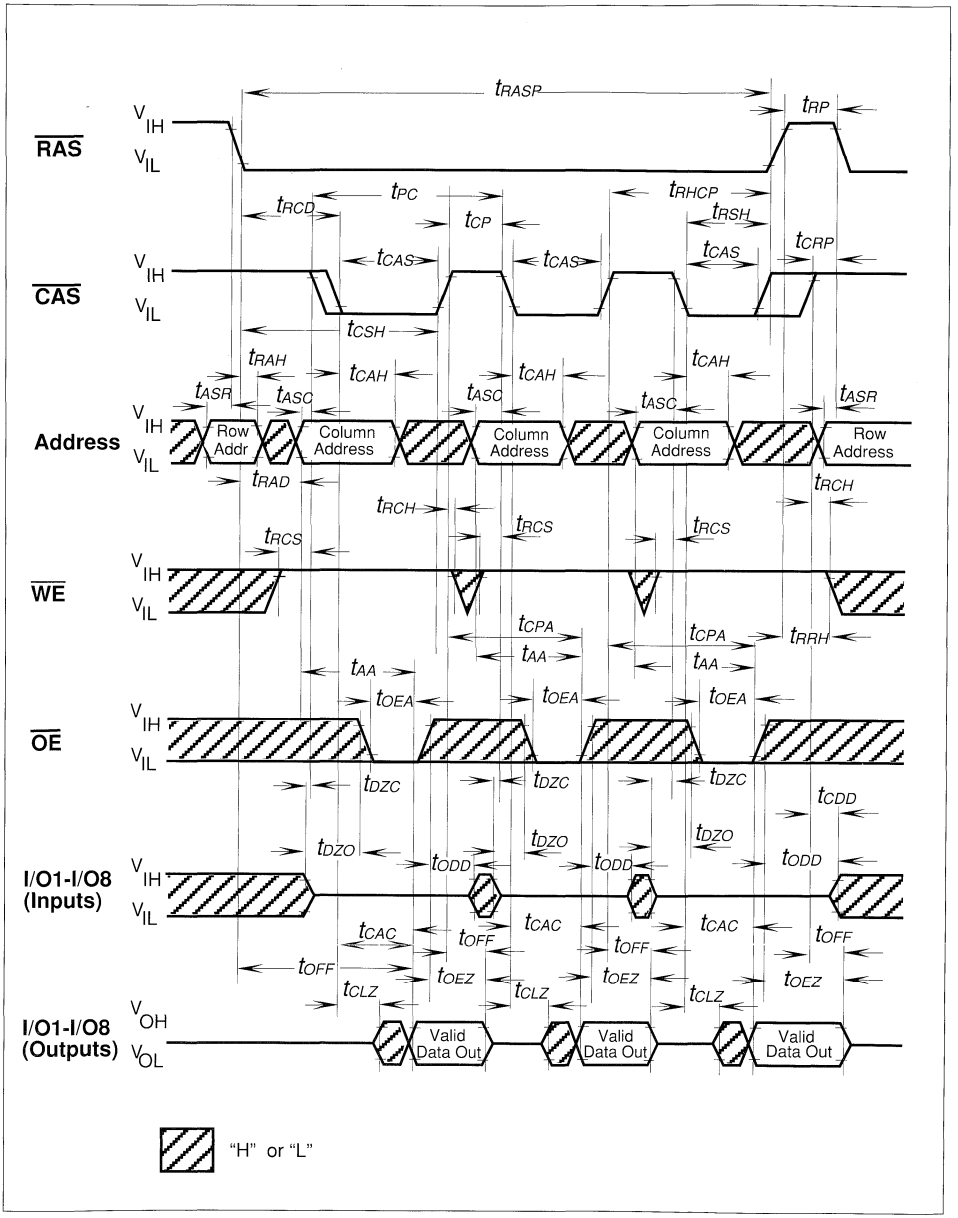
Write Cycle ($\overline{OE}$ Controlled Write)



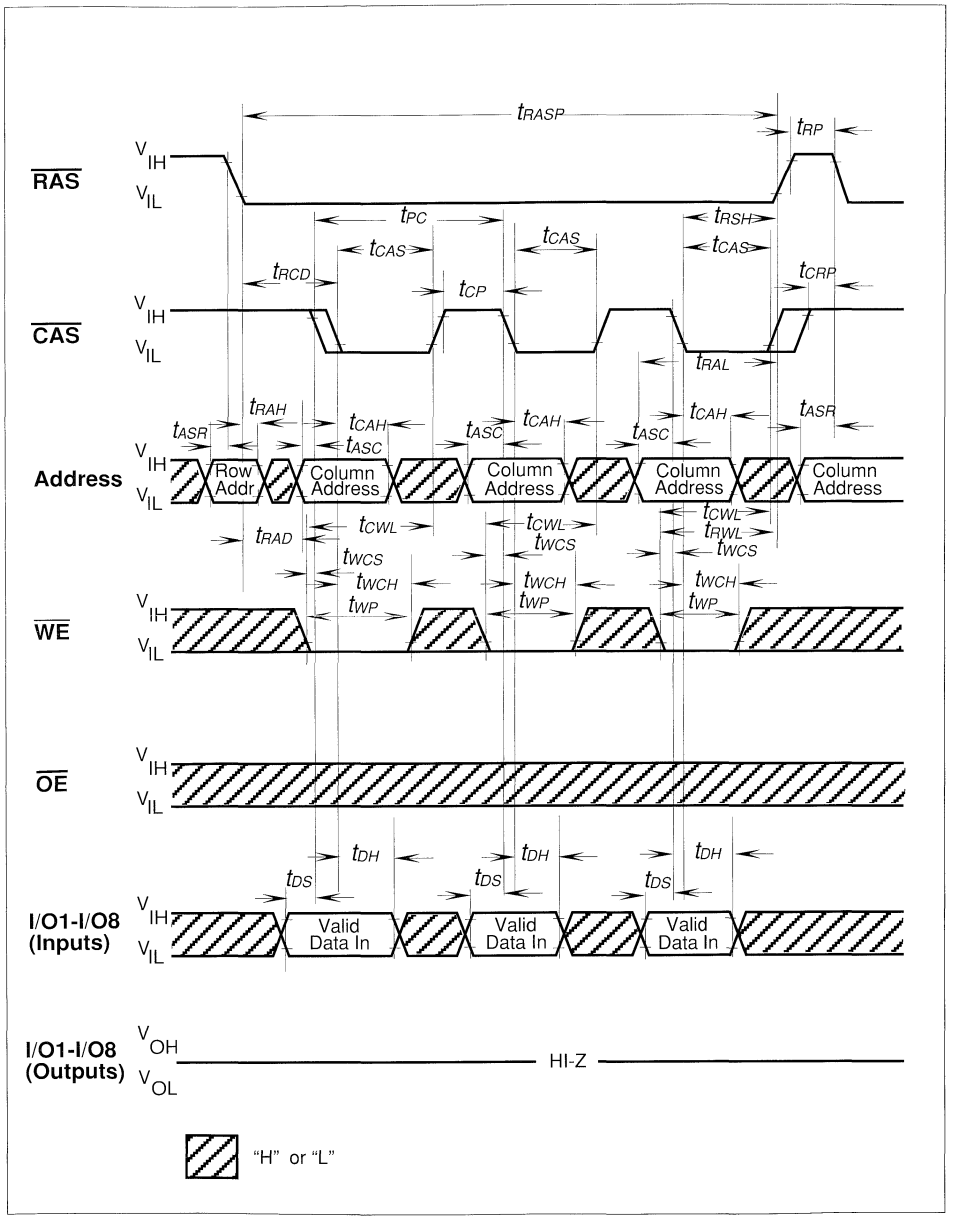
Read-Write (Read-Modify-Write) Cycle



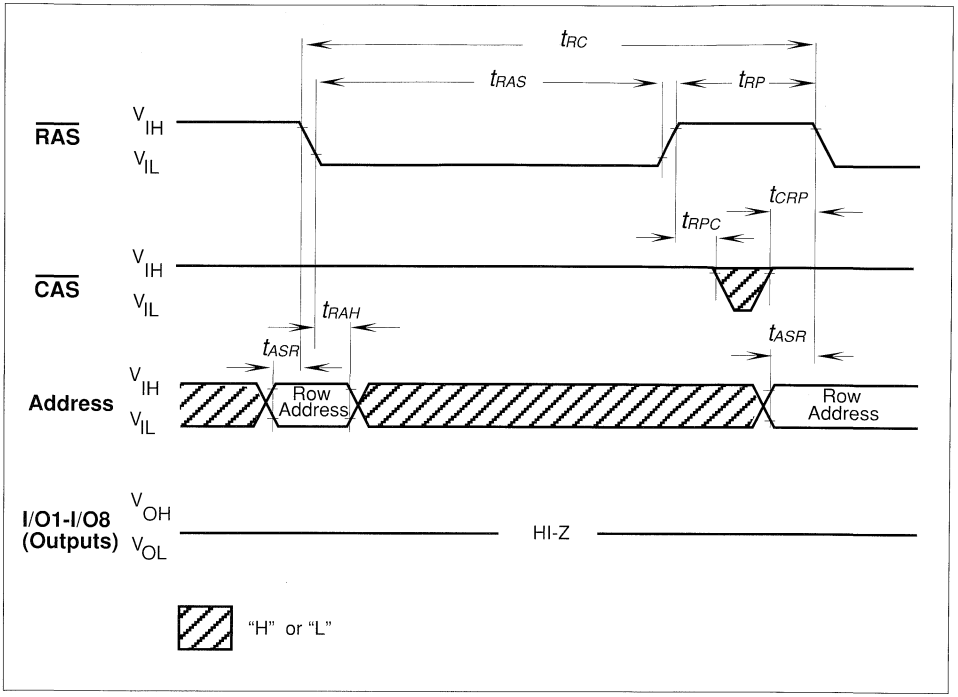
Fast Page Mode Read-Modify-Write Cycle



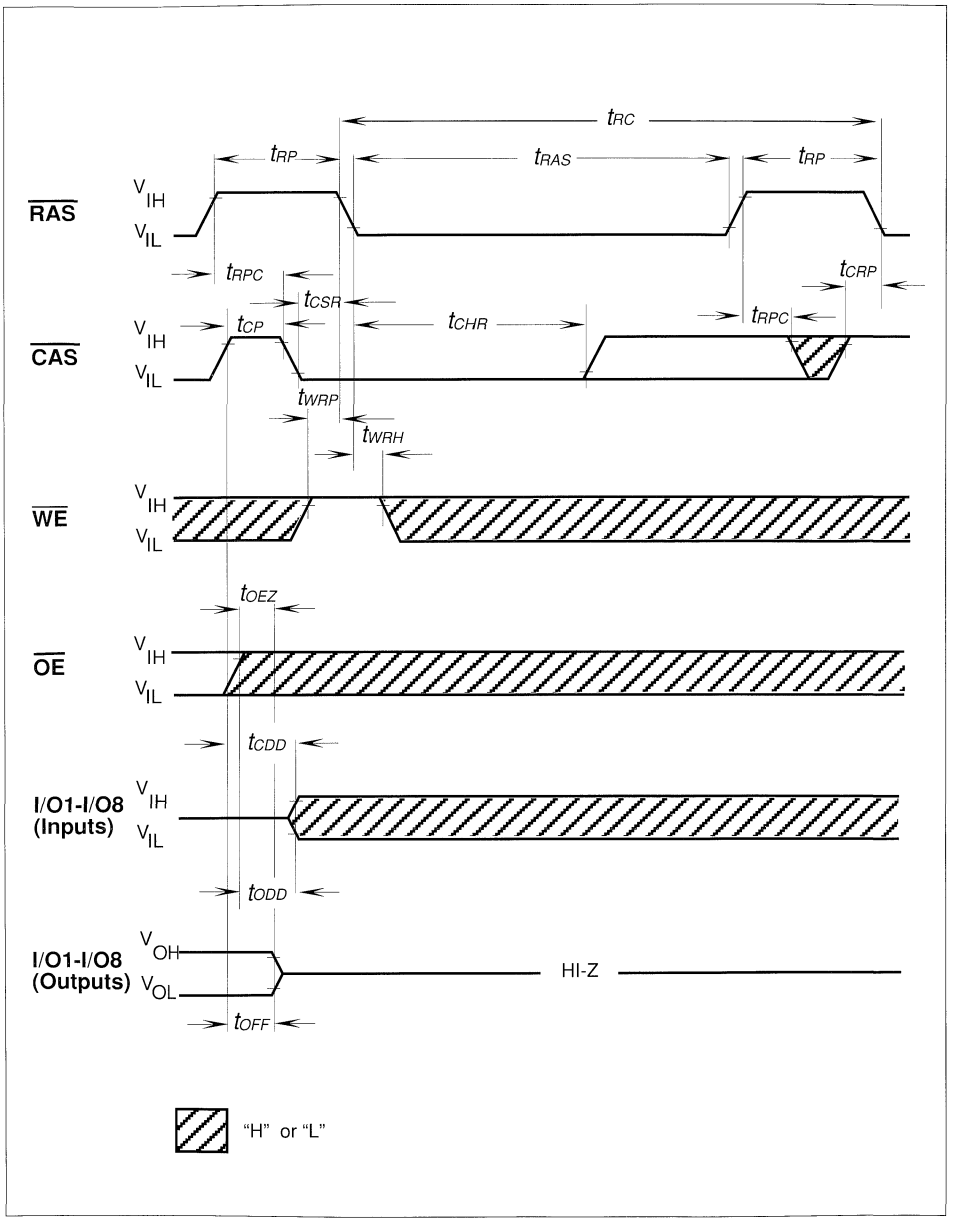
Fast Page Mode Read Cycle



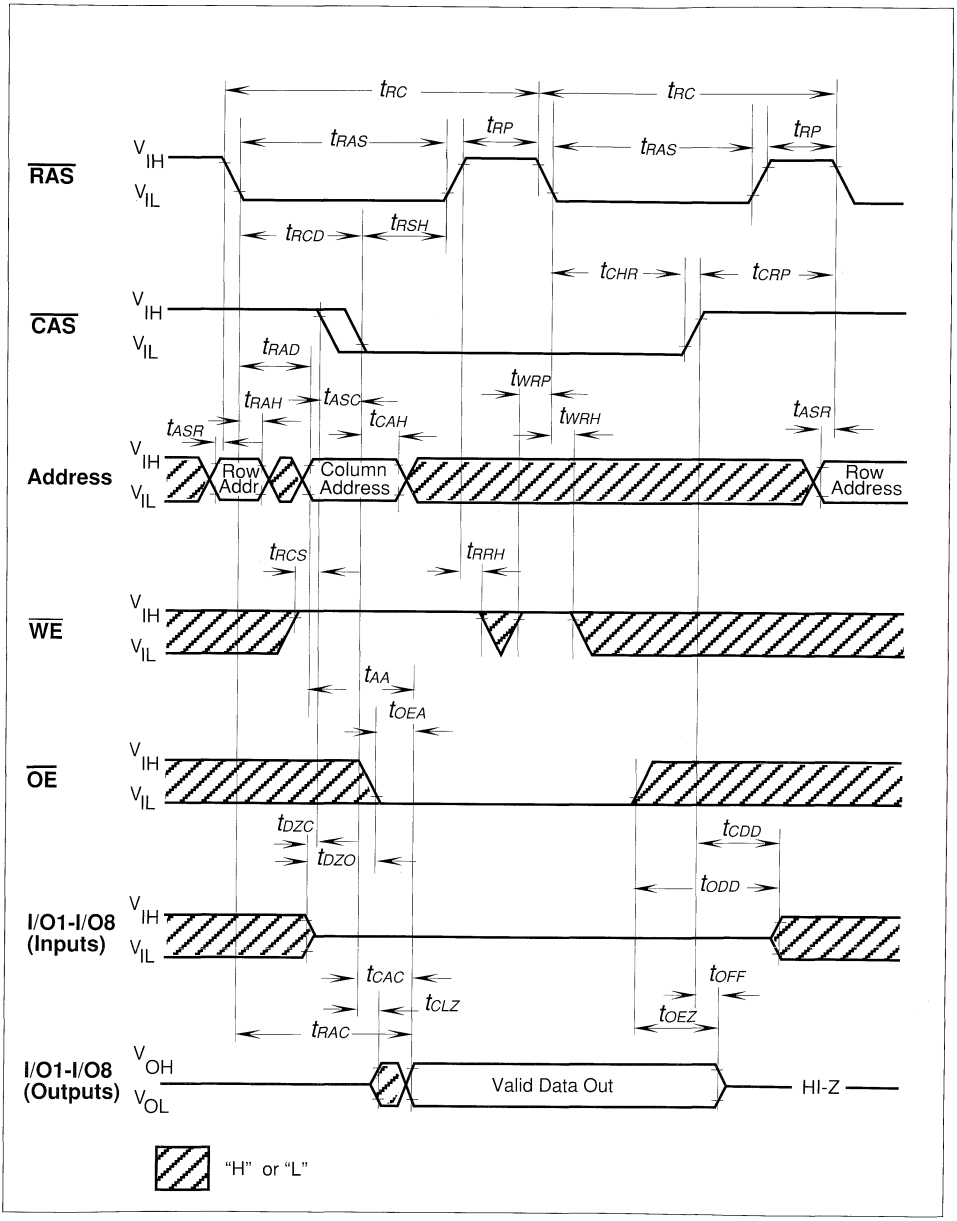
Fast Page Mode Early Write Cycle



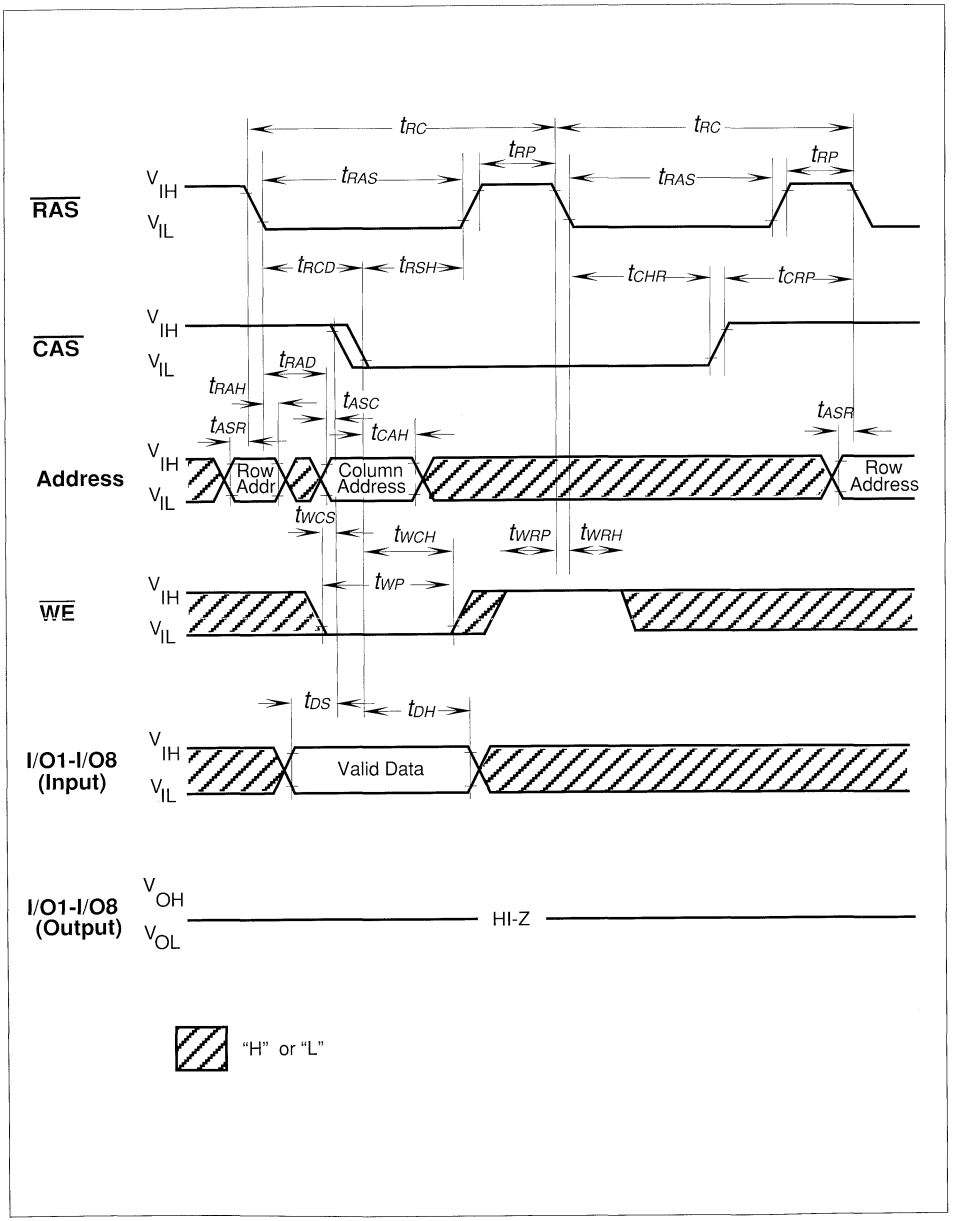
RAS-Only Refresh Cycle



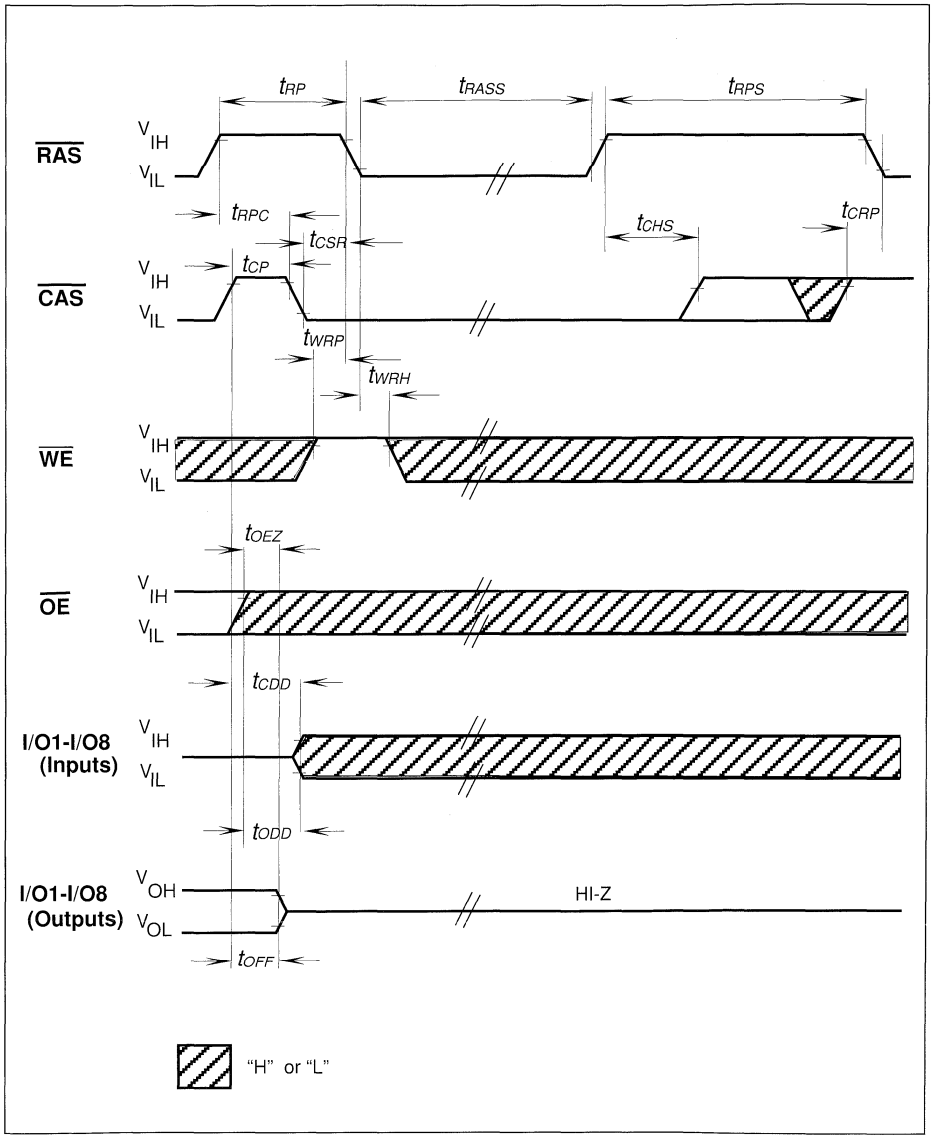
CAS-Before-RAS Refresh Cycle



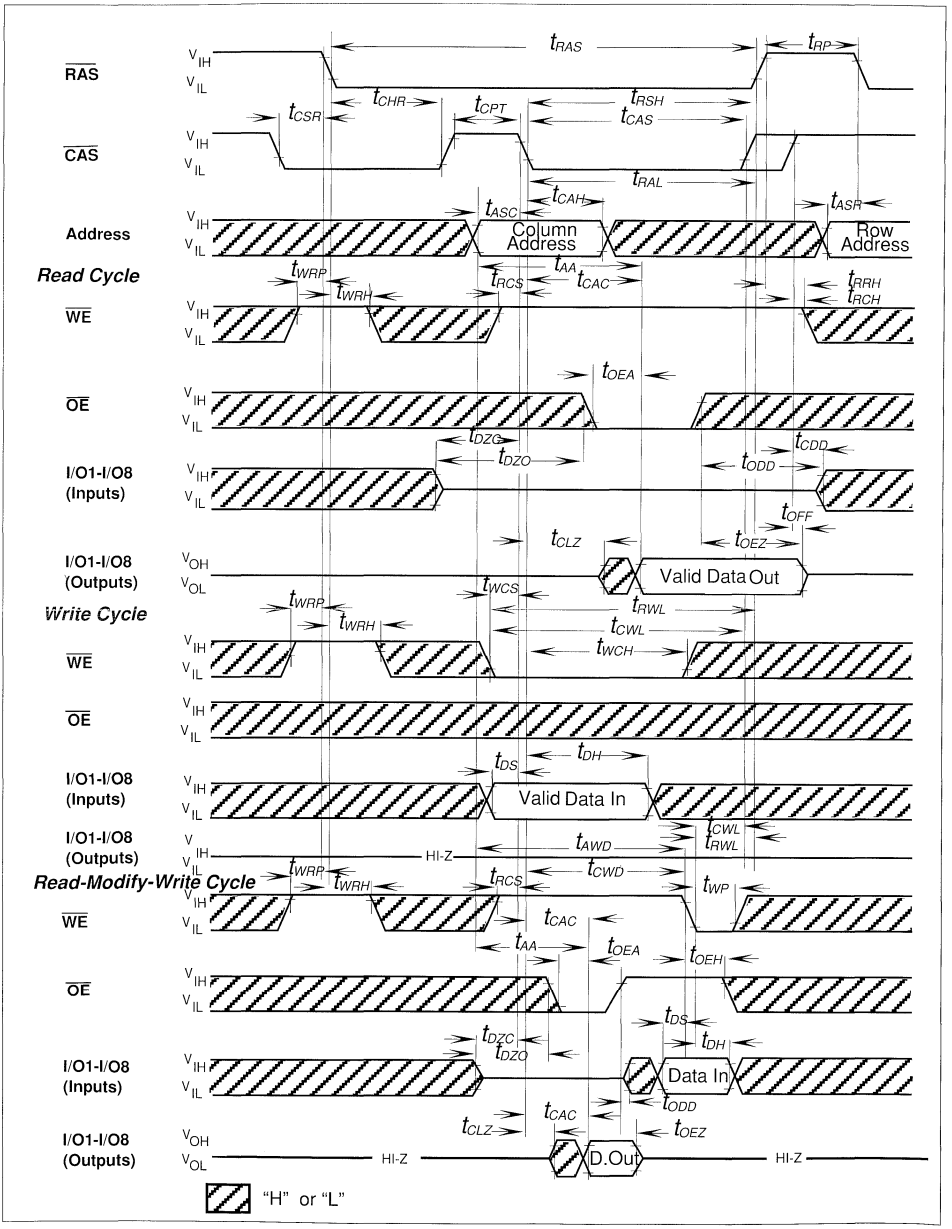
Hidden Refresh Cycle (Read)



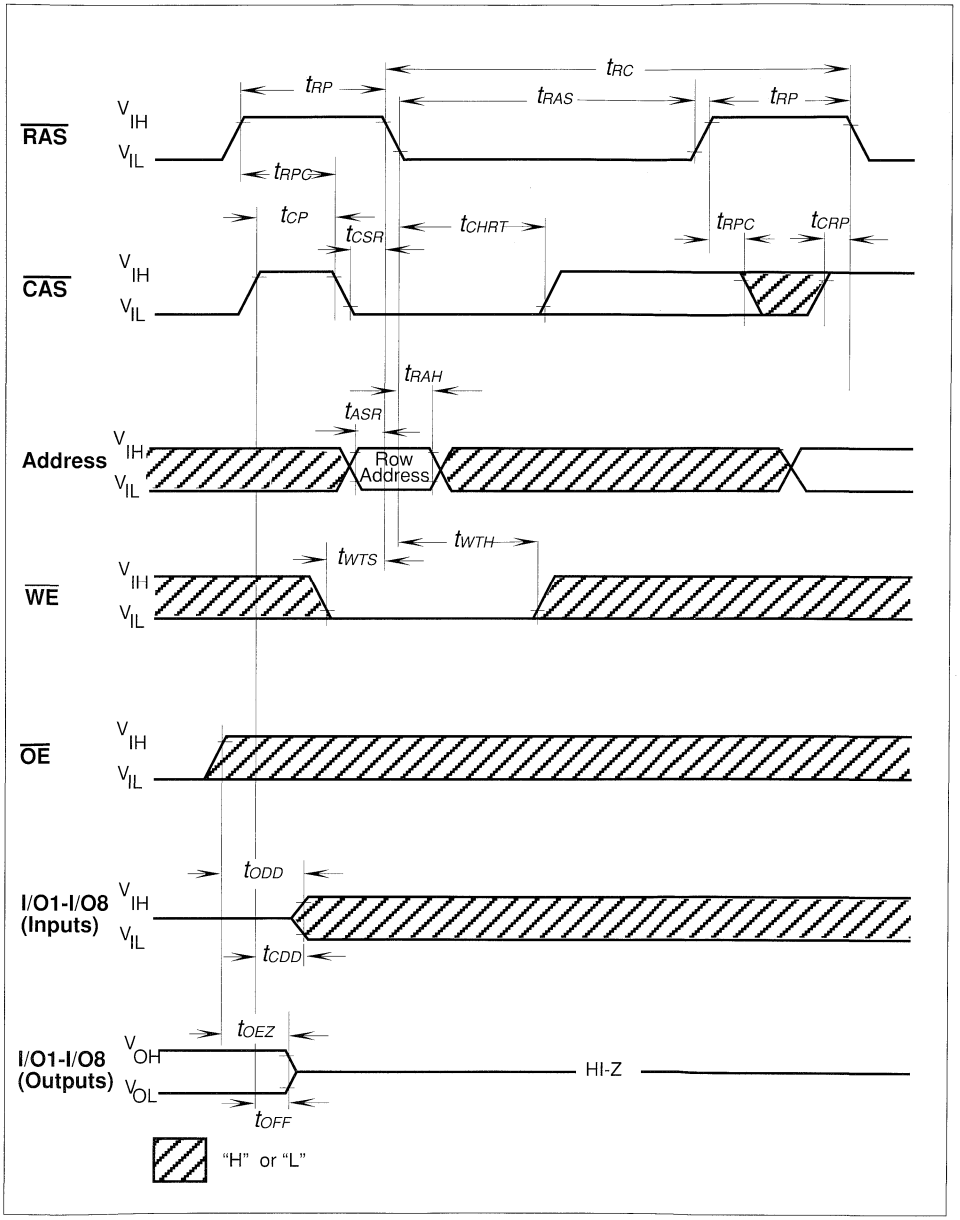
Hidden Refresh Cycle (Early Write)



Self Refresh



CAS-Before-RAS Refresh Counter Test Cycle



Test Mode Entry

Test Mode

As the HYB 5117800BSJ is organized internally as 1M x 16-bits, a test mode cycle using 2:1 compression can be used to improve test time. Note that in the 2M x 8 version the test time is reduced by 1/2 for a N test pattern.

In a test mode "write" the data from each I/O pin is written into two 1M blocks simultaneously (all "1" s or all "0" s). In test mode "read" each I/O output is used for indicating the test mode result. If the internal two bits are equal, the I/O would indicate a "1". If they were not equal, the I/O would indicate a "0". The WCBR cycle ($\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$) puts the device into test mode. To exit from test mode, a "$\overline{CAS}$ before $\overline{RAS}$ refresh", "$\overline{RAS}$ only refresh" or "Hidden refresh" can be used. Refresh during test mode operation can be performed by normal read cycles or by WCBR refresh cylces.

Row addresses A0 through A9 have to kept high to perform a testmode entry cycle. All other addresses are don't care.

2M x 8 - Bit Dynamic RAM
2k Refresh
(Hyper Page Mode - EDO)

HYB 5117805BSJ -50/-60/-70

Preliminary Information

- 2 097 152 words by 8-bit organization
- 0 to 70 °C operating temperature
- Fast access and cycle time
  RAS access time:
  50 ns (-50 version)
  60 ns (-60 version)
  70 ns (-70 version)
  Cycle time:
  89 ns (-50 version)
  104 ns (-60 version)
  124 ns (-70 version)
  CAS access time:
  12 ns (-50 version)
  15 ns (-60 version)
  20 ns (-70 version)
- Hyper page mode (EDO) cycle time
  20 ns (-50 version)
  25 ns (-60 version)
  30 ns (-70 version)
- Single + 5 V (± 10 %) supply
- Low power dissipation
  max. 660 mW active (-50 version)
  max. 605 mW active (-60 version)
  max. 550 mW active (-70 version)
  11 mW standby (TTL)
  5.5 mW standby (MOS)
- Output unlatched at cycle end allows two-dimensional chip selection
- Read, write, read-modify-write, CAS-before-RAS refresh, RAS-only refresh, hidden refresh, Self Refresh and test mode
- Hyper page mode (EDO) capability
- All inputs, outputs and clocks fully TTL-compatible
- 2048 refresh cycles / 32 ms (2k-Refresh)
- Plastic Package: P-SOJ-28-3 400 mil

Ordering Information

Type	Ordering Code	Package	Descriptions
HYB 5117805BJ-50	Q67100-Q1104	P-SOJ-28-3 400 mil	DRAM (access time 50 ns)
HYB 5117805BJ-60	Q67100-Q1105	P-SOJ-28-3 400 mil	DRAM (access time 60 ns)
HYB 5117805BJ-70	Q67100-Q1106	P-SOJ-28-3 400 mil	DRAM (access time 70 ns)

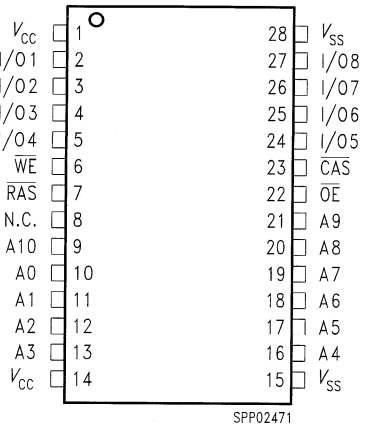
The HYB 5117805BSJ is the new generation dynamic RAM organized as 2 097 152 words by 8-bits. The HYB 5117805BSJ utilizes a submicron CMOS silicon gate process technology, as well as advanced circuit techniques to provide wide operating margins, both internally and for the system user. Multiplexed address inputs permit the HYB 5117805BSJ to be packaged in a standard SOJ 28 plastic package with 400 mil width. These packages provide high system bit densities and are compatible with commonly used automatic testing and insertion equipment. System-oriented features include single + 5 V (± 10 %) power supply, direct interfacing with high-performance logic device families such as Schottky TTL.

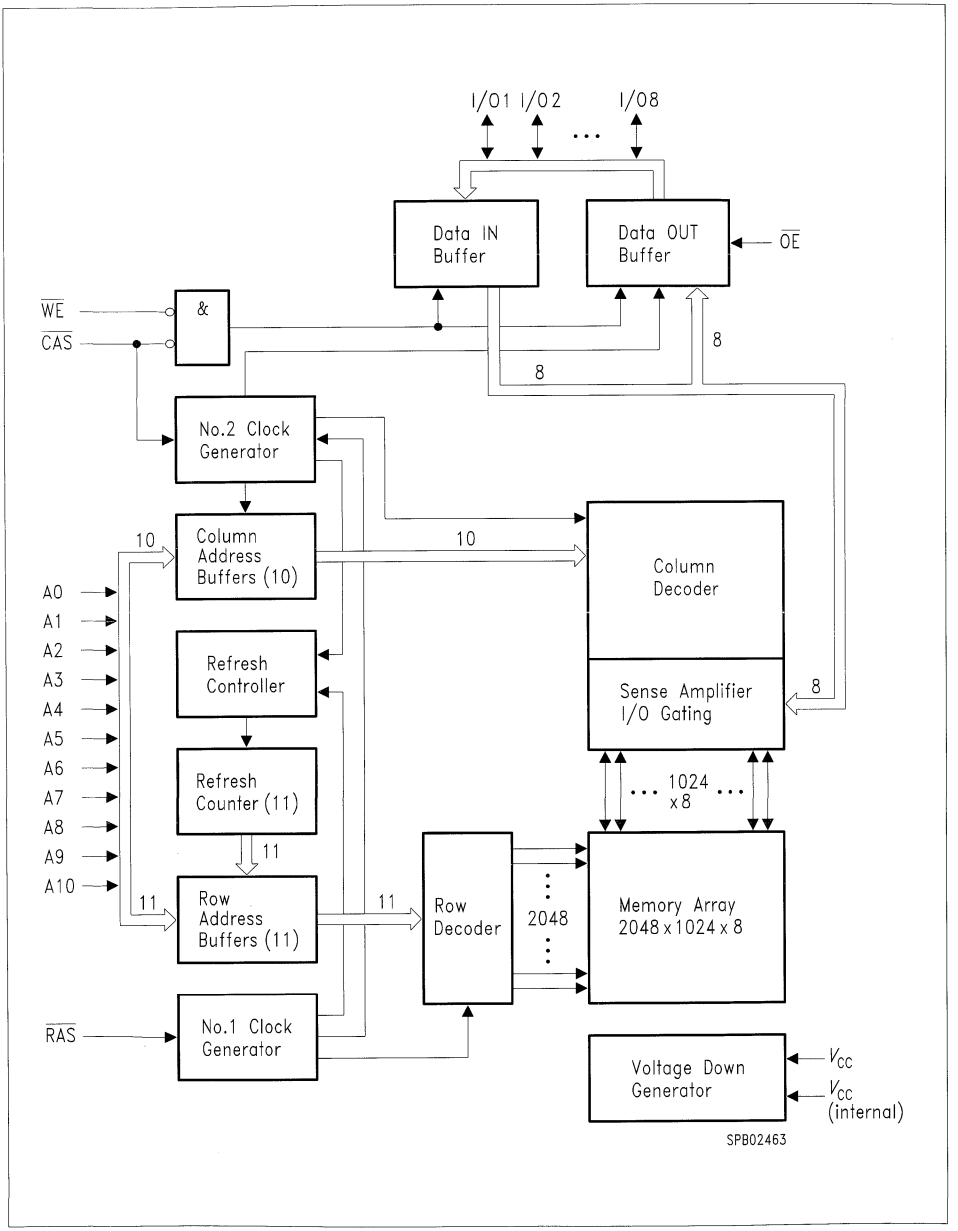
Pin Definitions and Functions

Pin No.	Function
A0-A10	Row Address Inputs
A0-A9	Column Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{OE}$	Output Enable
I/O1-I/O8	Data Input/Output
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground (0 V)
N.C.	not connected

Pin Configuration
(top view)

P-SOJ-28-3 400 mil





Block Diagram

Absolute Maximum Ratings

Operating temperature range ..... 0 to 70 °C
Storage temperature range ..... – 55 to 150 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 0.5 to min (V_{CC} + 0.5, 7.0) V
Power supply voltage ..... – 1.0 V to 7.0 V
Power dissipation ..... 1.0 W
Data out current (short circuit) ..... 50 mA

Note:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 5 V ± 10 %; t_T = 2 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	V_{CC} + 0.5	V	1)
Input low voltage	V_{IL}	– 0.5	0.8	V	1)
Output high voltage (I_{OUT} = – 5 mA)	V_{OH}	2.4	–	V	1)
Output low voltage (I_{OUT} = 4.2 mA)	V_{OL}	–	0.4	V	1)
Input leakage current (0 V ≤ V_{IH} ≤ V_{CC} + 0.3 V, all other pins = 0 V)	$I_{I(L)}$	– 10	10	µA	1)
Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ V_{CC} + 0.3 V)	$I_{O(L)}$	– 10	10	µA	1)
Average V_{CC} supply current:	I_{CC1}				
-50 ns version		–	120	mA	2) 3) 4)
-60 ns version		–	110	mA	2) 3) 4)
-70 ns version		–	100	mA	2) 3) 4)
($\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = t_{RC} min.)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	2	mA	–
Average V_{CC} supply current, during $\overline{RAS}$-only refresh cycles:	I_{CC3}				
-50 ns version		–	120	mA	2) 4)
-60 ns version		–	110	mA	2) 4)
-70 ns version		–	100	mA	2) 4)
($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)					

DC Characteristics (cont'd)

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 5 V ± 10 %; t_T = 2 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current, during hyper page mode: -50 ns version -60 ns version -70 ns version ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling: t_{PC} = t_{PC} min.)	I_{CC4}	 – – –	 90 80 70	 mA mA mA	 2) 3) 4) 2) 3) 4) 2) 3) 4)
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	–	1	mA	1)
Average V_{CC} supply current, during $\overline{CAS}$-before-RAS refresh mode: -50 ns version -60 ns version -70 ns version ($\overline{RAS}$, $\overline{CAS}$ cycling: t_{RC} = t_{RC} min.)	I_{CC6}	 – – –	 120 110 100	 mA mA mA	 2) 4) 2) 4) 2) 4)
Average Self Refresh Current ($\overline{CBR}$ cycle with t_{RAS} > t_{RASS} min., $\overline{CAS}$ held low, $\overline{WE}$ = V_{CC} - 0.2 V, Address and Din = V_{CC} - 0.2 V or 0.2 V)	I_{CC7}	–	1	mA	

AC Characteristics [5)7)]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 2 ns

Parameter	Symbol	Limit Values						Unit
		HYB 5117805BSJ-50		HYB 5117805BSJ-60		HYB 5118805BSJ-70		
		min.	max.	min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	89	–	104	–	124	–	ns
Read-write cycle time	t_{RWC}	117	–	138	–	162	–	ns
Hyper page mode (EDO) cycle time	t_{HPC}	20	–	25	–	30	–	ns
Hyper page mode (EDO) read-write cycle time	t_{PRWC}	57	–	68	–	77	–	ns
Access time from $\overline{RAS}$ [7) 12)]	t_{RAC}	–	50	–	60	–	70	ns
Access time from $\overline{CAS}$ [7) 12)]	t_{CAC}	–	12	–	15	–	17	ns
Access time from column address [7) 13)]	t_{AA}	–	25	–	30	–	35	ns
Access time from $\overline{CAS}$ precharge [7)]	t_{CPA}	–	27	–	32	–	37	ns
$\overline{CAS}$ to output in low-Z [7)]	t_{CLZ}	0	–	0	–	0	–	ns
Output buffer turn-off delay [8) 18)]	t_{OFF}	0	15	0	15	0	20	ns
Transition time (rise and fall) [6)]	t_T	1	50	1	50	1	50	ns
$\overline{RAS}$ precharge time	t_{RP}	35	–	40	–	50	–	ns
$\overline{RAS}$ pulse width	t_{RAS}	50	10k	60	10k	70	10k	ns
$\overline{RAS}$ pulse width (Hyper page mode- EDO)	t_{RASP}	50	200k	60	200k	70	200k	ns
$\overline{CAS}$ pulse width	t_{CAS}	7	10k	10	10k	12	10k	ns
$\overline{CAS}$ precharge to $\overline{RAS}$ Delay (Hyper Page Mode)	t_{RHCP}	27	–	32	–	37	–	ns
$\overline{CAS}$ precharge to $\overline{WE}$ (HPM RMW)	t_{CPWD}	41	–	49	–	56	–	ns
$\overline{RAS}$ hold time	t_{RSH}	12		15	–	17	–	ns
$\overline{CAS}$ hold time	t_{CSH}	50		60	–	70	–	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time [12)]	t_{RCD}	12	38	14	45	14	53	

AC Characteristics (cont'd) [5)7)]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 2 ns

Parameter	Symbol	Limit Values						Unit
		HYB 5117805BSJ-50		HYB 5117805BSJ-60		HYB 5118805BSJ-70		
		min.	max.	min.	max.	min.	max.	
$\overline{RAS}$ to column address delay time [13)]	t_{RAD}	10	25	12	30	12	35	ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	5	–	ns
$\overline{CAS}$ precharge time	t_{CP}	9	–	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns
Row address hold time	t_{RAH}	8	–	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns
Column address hold time	t_{CAH}	5	–	7	–	10	–	ns
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	–	30	–	35	–	ns
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns
Read command hold time [9)]	t_{RCH}	0	–	0	–	0	–	ns
Read command hold time referenced to $\overline{RAS}$ [9)]	t_{RRH}	0	–	0	–	0	–	ns
Write command hold time	t_{WCH}	5	–	7	–	10	–	ns
Write command pulse width	t_{WP}	5	–	7	–	10	–	ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	12	–	15	–	17	–	ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	12	–	15	–	17	–	ns
Data setup time [10)]	t_{DS}	0	–	0	–	0	–	ns
Data hold time [10)]	t_{DH}	5	–	7	–	10	–	ns
Refresh period	t_{REF}	–	32	–	32	–	32	ms
Write command setup time [11)]	t_{WCS}	0	–	0	–	0	–	ns
$\overline{CAS}$ to $\overline{WE}$ delay time [11)]	t_{CWD}	26	–	32	–	36	–	ns
$\overline{RAS}$ to WE delay time [11)]	t_{RWD}	64	–	77	–	89	–	ns
Column address to $\overline{WE}$ delay time [11)]	t_{AWD}	39	–	47	–	54	–	ns

AC Characteristics (cont'd) [5)7)]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 2 ns

Parameter	Symbol	Limit Values						Unit
		HYB 5117805BSJ-50		HYB 5117805BSJ-60		HYB 5118805BSJ-70		
		min.	max.	min.	max.	min.	max.	
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CSR}	10	–	10	–	10	–	ns
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CHR}	10	–	10	–	10	–	ns
$\overline{CAS}$ hold time (Test mode entry cycle)	t_{CHRT}	30	–	30	–	30	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5	–	5	–	5	–	ns
$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ counter test cycle)	t_{CPT}	35	–	40	–	40	–	ns
Write command setup time (in test mode entry cycle)	t_{WTS}	10	–	10	–	10	–	ns
Write command hold time (in test mode entry cycle)	t_{WTH}	10	–	10	–	10	–	ns
Write to $\overline{RAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{WRP}	10	–	10	–	10	–	ns
Write hold time referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{WRH}	10	–	10	–	10	–	ns
Output data hold time	t_{COH}	5	–	5	–	5	–	ns
$\overline{OE}$ command hold time	t_{OEH}	12	–	15	–	17	–	ns
$\overline{OE}$ access time	t_{OEA}	–	12	–	15	–	17	ns
Output buffer turn-off delay from $\overline{OE}$	t_{OEZ}	0	12	0	15	0	17	ns
Data to $\overline{CAS}$ low delay [15)]	t_{DZC}	0	–	0	–	0	–	ns
Data to $\overline{OE}$ low delay [15)]	t_{DZO}	0	–	0	–	0	–	ns
$\overline{CAS}$ high to data delay [16)]	t_{CDD}	12	–	15	–	17	–	ns
$\overline{OE}$ high to data delay [16)]	t_{ODD}	12	–	15	–	17	–	ns
$\overline{RAS}$ pulse width during self refresh	t_{RASS}	100k	–	100k	–	100k	–	ns

AC Characteristics (cont'd) [5)7)]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 2 ns

Parameter	Symbol	Limit Values						Unit
		HYB 5117805BSJ-50		HYB 5117805BSJ-60		HYB 5118805BSJ-70		
		min.	max.	min.	max.	min.	max.	
$\overline{RAS}$ precharge time during self refresh	t_{RPS}	95	–	110	–	130	–	ns
$\overline{CAS}$ hold time during self refresh	t_{CHS}	– 50	–	– 50	–	– 50	–	ns

Capacitance

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A10)	C_{I1}	–	5	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}	–	7	pF
I/O capacitance (I/O1-I/O8)	C_{IO}	–	7	pF

Notes:

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.

4) Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4} it can be changed once or less during a hyper page mode cycle (t_{HPC}).

5) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6) $V_{IH\ (min.)}$ and $V_{IL\ (max.)}$ are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.

7) Measured with a load equivalent to 2 TTL gates and 50 pF (V_{ol} = 0.8 V and V_{oh} = 2.0 V).

8) $t_{OFF\ (max.)}$ and $t_{OEZ\ (max.)}$ define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.

9) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

10) These parameters are referenced to the CAS leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.

11) t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS\ (min.)}$, the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} > t_{RWD\ (min.)}$, $t_{CWD} > t_{CWD\ (min.)}$, $t_{AWD} > t_{AWD\ (min.)}$ and $t_{CPWD} > t_{CPWD\ (min.)}$, the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.

12) Operation within the $t_{RCD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RCD\ (max.)}$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD\ (max.)}$ limit, then access time is controlled by t_{CAC}.

13) Operation within the $t_{RAD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RAD\ (max.)}$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD\ (max.)}$ limit, then access time is controlled by t_{AA}.

14) AC measurements assume t_T = 2 ns.

15) Either t_{DZC} or t_{DZO} must be satisfied.

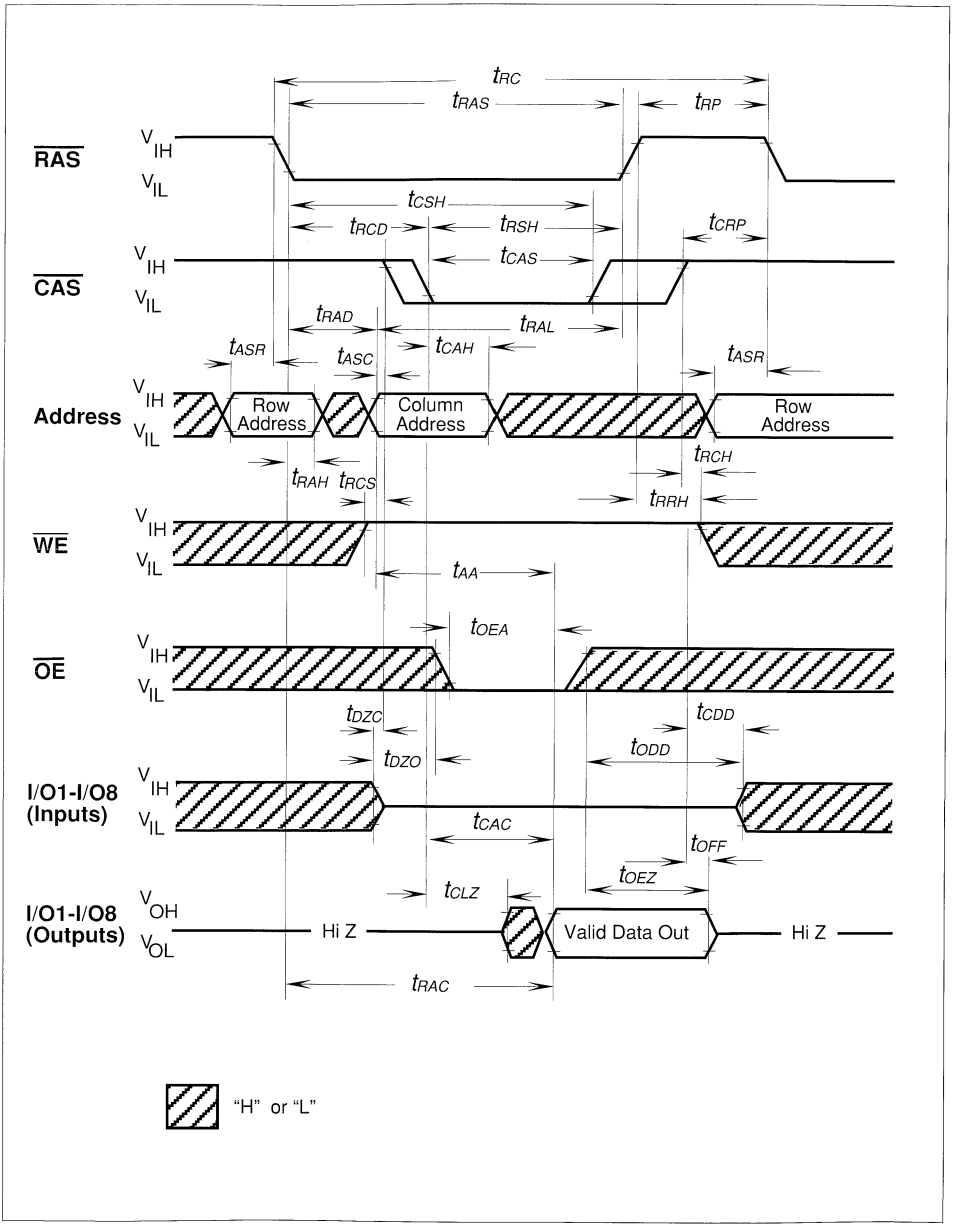
16) Either t_{CDD} or t_{ODD} must be satisfied.

17) When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:

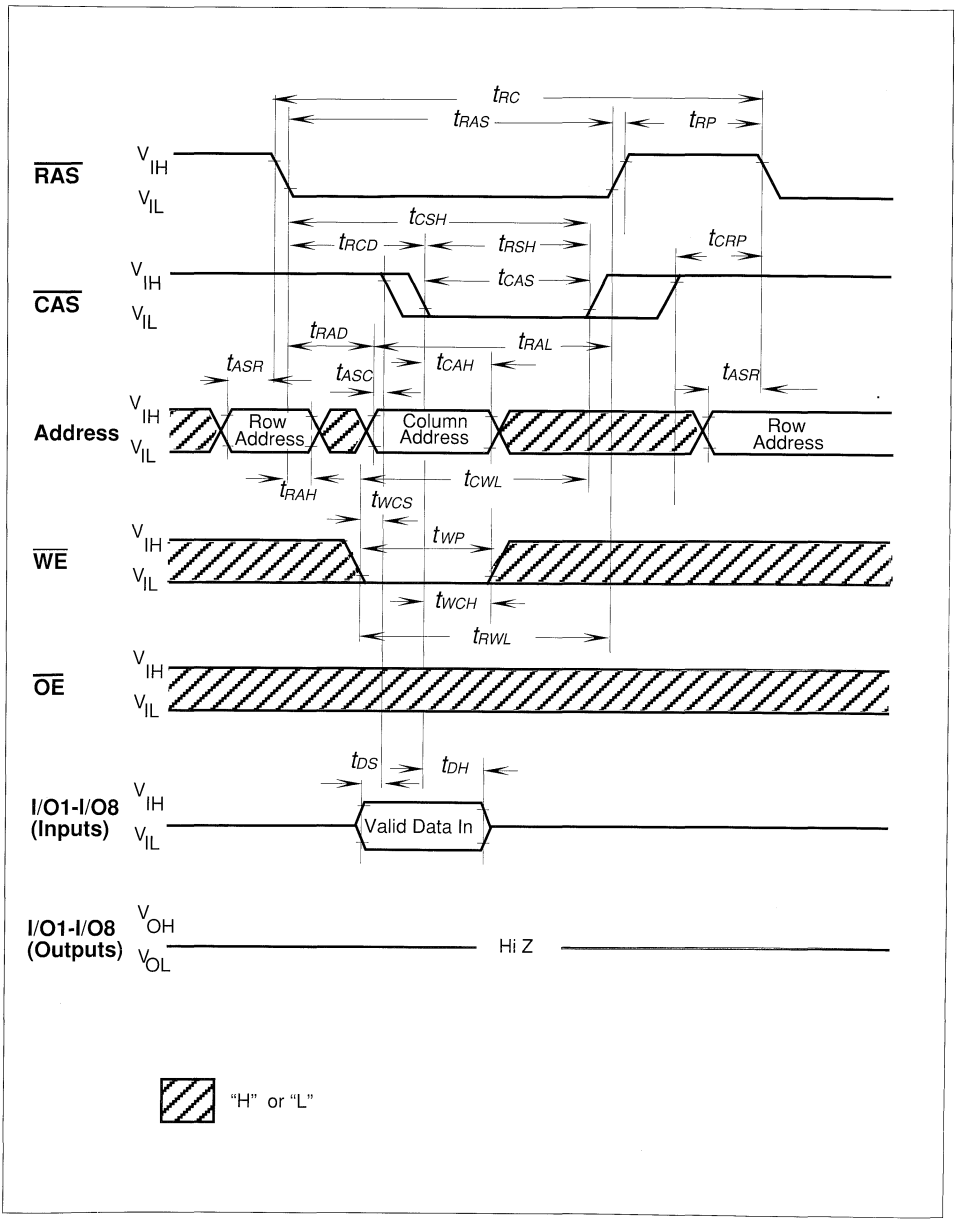
    If row addresses are being refreshed on an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh.

    If row addresses are being refreshed in any other manner (ROR - Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh.

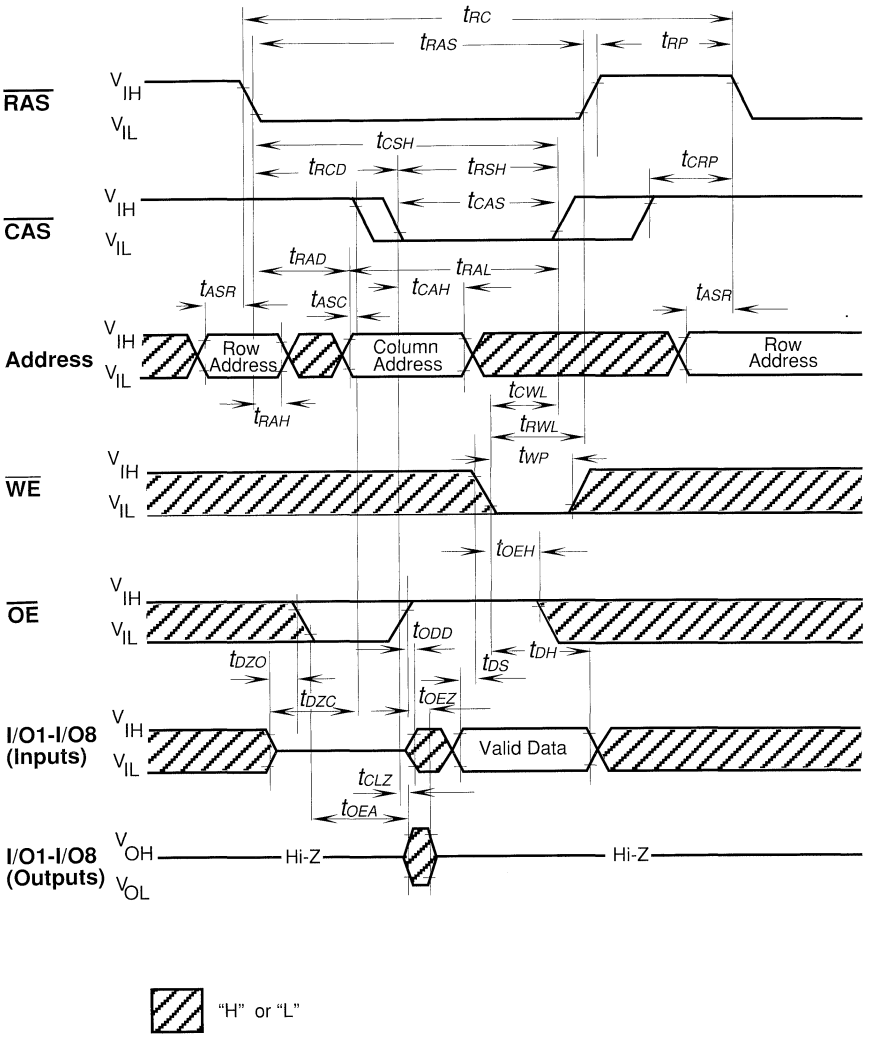
18) t_{off} is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
tCAS
CAS
tRAD
tRAL
tASR
tASC
tCAH
tASR
Address
Row Address
Column Address
Row Address
tRCH
tRAH
tRCS
tRRH
WE
tAA
tOEA
OE
tDZC
tCDD
tDZO
tODD
I/O1-I/O8 (Inputs)
tCAC
tOFF
tOEZ
tCLZ
I/O1-I/O8 (Outputs)
VOH
VOL
Hi Z
Valid Data Out
Hi Z
tRAC
"H" or "L"

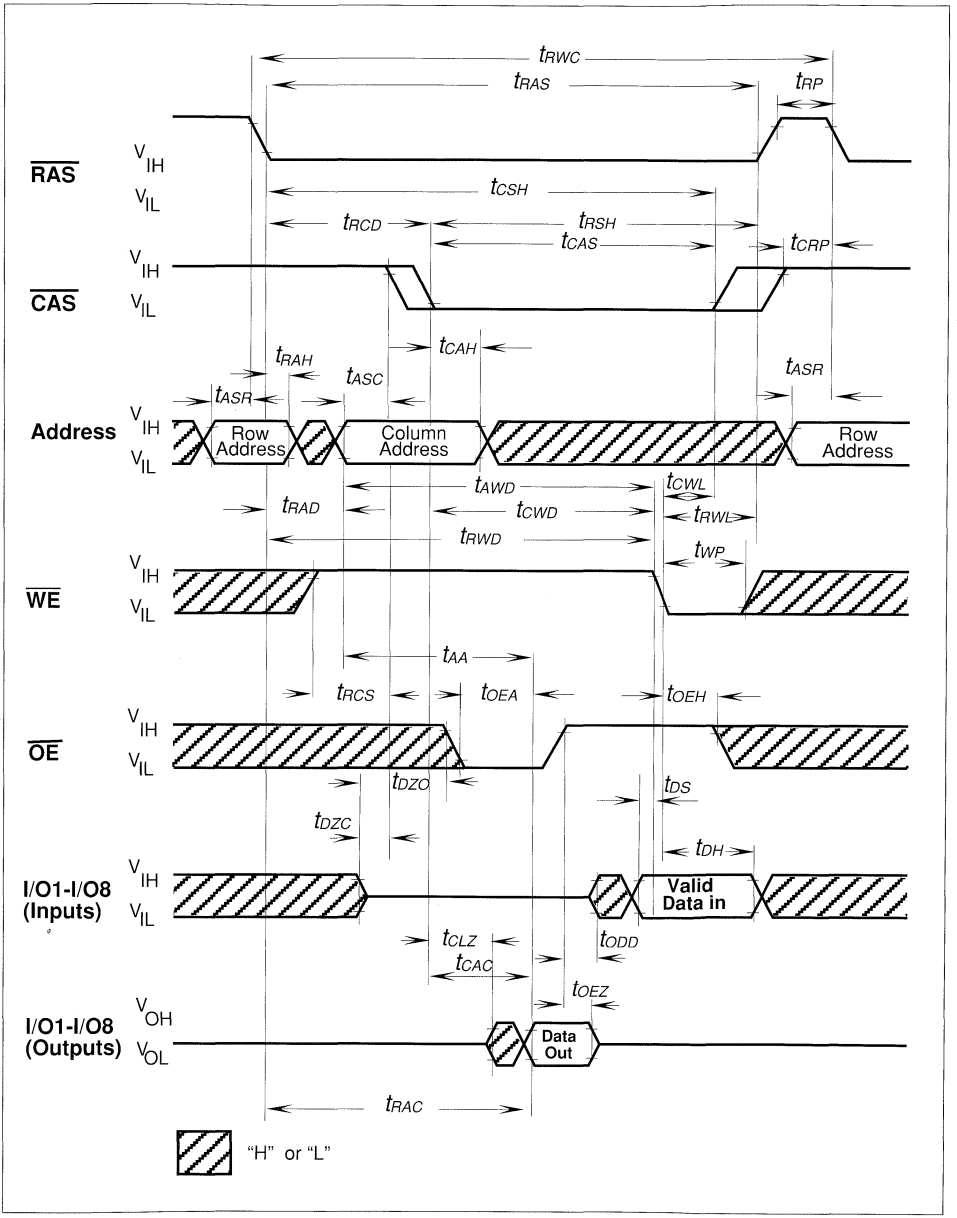
Read Cycle



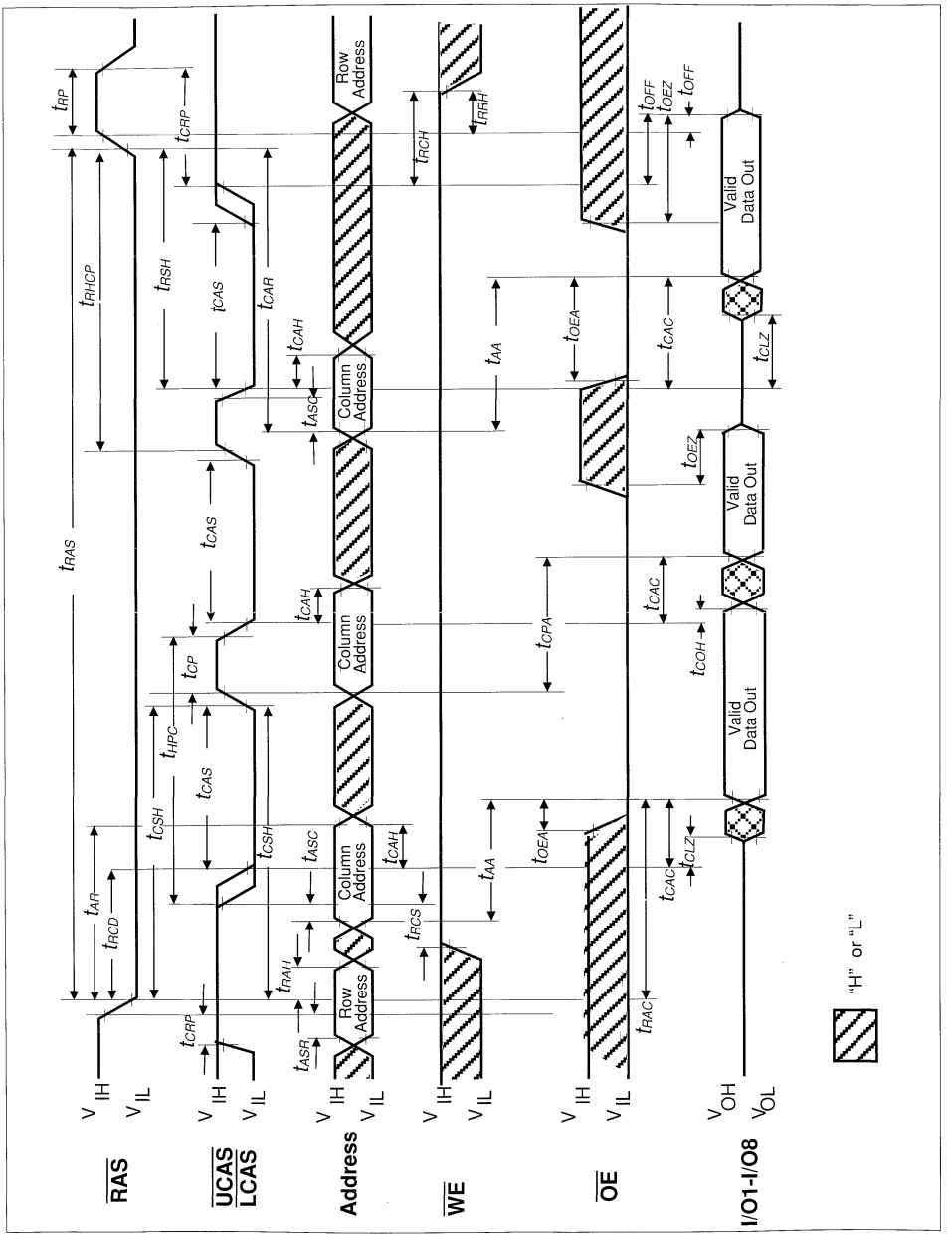
Write Cycle (Early Write)



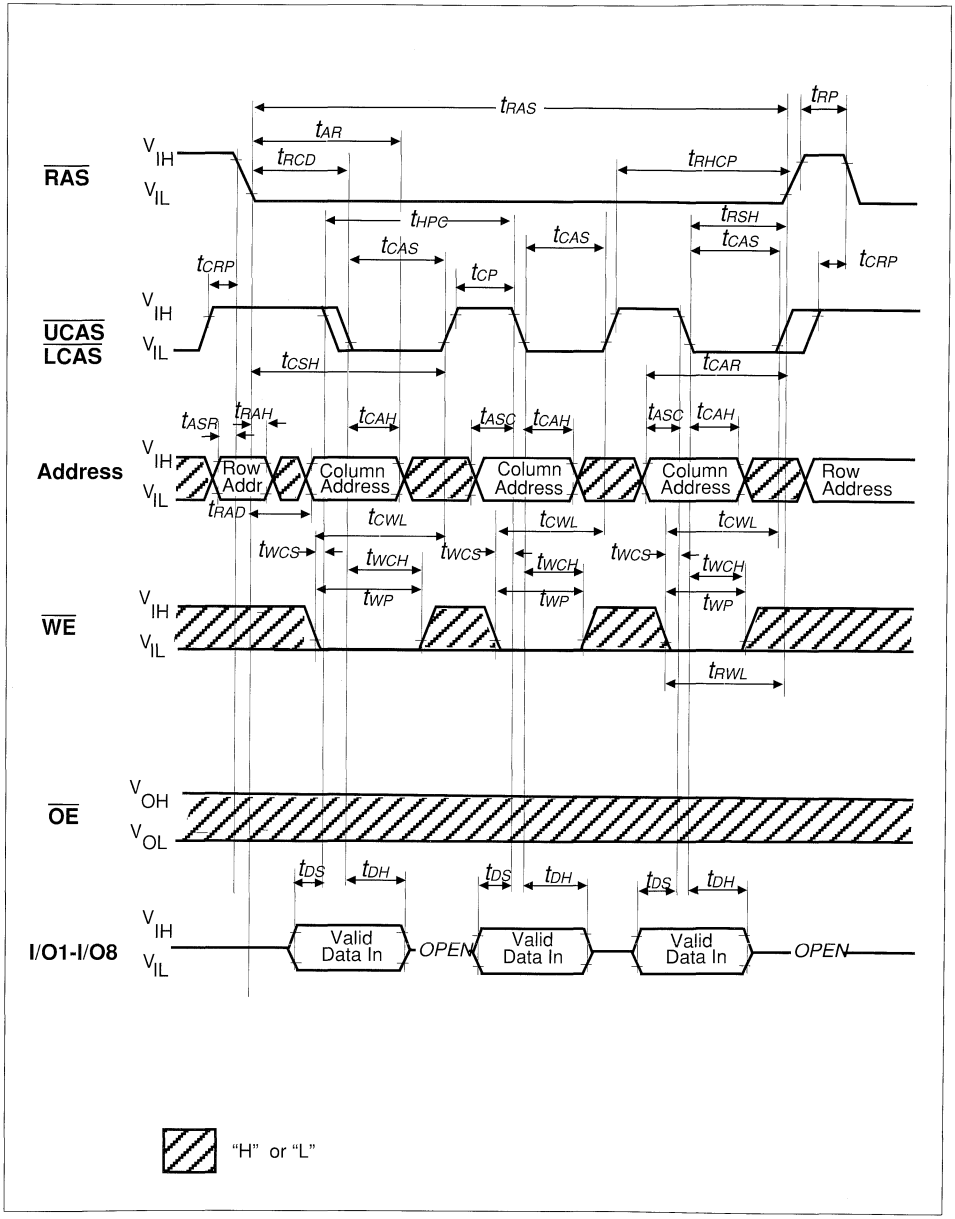
Write Cycle ($\overline{OE}$ Controlled Write)



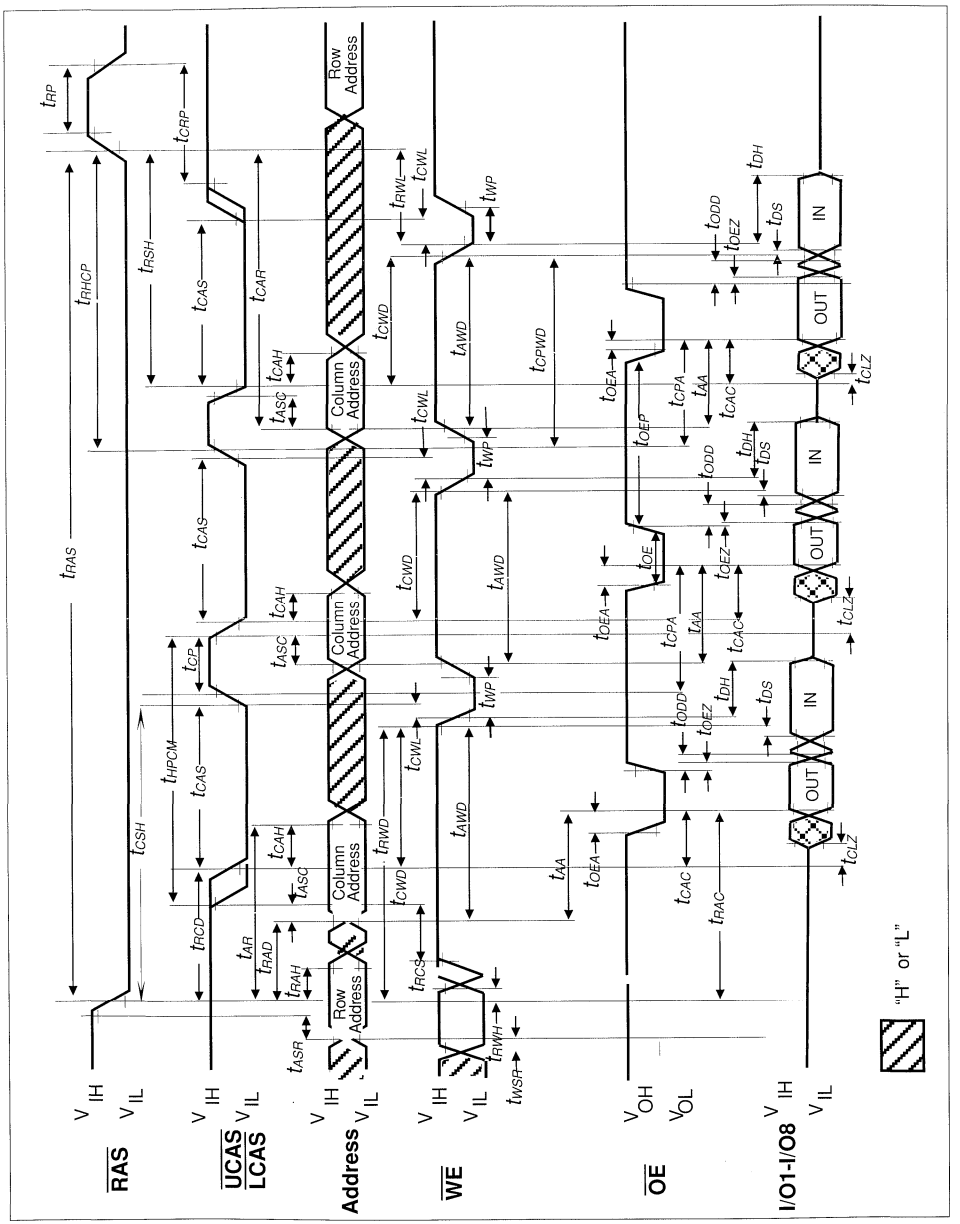
Read-Write (Read-Modify-Write) Cycle



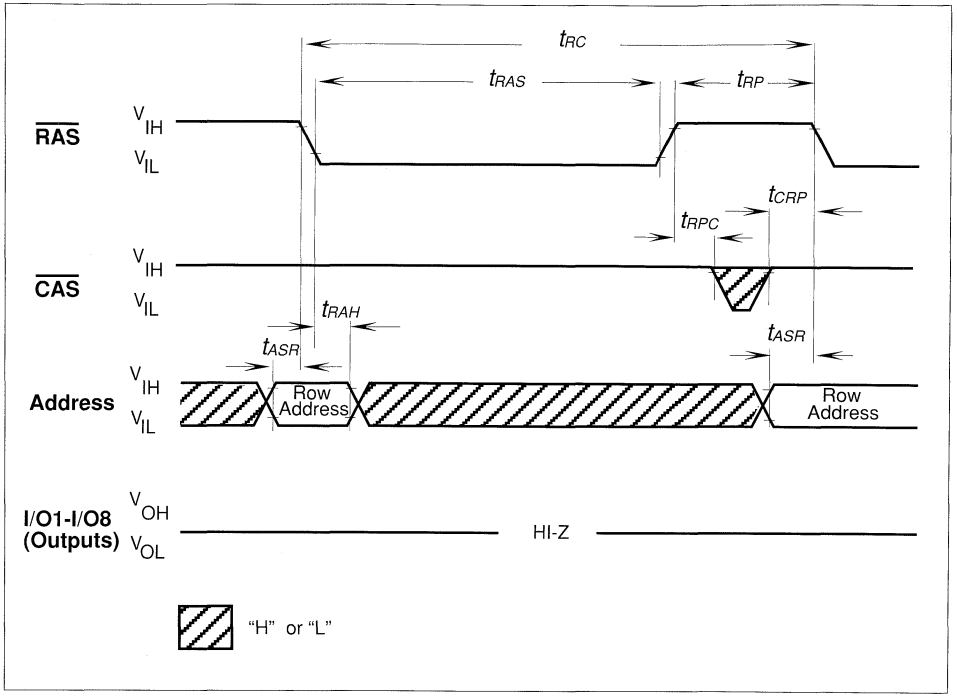
Hyper Page Mode (EDO) Read Cycle



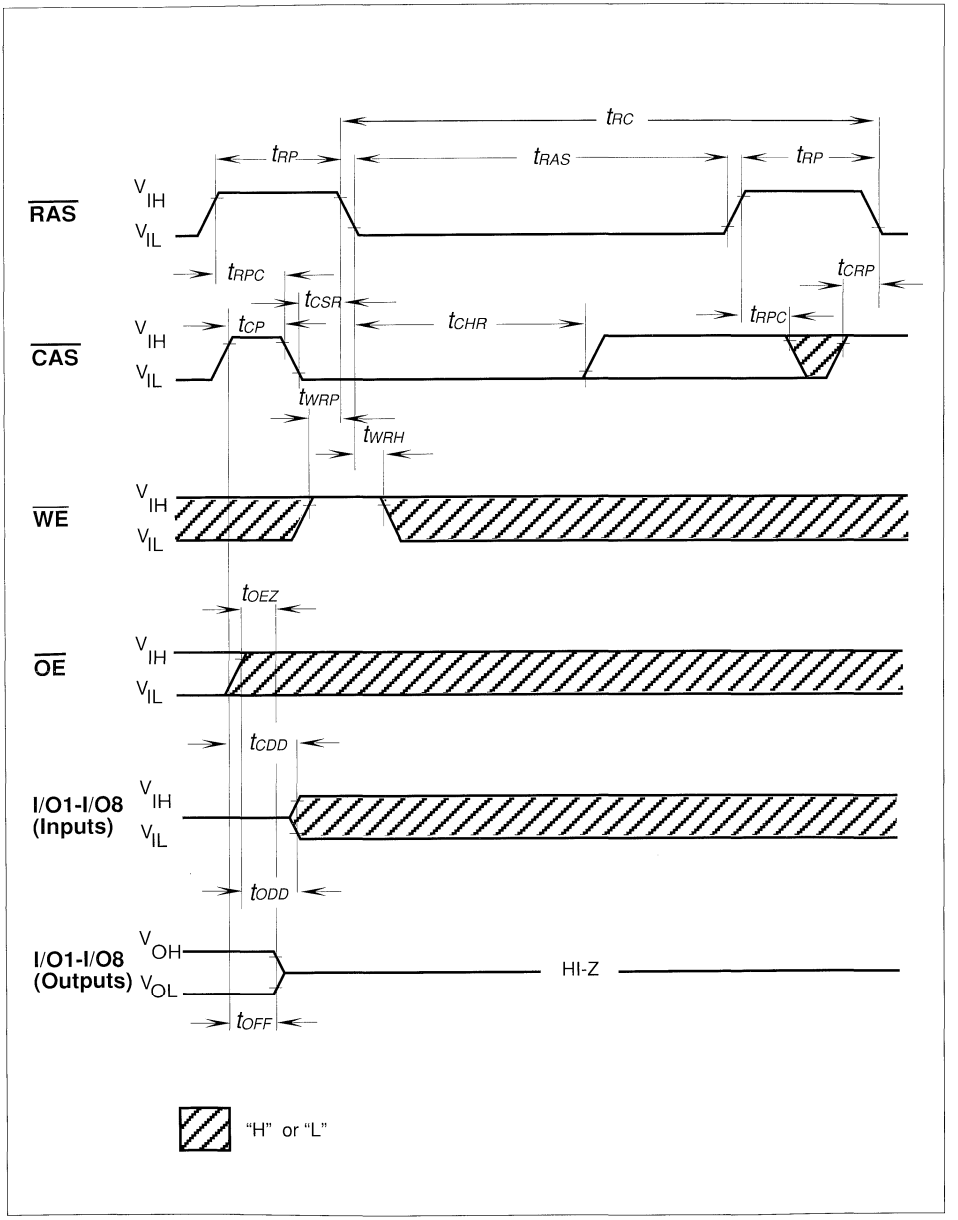
Hyper Page Mode (EDO) Write Cycle



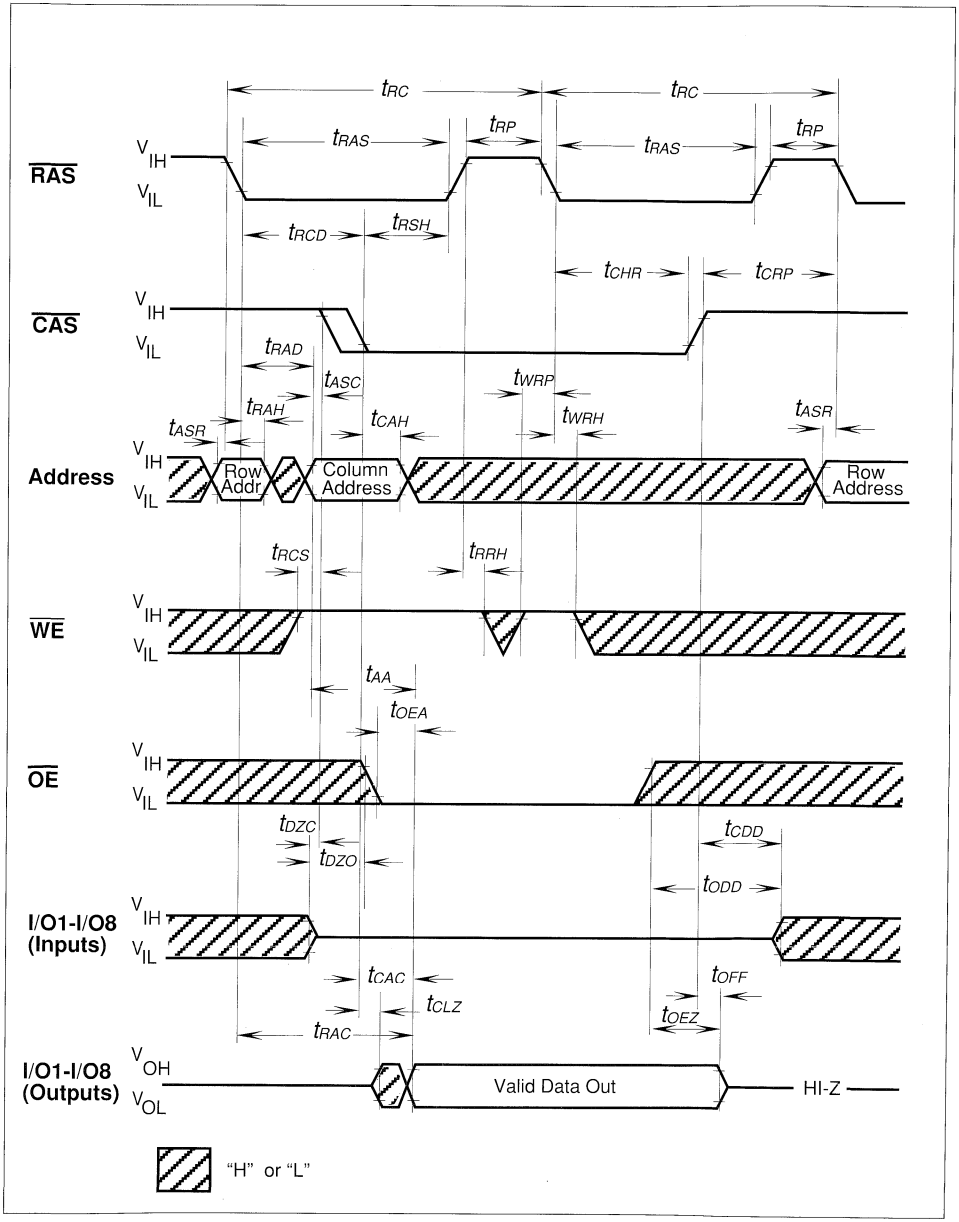
Hyper Page Mode (EDO) Late Write and Read-Modify Write Cycle



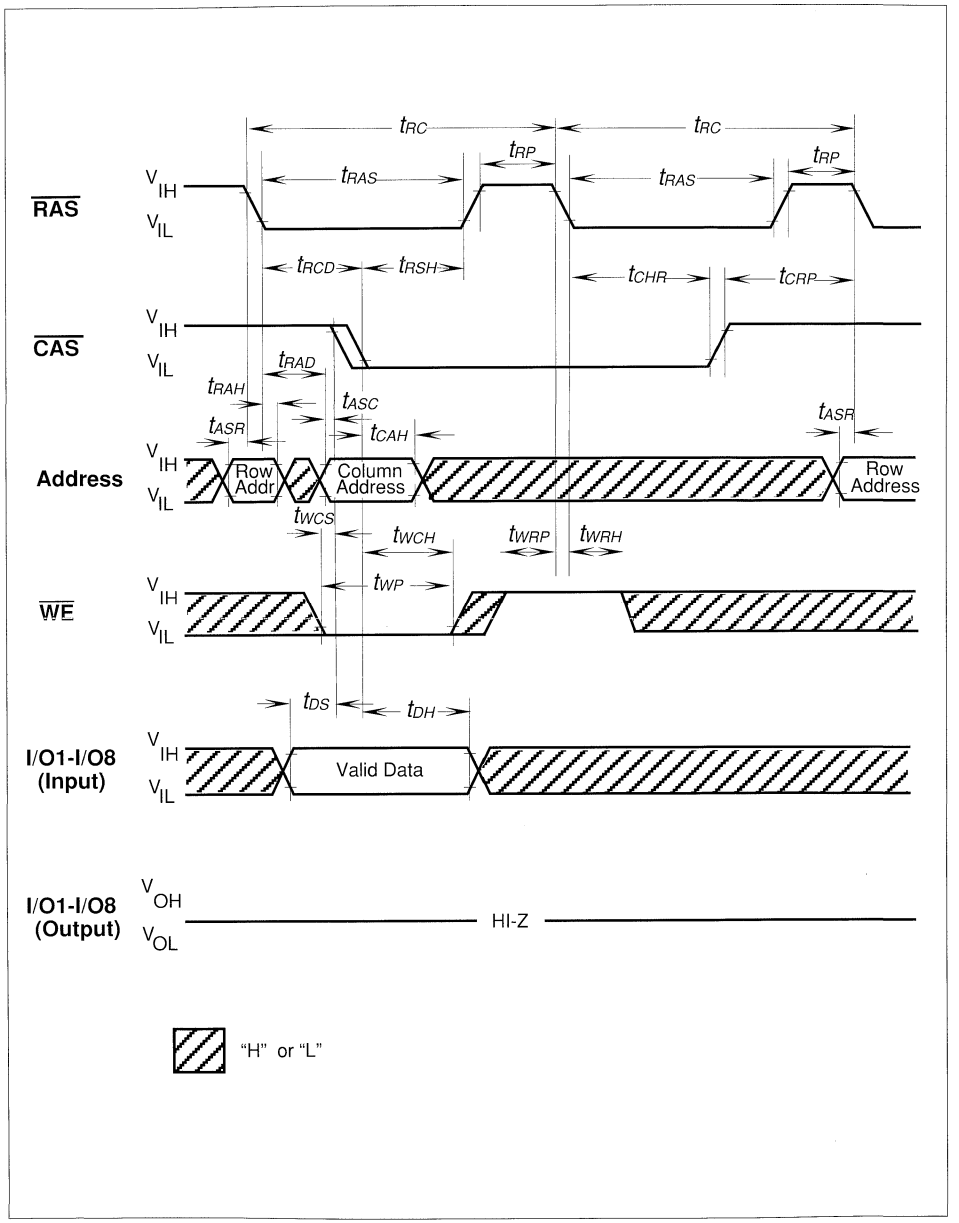
RAS-Only Refresh Cycle



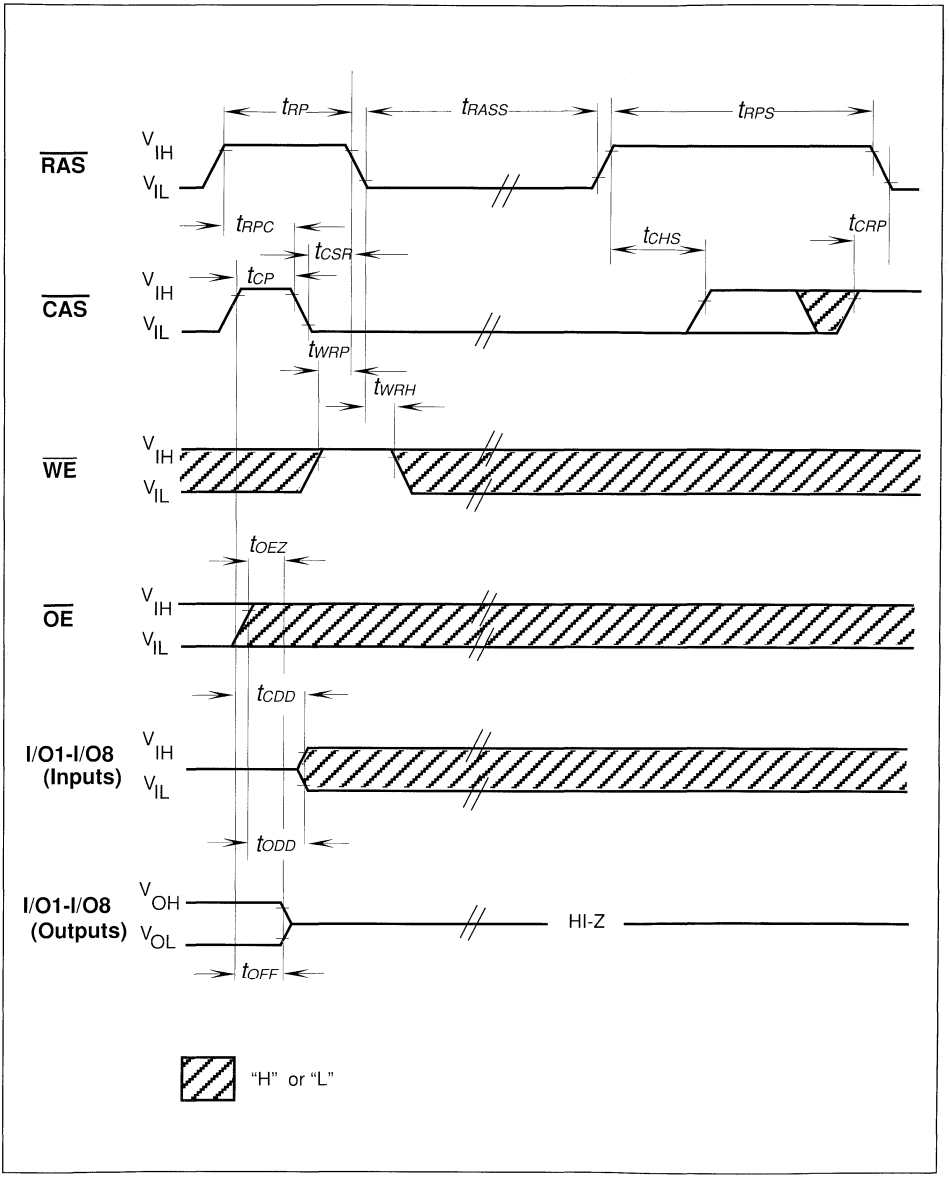
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



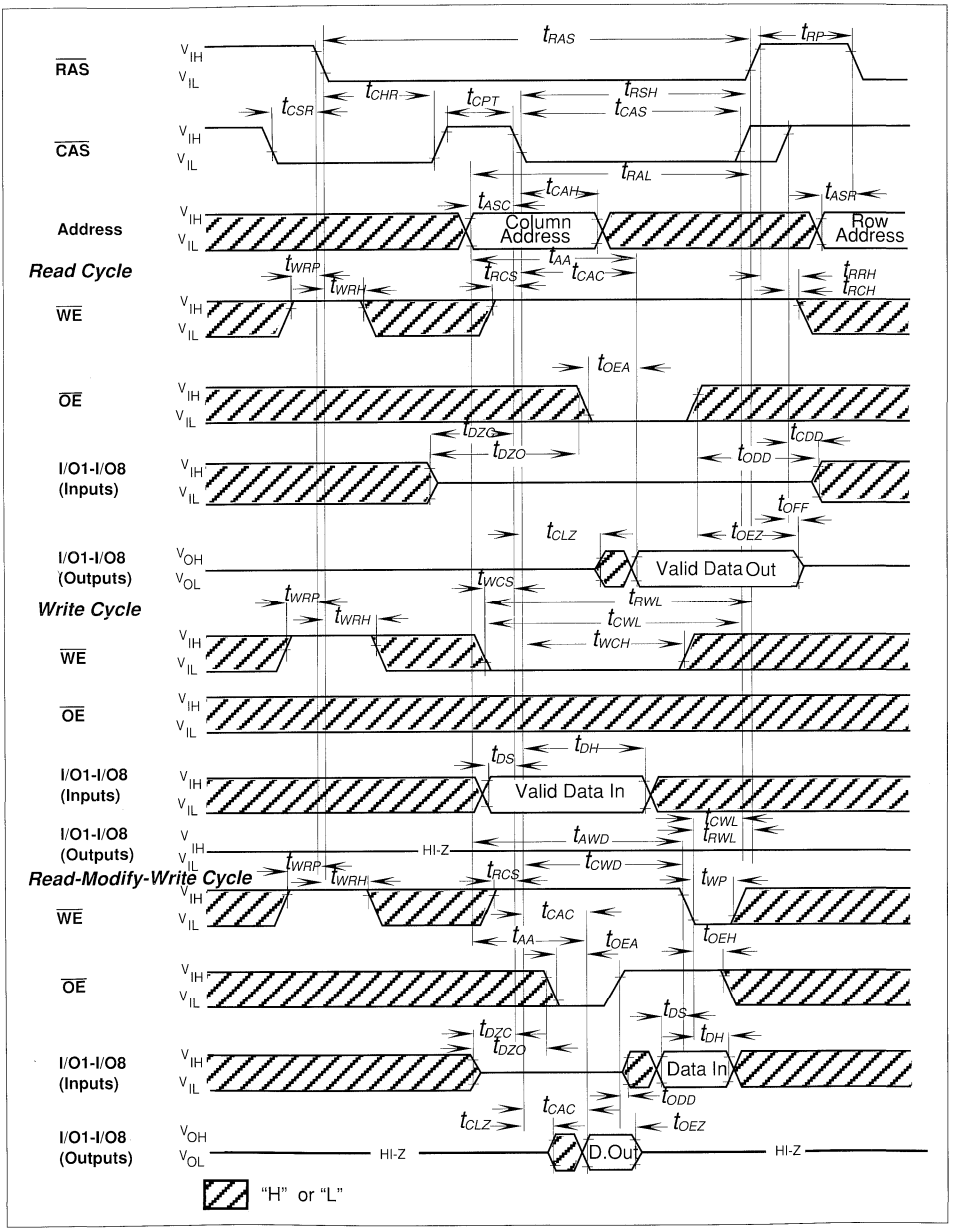
Hidden Refresh Cycle (Read)



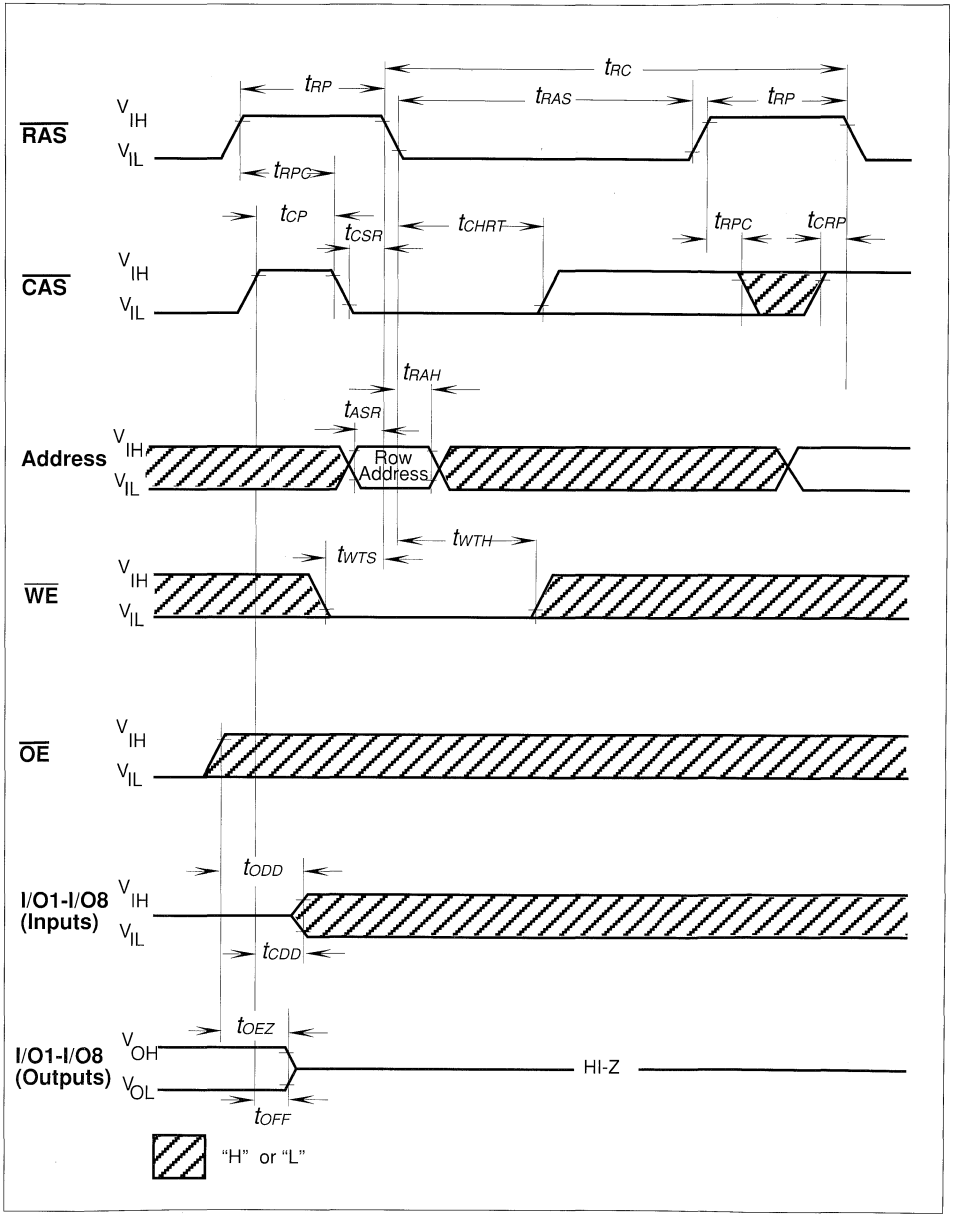
Hidden Refresh Cycle (Early Write)



CAS-before-RAS Self Refresh



CAS-Before-RAS Refresh Counter Test Cycle



Test Mode Entry

1M x 16-Bit Dynamic RAM (1k-Refresh)

HYB 5118160BSJ-50/-60/-70

Advanced Information

- 1 048 576 words by 16-bit organization
- 0 to 70 °C operating temperature
- Fast access and cycle time
  RAS access time:
  50 ns (-50 version)
  60 ns (-60 version)
  70 ns (-70 version)
  Cycle time:
  95 ns (-50 version)
  110 ns (-60 version)
  130 ns (-70 version)
  CAS access time:
  15 ns (-50, -60 version)
  20 ns (-70 version)
- Fast page mode cycle time
  35 ns (-50 version)
  40 ns (-60 version)
  45 ns (-70 version)
- Single + 5 V (± 10 %) supply
- Low power dissipation
  max. 990 active mW (-50 version)
  max. 935 active mW (-60 version)
  max. 880 active mW (-70 version)
  11 mW standby (TTL)
  5.5 mW standby (MOS)
- Output unlatched at cycle end allows two-dimensional chip selection
- Read, write, read-modify-write, CAS-before-RAS refresh, RAS-only refresh, hidden refresh, self refresh
- Fast page mode capability
- 2 CAS / 1 WE
- All inputs, outputs and clocks fully TTL-compatible
- 1024 refresh cycles / 16 ms
- Plastic Package: P-SOJ-42-1 400 mil

Ordering Information

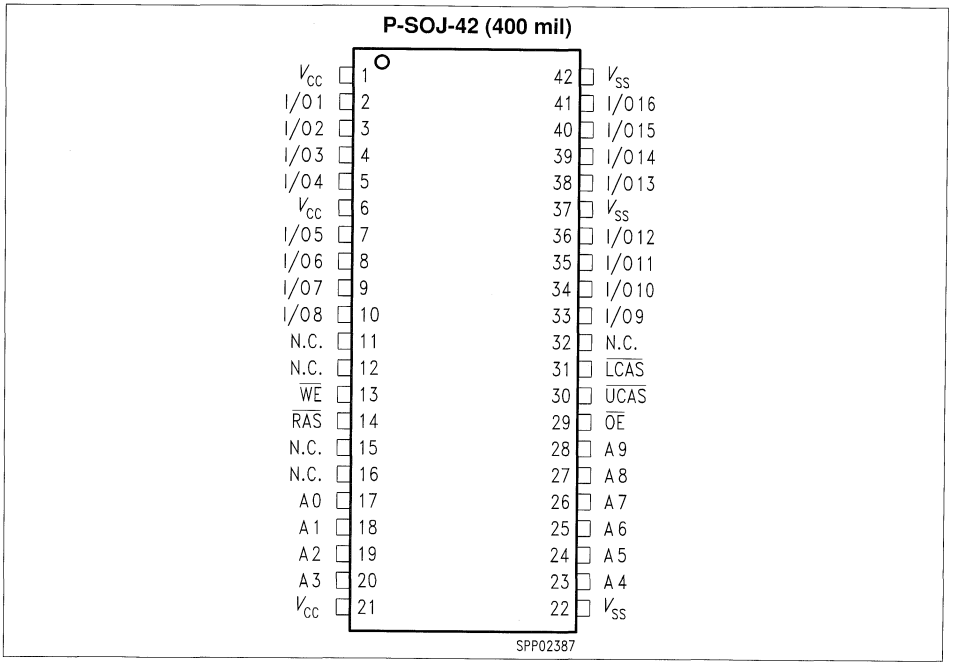
Type	Ordering Code	Package	Descriptions
HYB 5118160BSJ-50	Q67100-Q1072	P-SOJ-42-1 400 mil	DRAM (access time 50 ns)
HYB 5118160BSJ-60	Q67100-Q1073	P-SOJ-42-1 400 mil	DRAM (access time 60 ns)
HYB 5118160BSJ-70	Q67100-Q1074	P-SOJ-42-1 400 mil	DRAM (access time 70 ns)

The HYB 5118160BSJ is the new generation dynamic RAM organized as 1 048 576 words by 16 bits. The HYB 5118160BSJ utilizes a submicron CMOS silicon gate process technology, as well as advanced circuit techniques to provide wide operating margins, both internally and for the system user. Multiplexed address inputs permit the HYB 5118160BSJ to be packaged in a standard SOJ-42 400 mil plastic package. These packages provide high system bit densities and are compatible with commonly used automatic testing and insertion equipment. System-oriented features include single + 5 V (± 10 %) power supply, direct interfacing with high-performance logic device families such as Schottky TTL.

Pin Definitions and Functions

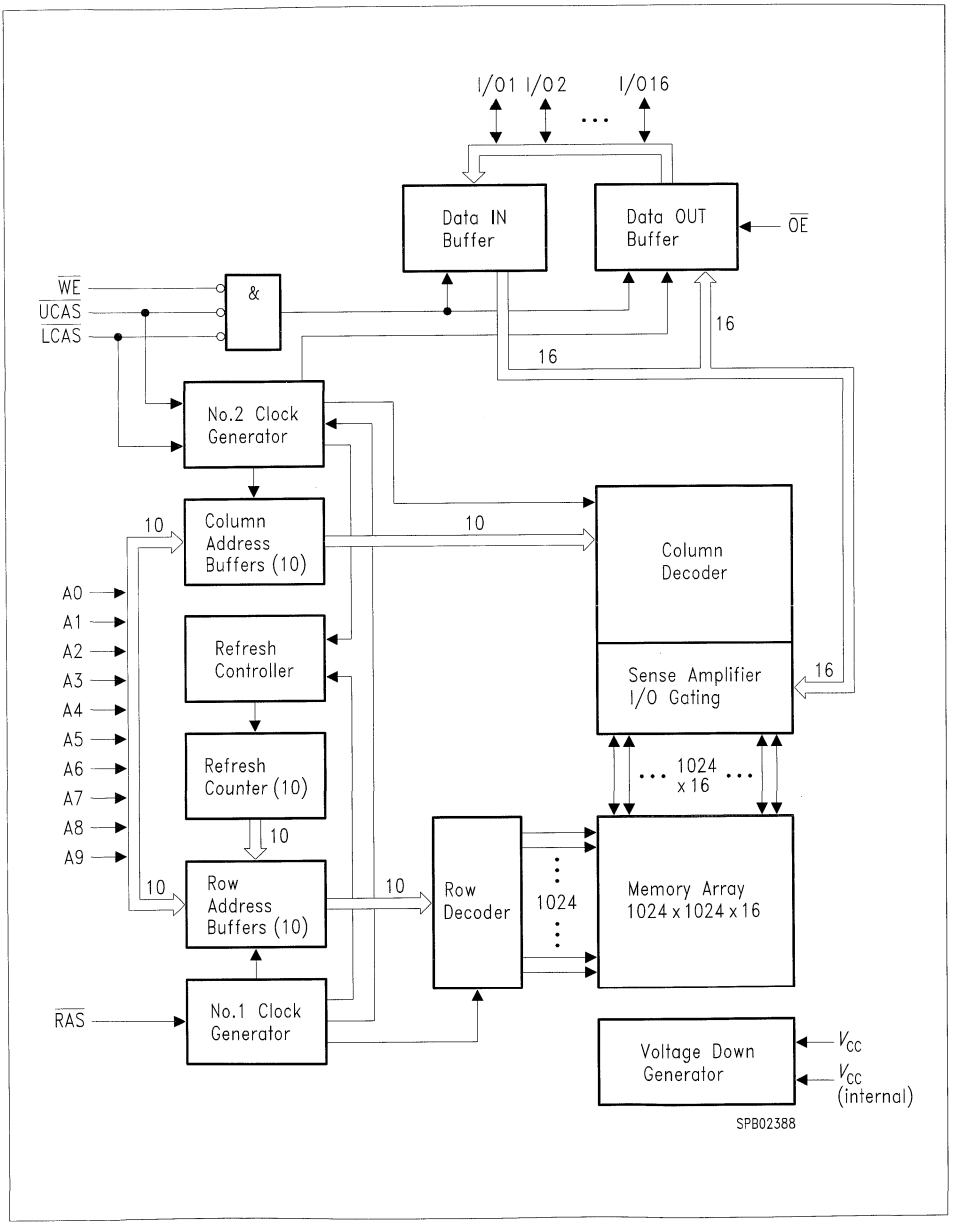
Pin No.	Function
A0 to A9	Row Address Inputs
A0 to A9	Column Addess Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{OE}$	Output Enable
I/O1-I/O16	Data Input/Output
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground (0 V)
N.C.	not connected

Pin Configuration
(top view)



Truth Table

RAS	LCAS	UCAS	WE	OE	I/O1-I/O8	I/O9-I/O16	Operation
H	H	H	H	H	High-Z	High-Z	Standby
L	H	H	H	H	High-Z	High-Z	Refresh
L	L	H	H	L	Dout	High-Z	Lower byte read
L	H	L	H	L	High-Z	Dout	Upper byte read
L	L	L	H	L	Dout	Dout	Word read
L	L	H	L	H	Din	Don't care	Lower byte write
L	H	L	L	H	Don't care	Din	Upper byte write
L	L	L	L	H	Din	Din	Word write
L	L	L	H	H	High-Z	High-Z	NOP



Block Diagram

Absolute Maximum Ratings

Operating temperature range ..... 0 to 70 °C
Storage temperature range ..... – 55 to 150 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 0.5 to min (V_{CC} + 0.5, 7.0) V
Power supply voltage ..... – 1.0 V to 7.0 V
Power dissipation ..... 1.0 W
Data out current (short circuit) ..... 50 mA

Note:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	V_{CC} + 0.5	V	1)
Input low voltage	V_{IL}	– 0.5	0.8	V	1)
Output high voltage (I_{OUT} = – 5 mA)	V_{OH}	2.4	–	V	1)
Output low voltage (I_{OUT} = 4.2 mA)	V_{OL}	–	0.4	V	1)
Input leakage current, any input (0 V ≤ V_{IH} ≤ V_{CC} + 0.3 V, all other pins = 0 V)	$I_{I(L)}$	– 10	10	µA	1)
Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ V_{CC} + 0.3 V)	$I_{O(L)}$	– 10	10	µA	1)
Average V_{CC} supply current:	I_{CC1}				
-50 ns version		–	200	mA	2) 3) 4)
-60 ns version		–	180	mA	2) 3) 4)
-70 ns version		–	160	mA	2) 3) 4)
($\overline{RAS}$, $\overline{CAS}$, address cycling, t_{RC} = t_{RC} min.)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	2	mA	–
Average V_{CC} supply current, during $\overline{RAS}$-only refresh cycles:	I_{CC3}				
-50 ns version		–	200	mA	2) 4)
-60 ns version		–	180	mA	2) 4)
-70 ns version		–	160	mA	2) 4)
($\overline{RAS}$ cycling: $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)					

DC Characteristics (cont'd)

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current, during fast page mode: -50 ns version -60 ns version -70 ns version ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling, t_{PC} = t_{PC} min.)	I_{CC4}	– – –	90 80 70	mA mA mA	2) 3) 4) 2) 3) 4) 2) 3) 4)
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	–	1	mA	1)
Average V_{CC} supply current, during $\overline{CAS}$-before-RAS refresh mode: -50 ns version -60 ns version -70 ns version ($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min.)	I_{CC6}	– – –	200 180 160	mA mA mA	2) 4) 2) 4) 2) 4)
Average Self Refresh Current ($\overline{CBR}$ cycle with t_{RAS} > t_{RASS} min., $\overline{CAS}$ held low, $\overline{WE}$ = V_{CC} – 0.2 V, Address and Din = V_{CC} – 0.2 V or 0.2 V)	I_{CC7}	–	1	mA	

AC Characteristics 5)

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		HYB 5118160 BSJ -50		HYB 5118160 BSJ -60		HYB 5118160 BSJ -70		
		min.	max.	min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	95	–	110	–	130	–	ns
Read-write cycle time	t_{RWC}	135	–	150	–	180	–	ns
Fast page mode cycle time	t_{PC}	35	–	40	–	45	–	ns

AC Characteristics (cont'd) [5]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		HYB 5118160 BSJ -50		HYB 5118160 BSJ -60		HYB 5118160 BSJ -70		
		min.	max.	min.	max.	min.	max.	
Fast page mode read-write cycle time	t_{PRWC}	75	–	80	–	95	–	ns
Access time from $\overline{RAS}$ [7) 12)]	t_{RAC}	–	50	–	60	–	70	ns
Access time from $\overline{CAS}$ [7) 12)]	t_{CAC}	–	15	–	15	–	20	ns
Access time from column address [7) 13)]	t_{AA}	–	25	–	30	–	35	ns
Access time from $\overline{CAS}$ precharge [7)]	t_{CPA}	–	30	–	35	–	40	ns
$\overline{CAS}$ to output in low-Z [7)]	t_{CLZ}	0	–	0	–	0	–	ns
Output buffer turn-off delay [8)]	t_{OFF}	0	15	0	15	0	20	ns
Transition time (rise and fall) [6)]	t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	35	–	40	–	50	–	ns
$\overline{RAS}$ pulse width	t_{RAS}	50	10k	60	10k	70	10k	ns
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	50	200k	60	200k	70	200k	ns
$\overline{CAS}$ precharge to $\overline{RAS}$ Delay	t_{RHCP}	30	–	35	–	40	–	ns
$\overline{CAS}$ precharge to $\overline{WE}$ (FPMR RMW)	t_{CPWD}	50	–	55	–	65	–	ns
$\overline{RAS}$ hold time	t_{RSH}	15		15	–	20	–	ns
$\overline{CAS}$ hold time	t_{CSH}	50		60	–	70	–	ns
$\overline{CAS}$ pulse width	t_{CAS}	15	10k	15	10k	20	10k	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time [12)]	t_{RCD}	20	35	20	45	20	50	
$\overline{RAS}$ to column address delay time [13)]	t_{RAD}	15	25	15	30	15	35	ns

AC Characteristics (cont'd) [5]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		HYB 5118160 BSJ -50		HYB 5118160 BSJ -60		HYB 5118160 BSJ -70		
		min.	max.	min.	max.	min.	max.	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	5	–	ns
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns
Row address hold time	t_{RAH}	10	–	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns
Column address hold time	t_{CAH}	10	–	15	–	15	–	ns
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	–	30	–	35	–	ns
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns
Read command hold time [9]	t_{RCH}	0	–	0	–	0	–	ns
Read command hold time referenced to $\overline{RAS}$ [9]	t_{RRH}	0	–	0	–	0	–	ns
Write command hold time	t_{WCH}	10	–	15	–	15	–	ns
Write command pulse width	t_{WP}	10	–	15	–	15	–	ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	–	15	–	20	–	ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	–	15	–	20	–	ns
Data setup time [10]	t_{DS}	0	–	0	–	0	–	ns
Data hold time [10]	t_{DH}	10	–	15	–	15	–	ns
Refresh period	t_{REF}	–	16	–	16	–	16	ms
Write command setup time [11]	t_{WCS}	0	–	0	–	0	–	ns

AC Characteristics (cont'd) [5]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		HYB 5118160 BSJ -50		HYB 5118160 BSJ -60		HYB 5118160 BSJ -70		
		min.	max.	min.	max.	min.	max.	
$\overline{CAS}$ to $\overline{WE}$ delay time [11]	t_{CWD}	35	–	35	–	45	–	ns
$\overline{RAS}$ to $\overline{WE}$ delay time [11]	t_{RWD}	70	–	80	–	95	–	ns
Column address to $\overline{WE}$ delay time [11]	t_{AWD}	45	–	50	–	60	–	ns
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CSR}	10	–	10	–	10	–	ns
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CHR}	10	–	10	–	10	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5	–	5	–	5	–	ns
$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ counter test cycle)	t_{CPT}	35	–	40	–	40	–	ns
Write to $\overline{RAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{WRP}	10	–	10	–	10	–	ns
Write hold time referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{WRH}	10	–	10	–	10	–	ns
$\overline{OE}$ command hold time	t_{OEH}	15	–	15	–	20	–	ns
$\overline{OE}$ access time	t_{OEA}	–	15	–	15	–	20	ns
Output buffer turn-off delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	ns
Data to $\overline{CAS}$ low delay [15]	t_{DZC}	0	–	0	–	0	–	ns
Data to $\overline{OE}$ low delay [15]	t_{DZO}	0	–	0	–	0	–	ns
$\overline{CAS}$ high to data delay [16]	t_{CDD}	15	–	15	–	20	–	ns

AC Characteristics (cont'd) [5]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		HYB 5118160 BSJ -50		HYB 5118160 BSJ -60		HYB 5118160 BSJ -70		
		min.	max.	min.	max.	min.	max.	
$\overline{OE}$ high to data delay [16]	t_{ODD}	15	–	15	–	20	–	ns
$\overline{RAS}$ pulse width during self refresh	t_{RASS}	100k	–	100k	–	100k	–	ns
$\overline{RAS}$ precharge time during self refresh	t_{RPS}	95	–	110	–	130	–	ns
$\overline{CAS}$ hold time during self refresh	t_{CHS}	– 50	–	– 50	–	– 50	–	ns

Capacitance

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A9)	C_{I1}	–	5	pF
Input capacitance ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}	–	7	pF
I/O capacitance (I/O1-I/O16)	C_{IO}	–	7	pF

Notes:

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.

4) Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4} it can be changed once or less during a fast page mode cycle (t_{PC}).

5) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6) $V_{IH\ (min.)}$ and $V_{IL\ (max.)}$ are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.

7) Measured with a load equivalent to 2 TTL loads and 100 pF.

8) $t_{OFF\ (max.)}$ and $t_{OEZ\ (max.)}$ define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.

9) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

10) These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.

11) t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS\ (min.)}$, the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} > t_{RWD\ (min.)}$, $t_{CWD} > t_{CWD\ (min.)}$, $t_{AWD} > t_{AWD\ (min.)}$ and $t_{CPWD} > t_{CPWD\ (min.)}$, the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.

12) Operation within the $t_{RCD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RCD\ (max.)}$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD\ (max.)}$ limit, then access time is controlled by t_{CAC}.

13) Operation within the $t_{RAD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RAD\ (max.)}$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD\ (max.)}$ limit, then access time is controlled by t_{AA}.

14) AC measurements assume t_T = 5 ns.

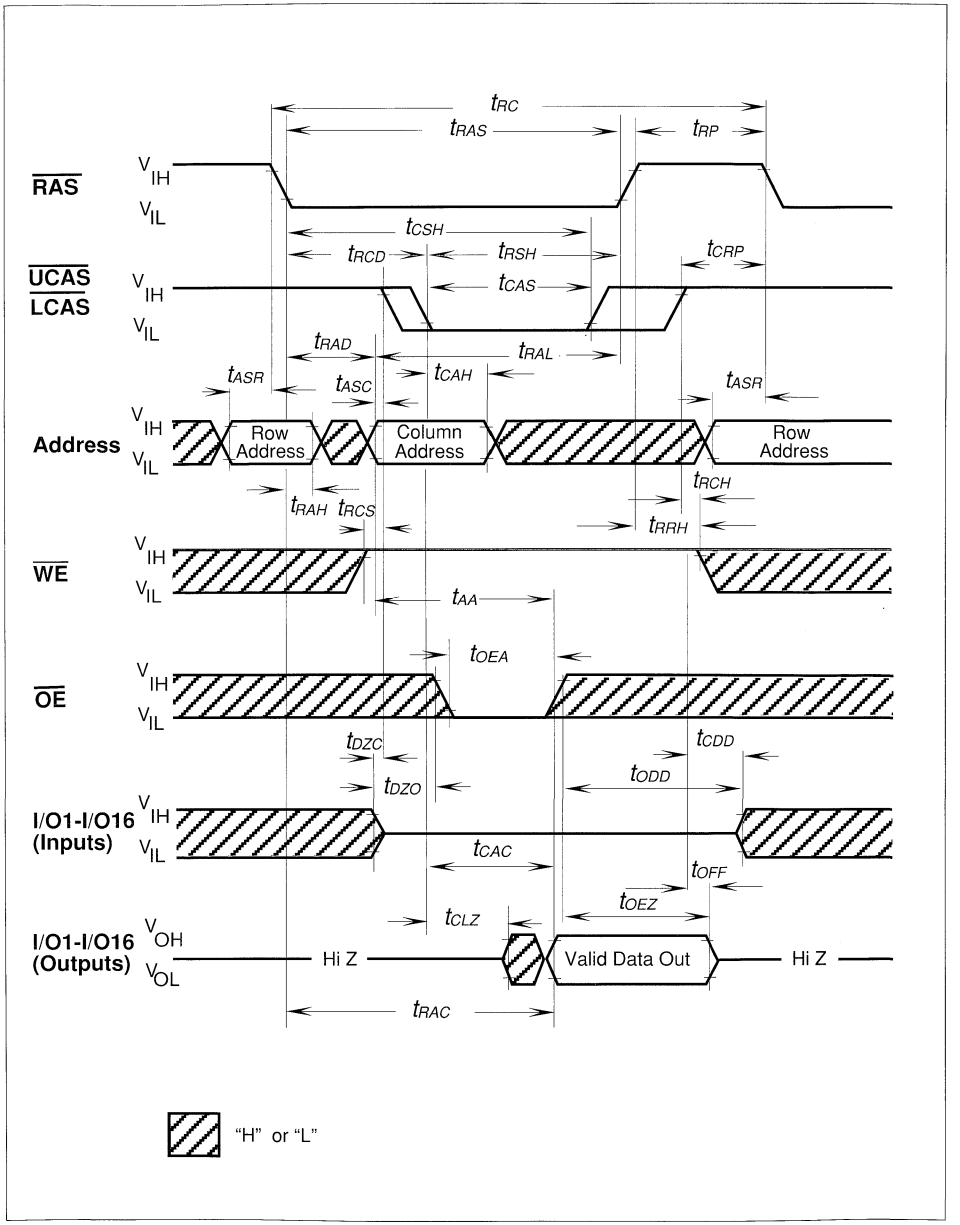
15) Either t_{DZC} or t_{DZO} must be satisfied.

16) Either t_{CDD} or t_{ODD} must be satisfied.

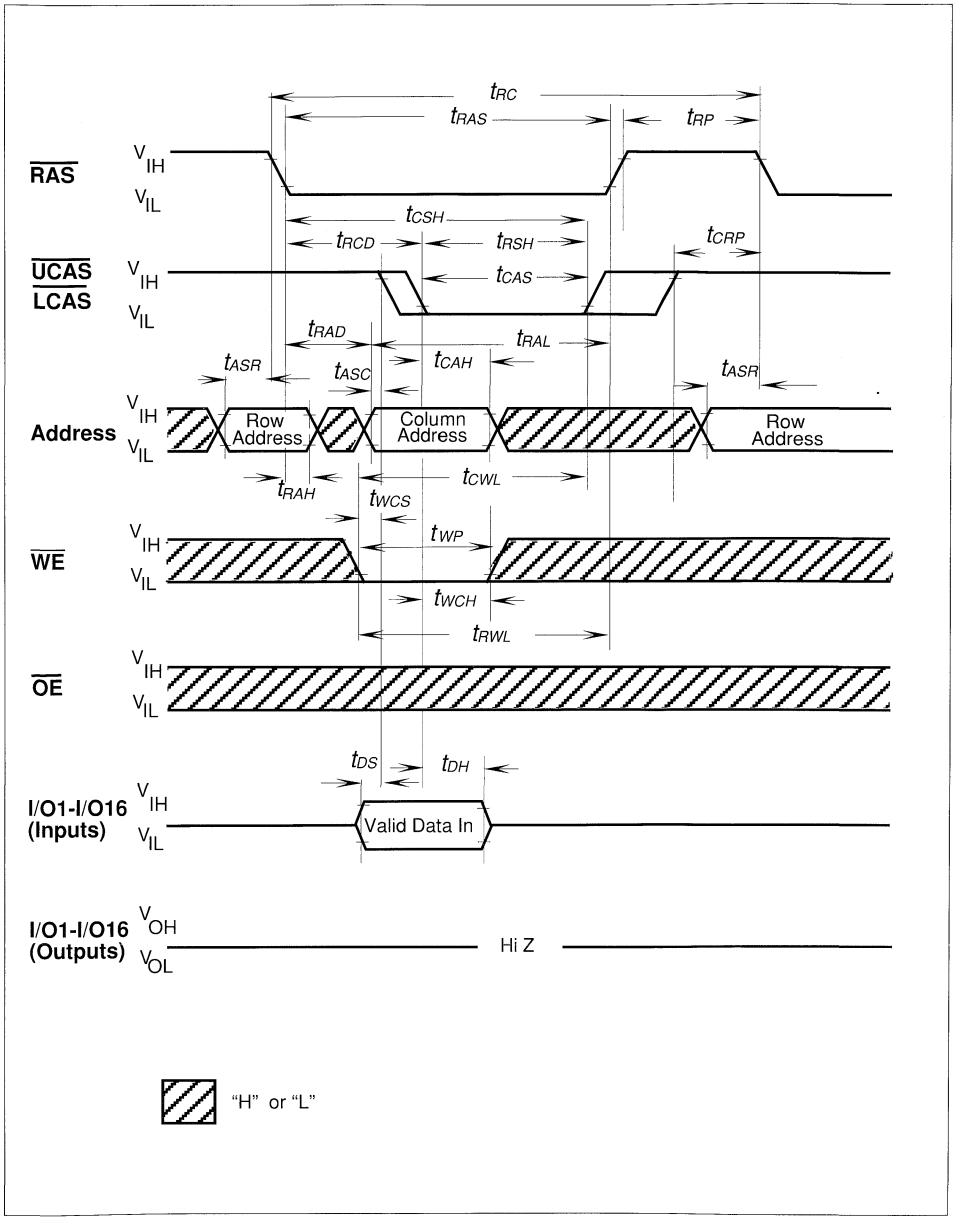
17) When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:

If row addresses are being refreshed on an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh.

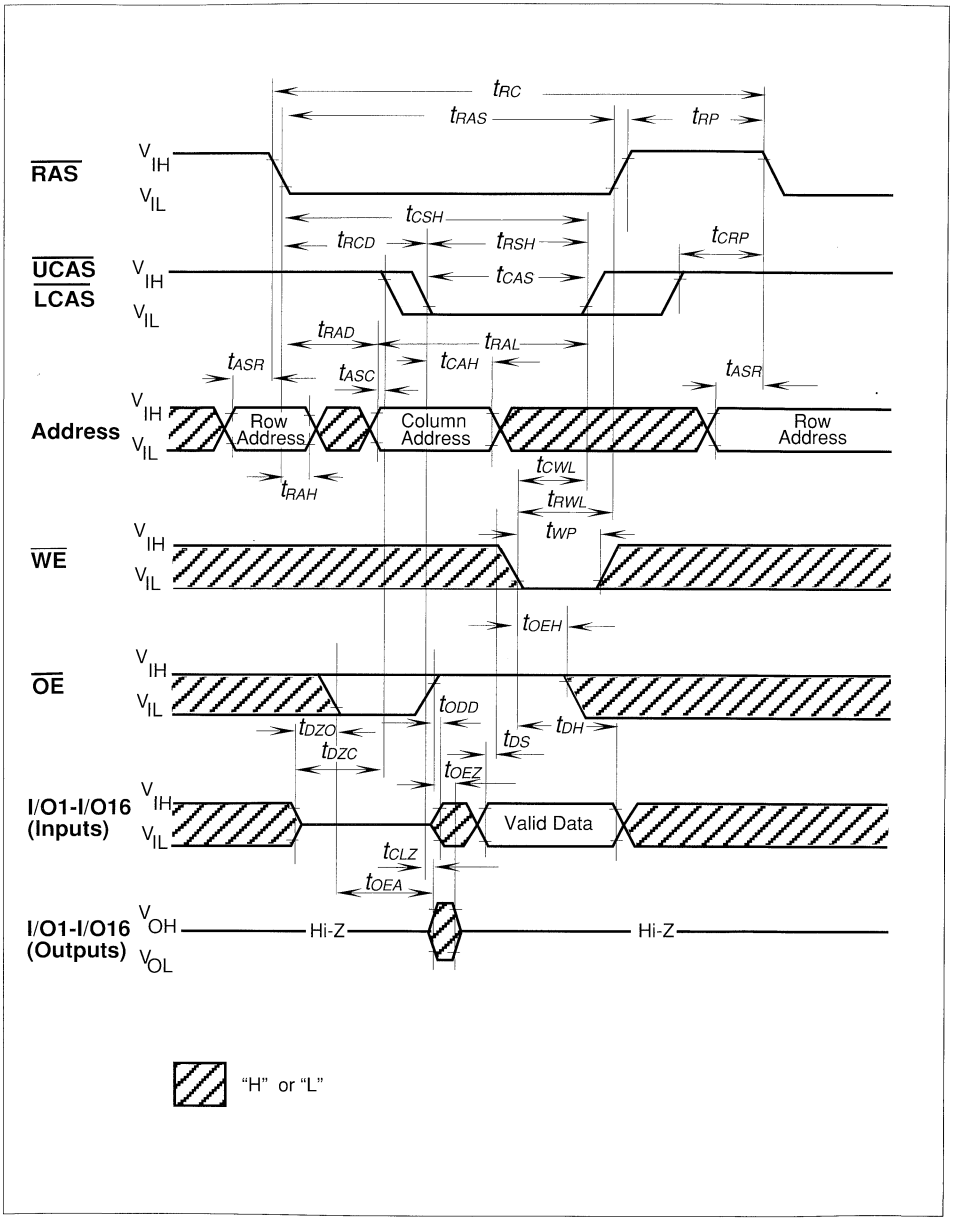
If row addresses are being refreshed in any other manner (ROR - Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh.


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
UCAS
LCAS
tCAS
tRAD
tRAL
tASR
tASC
tCAH
tASR
Address
Row Address
Column Address
Row Address
tRCH
tRAH
tRCS
tRRH
WE
tAA
tOEA
OE
tDZC
tCDD
tDZO
tODD
I/O1-I/O16 (Inputs)
tCAC
tOFF
tOEZ
tCLZ
I/O1-I/O16 (Outputs)
VOH
VOL
Hi Z
Valid Data Out
Hi Z
tRAC
"H" or "L"

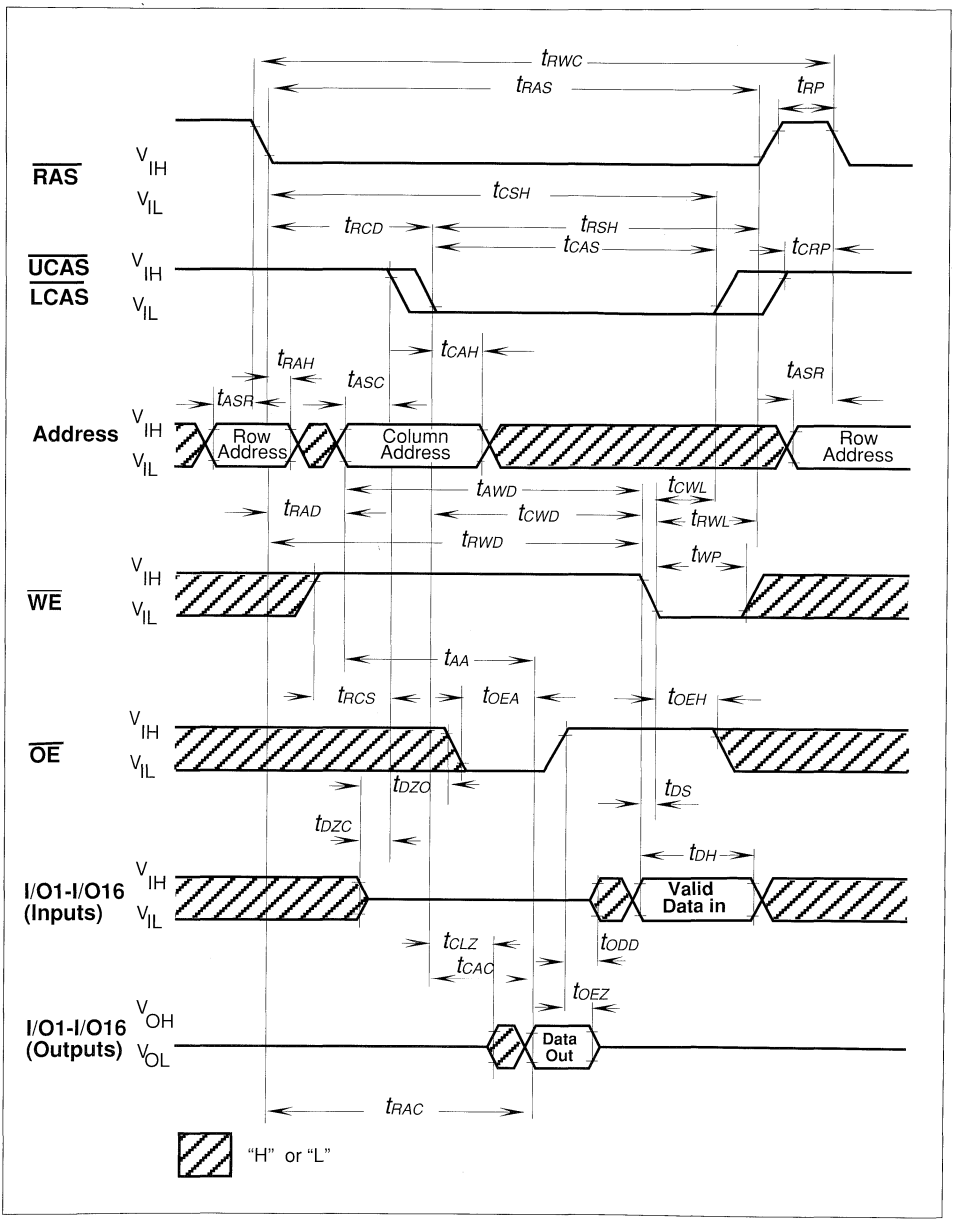
Read Cycle



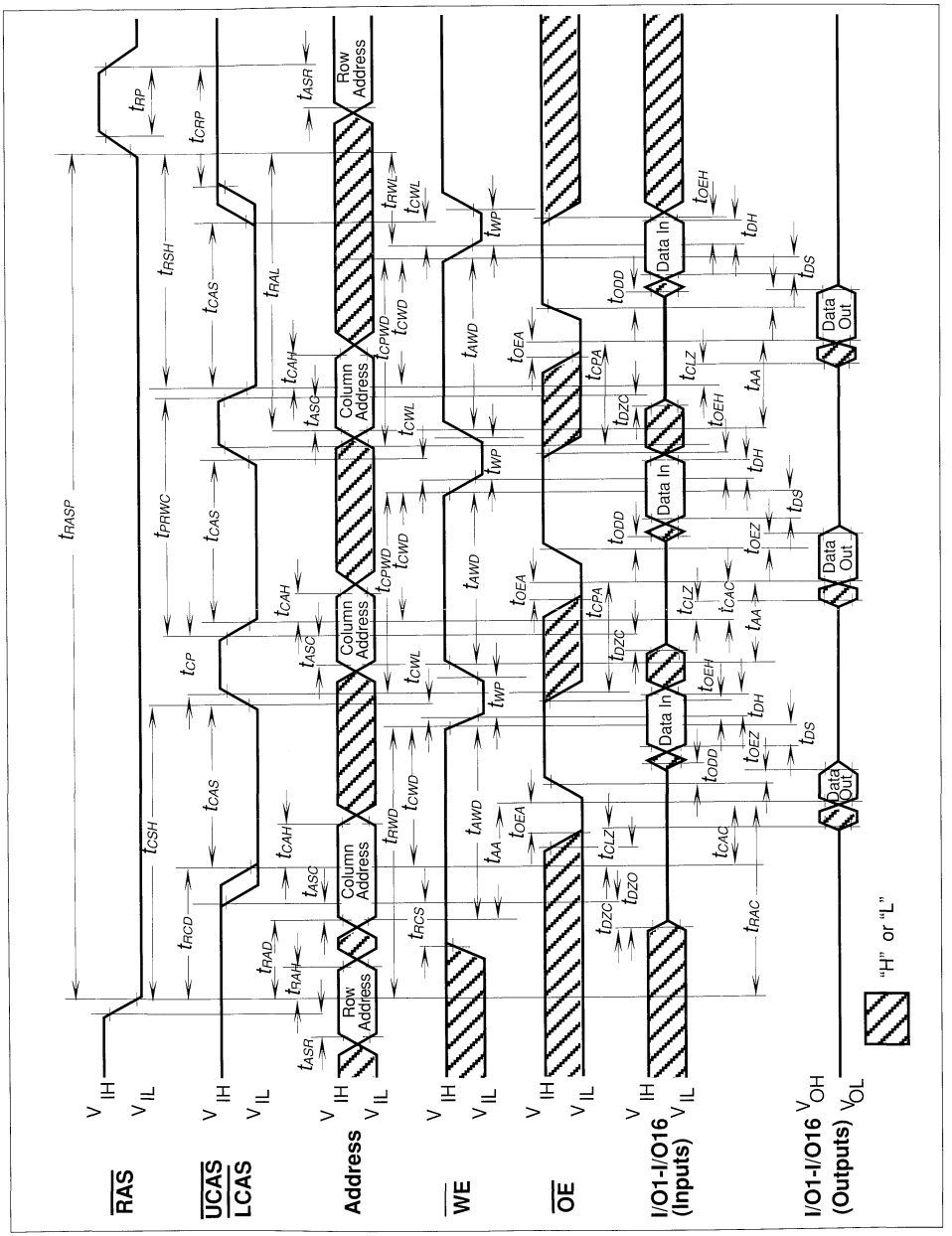
Write Cycle (Early Write)



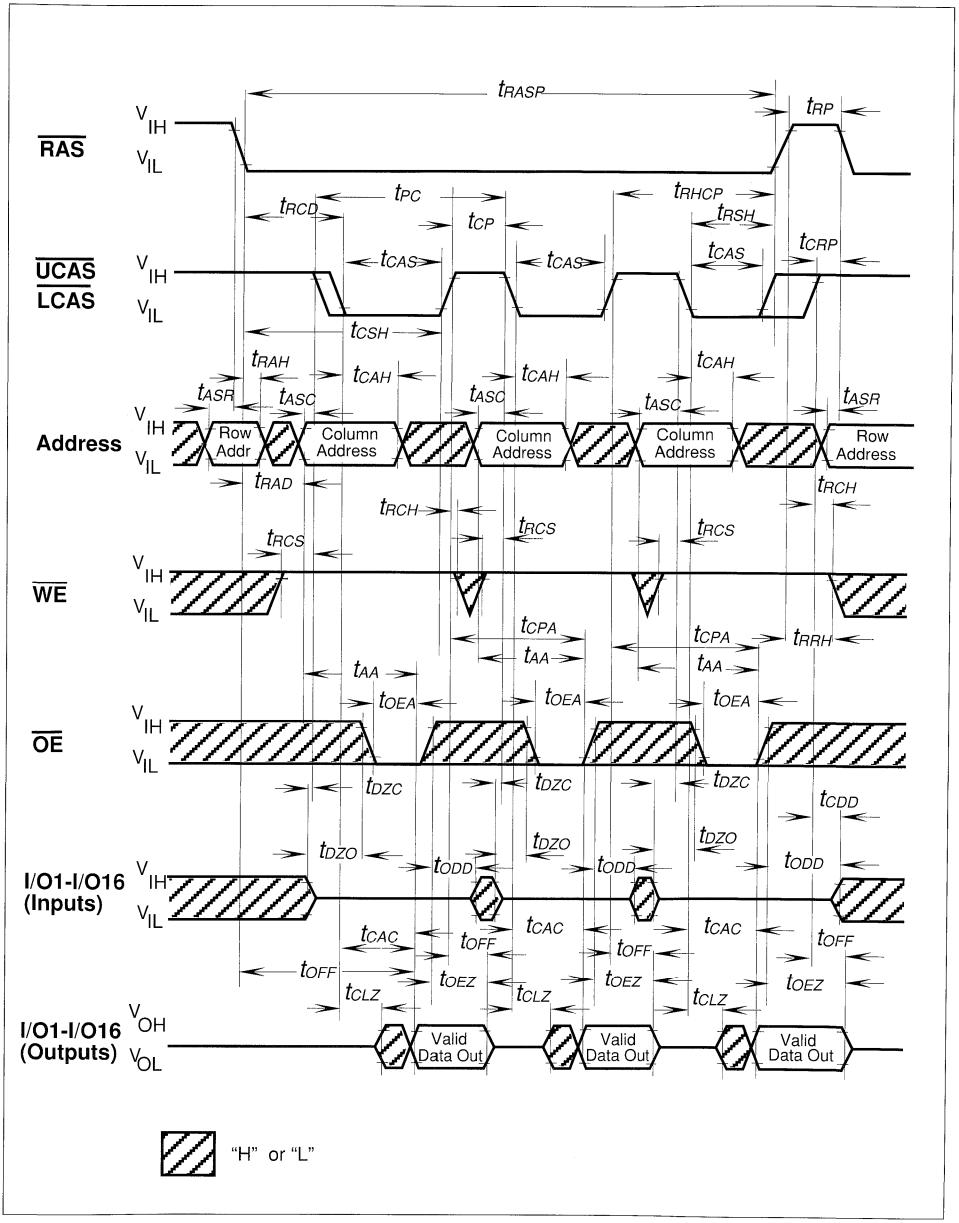
Write Cycle ($\overline{OE}$ Controlled Write)



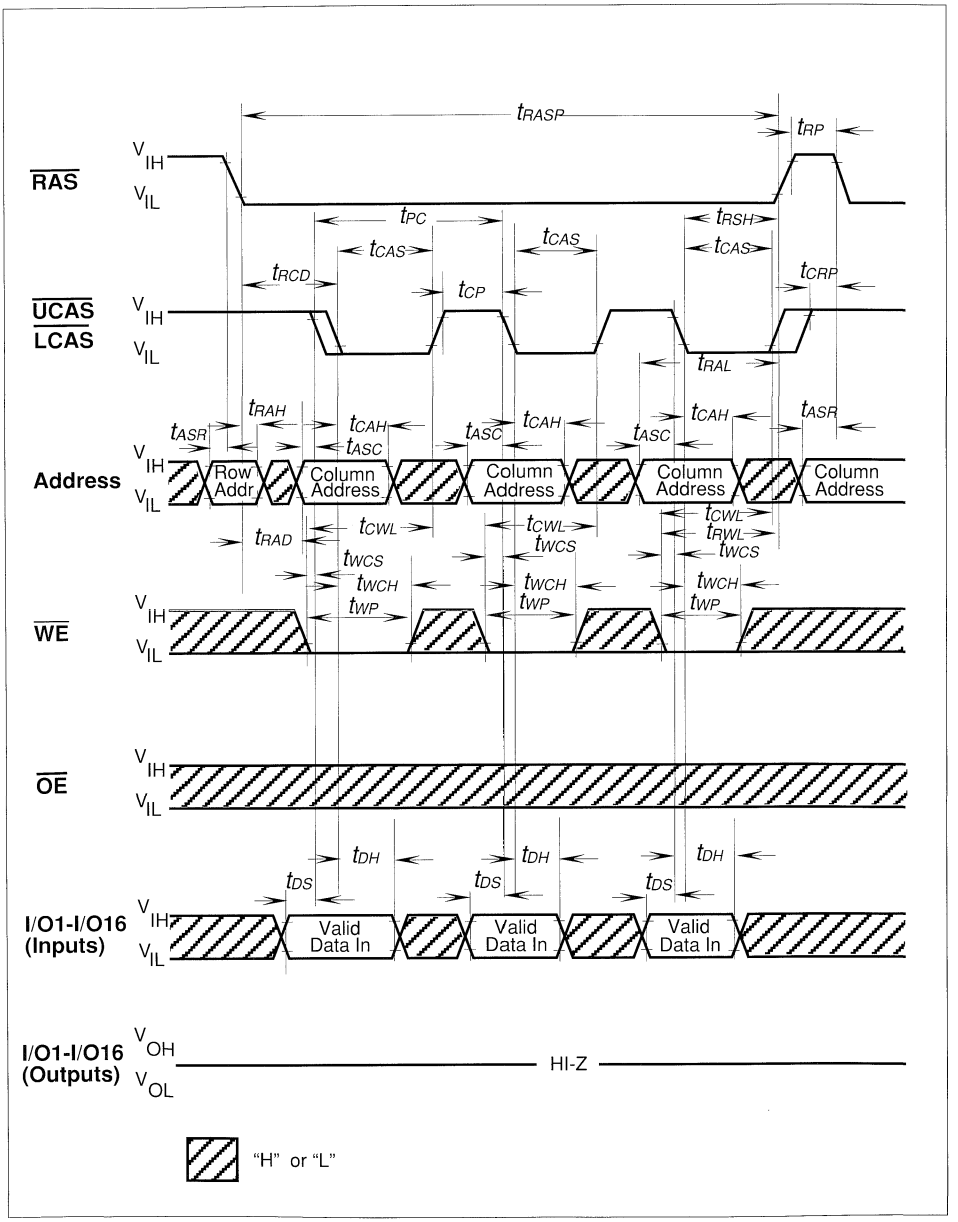
Read-Write (Read-Modify-Write) Cycle



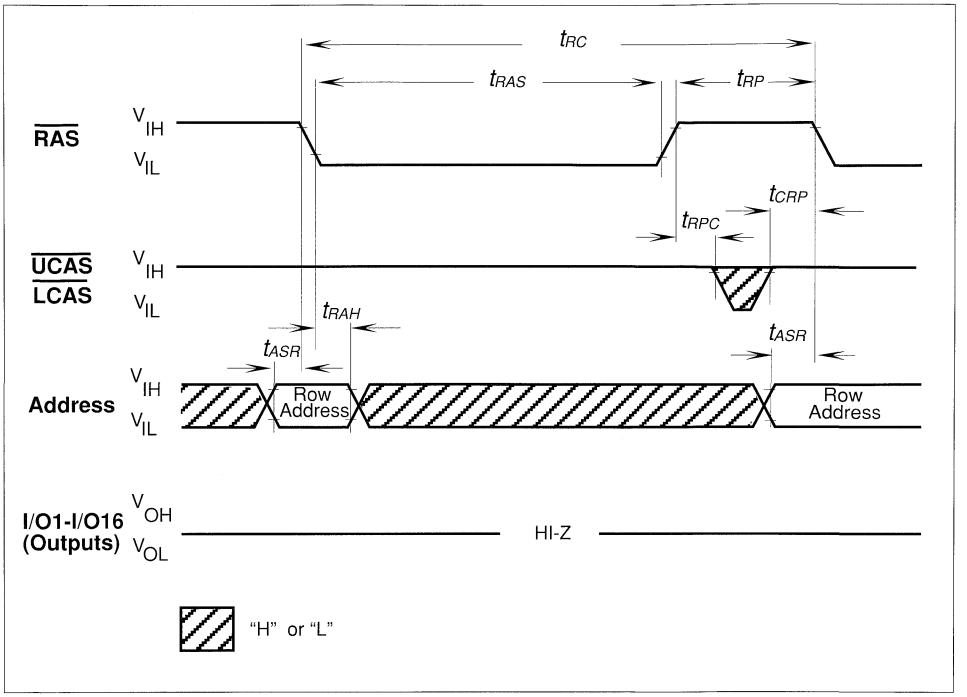
Fast Page Mode Read-Modify-Write Cycle



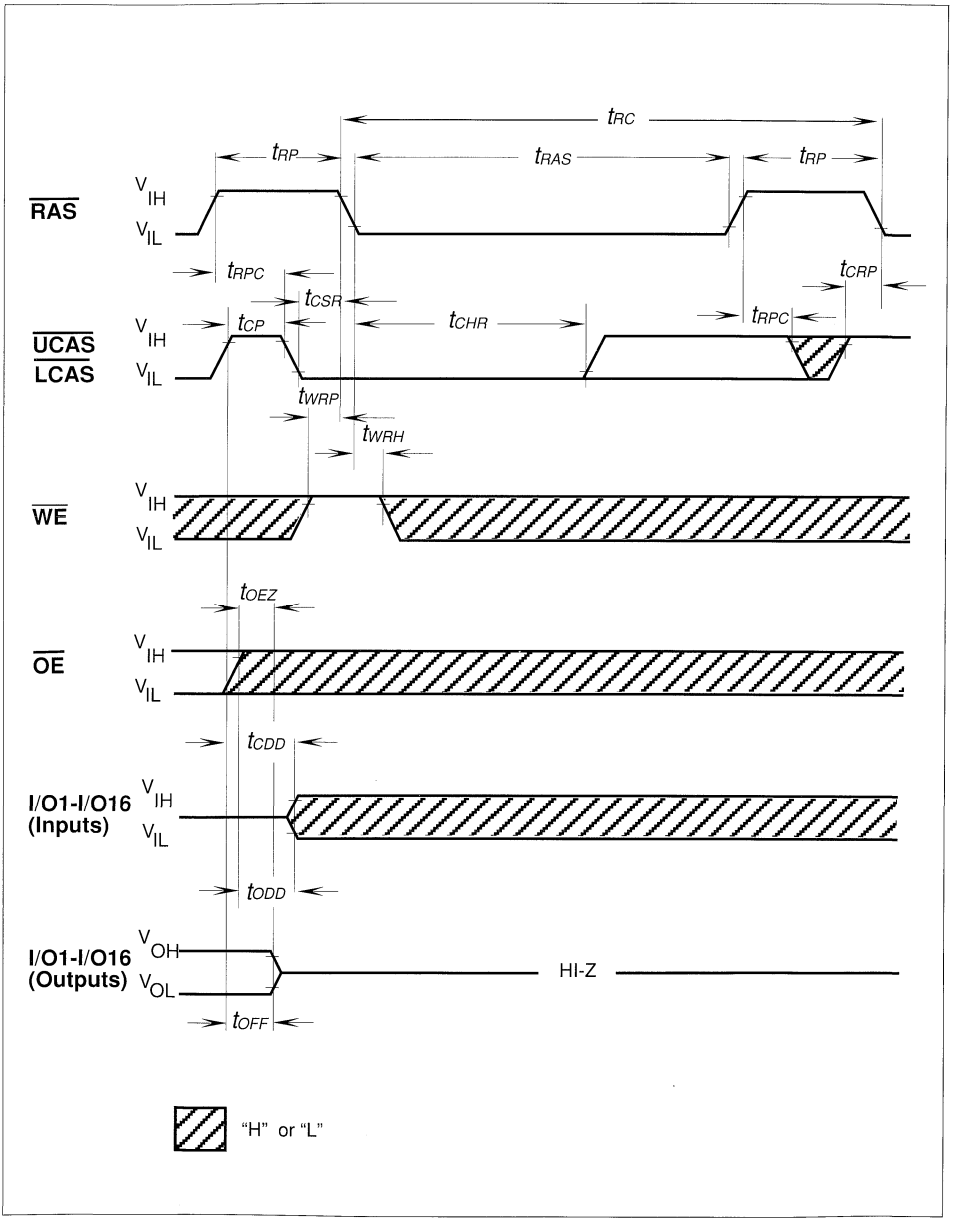
Fast Page Mode Read Cycle



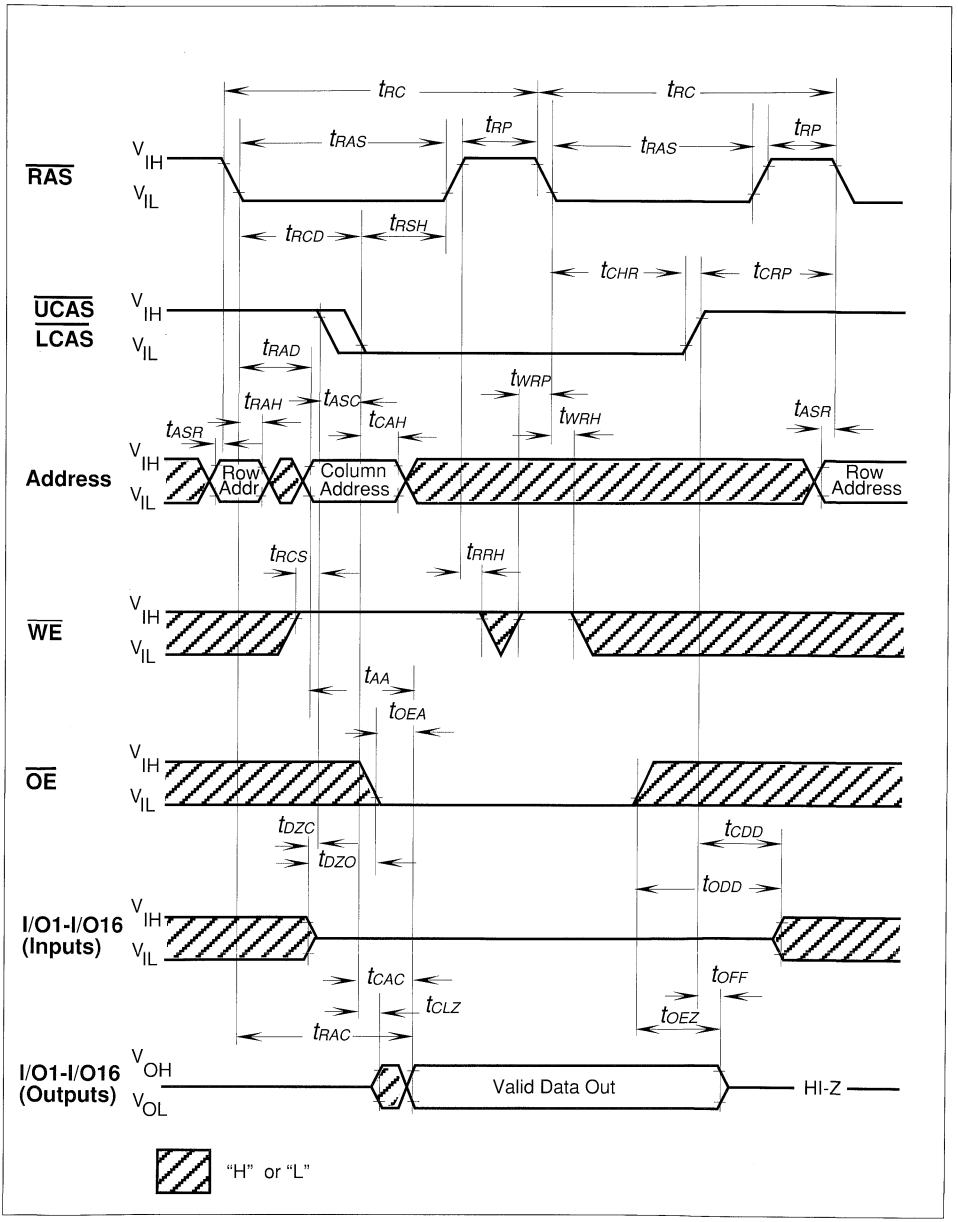
Fast Page Mode Early Write Cycle



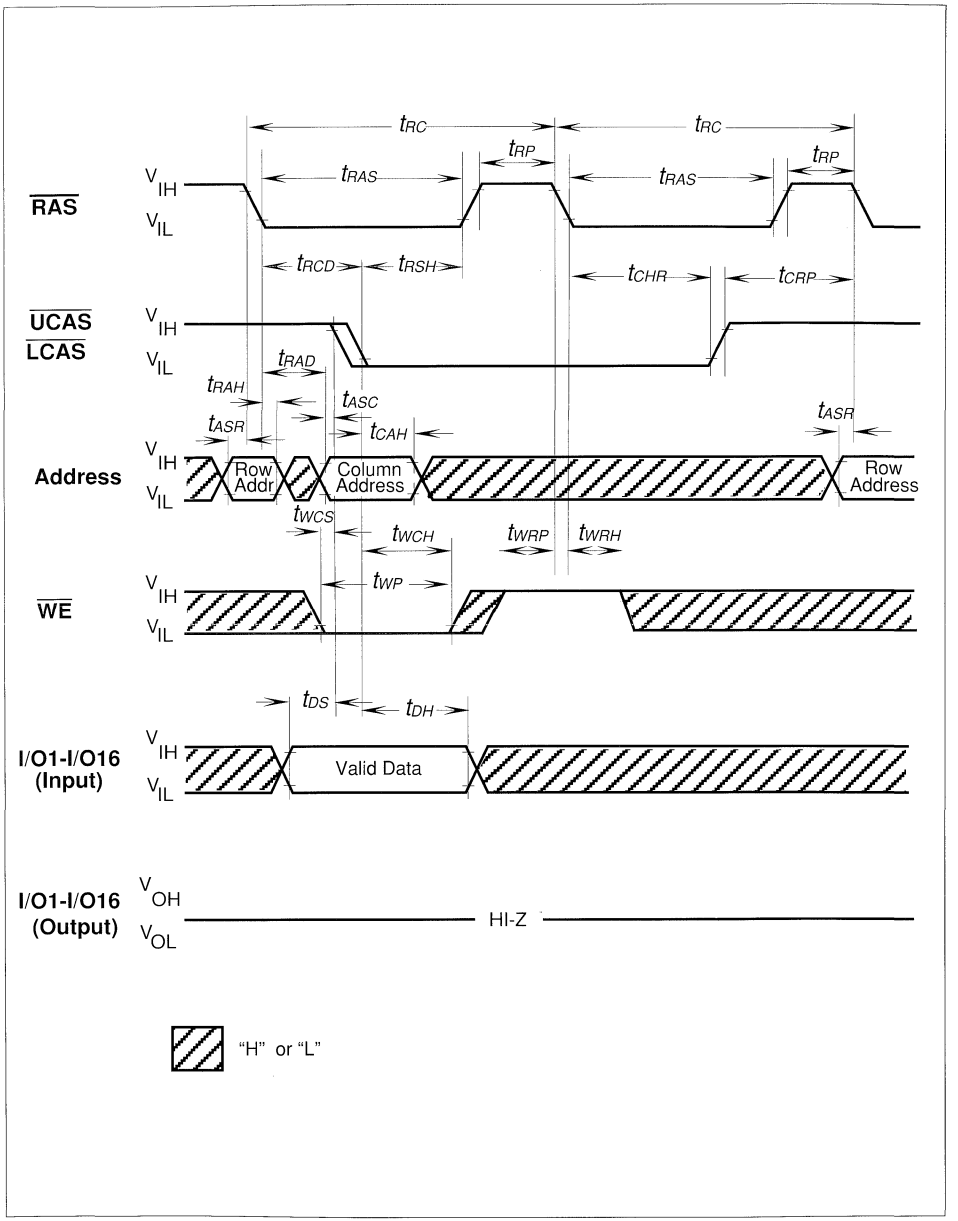
RAS-Only Refresh Cycle



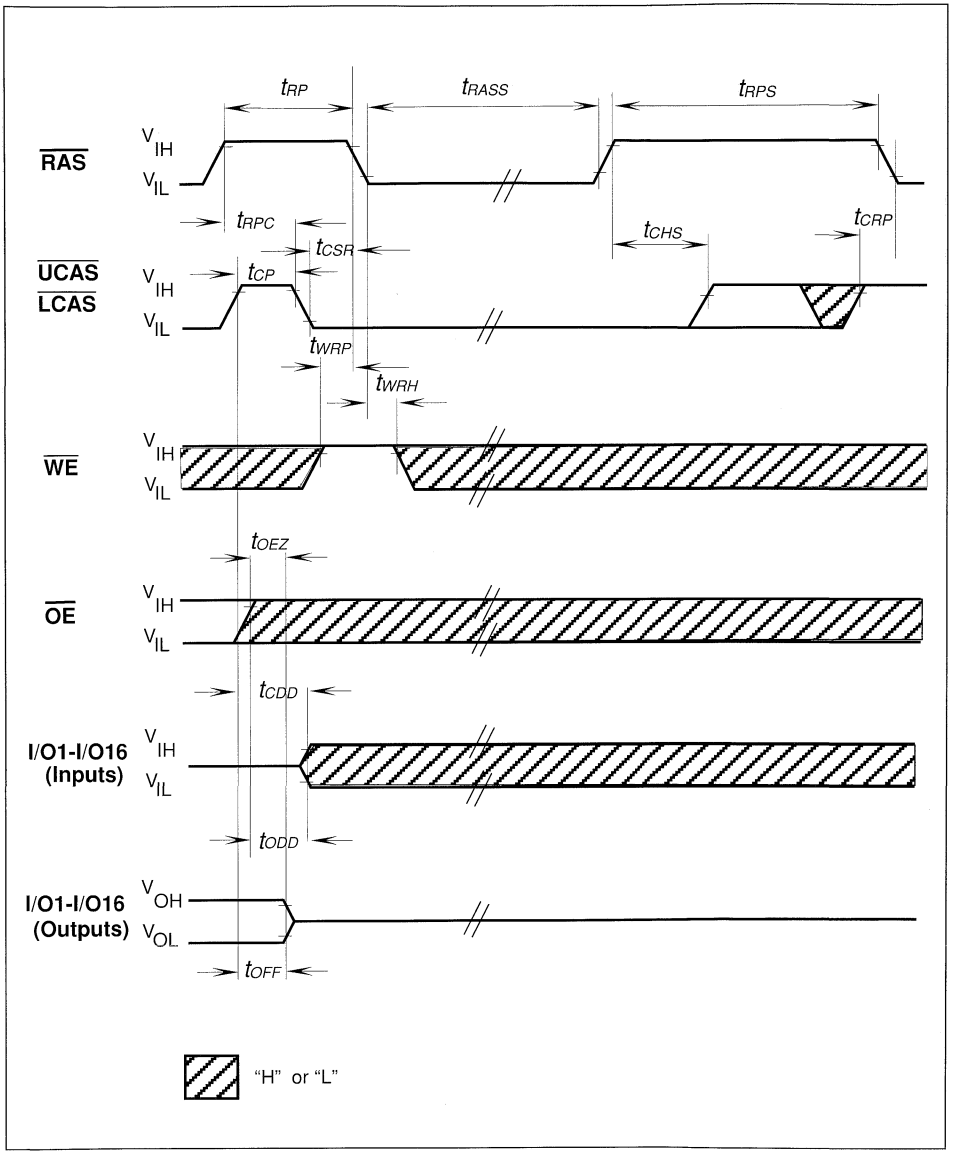
CAS-Before-RAS Refresh Cycle



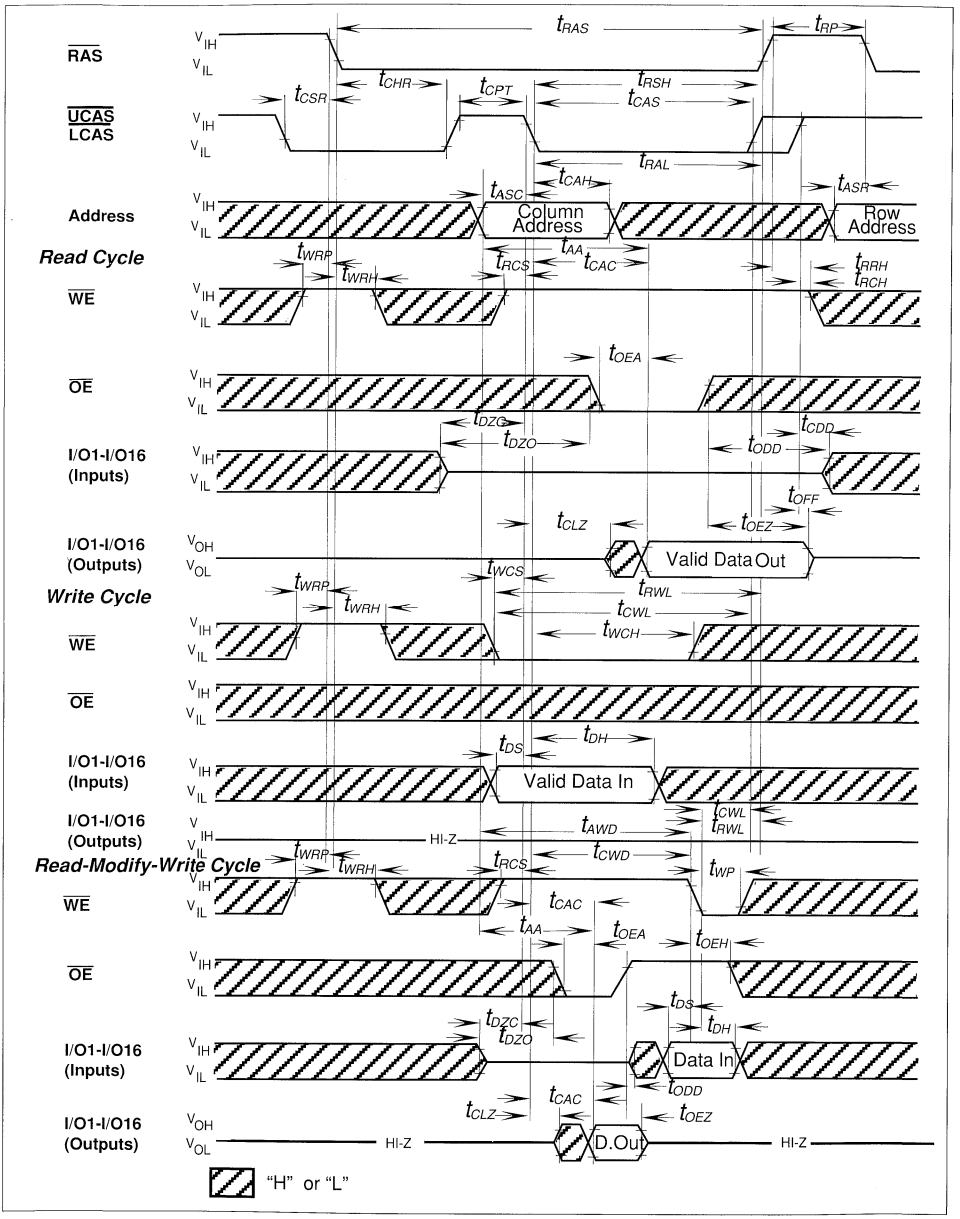
Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Early Write)



Self Refresh



CAS-Before-RAS Refresh Counter Test Cycle

1M x 16-Bit Dynamic RAM (4k-Refresh)

HYB 5116160BSJ-50/-60/-70

Advanced Information

- 1 048 576 words by 16-bit organization
- 0 to 70 °C operating temperature
- Fast access and cycle time
  RAS access time:
  50 ns (-50 version)
  60 ns (-60 version)
  70 ns (-70 version)
  Cycle time:
  95 ns (-50 version)
  110 ns (-60 version)
  130 ns (-70 version)
  CAS access time:
  15 ns (-50,-60 version)
  20 ns (-70 version)
- Fast page mode cycle time
  35 ns (-50 version)
  40 ns (-60 version)
  45 ns (-70 version)
- Single + 5 V (± 10 %) supply
- Low power dissipation
  max. 550 active mW (-50 version)
  max. 495 active mW (-60 version)
  max. 440 active mW (-70 version)
- 11 mW standby (TTL)
  5.5 mW standby (MOS)
- Output unlatched at cycle end allows two-dimensional chip selection
- Read, write, read-modify-write, CAS-before-RAS refresh, RAS-only refresh, hidden refresh and self refresh
- Fast page mode capability
- 2 $\overline{CAS}$ / 1 $\overline{WE}$
- All inputs, outputs and clocks fully TTL-compatible
- 4096 refresh cycles/64 ms
- Plastic Package: P-SOJ-42-1 400 mil

Ordering Information

Type	Ordering Code	Package	Descriptions
HYB 5116160BSJ-50	on request	P-SOJ-42-1 400 mil	DRAM (access time 50 ns)
HYB 5116160BSJ-60	on request	P-SOJ-42-1 400 mil	DRAM (access time 60 ns)
HYB 5116160BSJ-70	on request	P-SOJ-42-1 400 mil	DRAM (access time 70 ns)

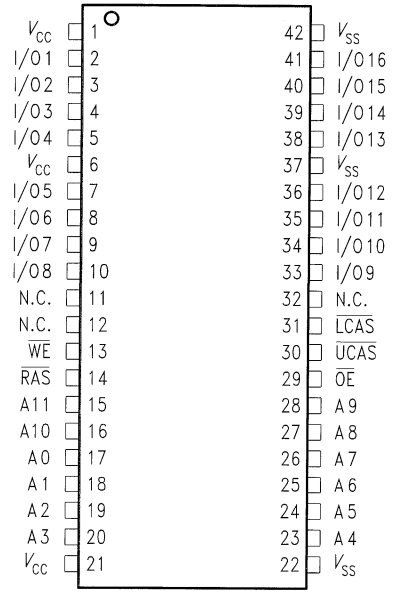
The HYB 5116160BSJ is the new generation dynamic RAM organized as 1 048 576 words by 16 bits. The HYB 5116160BSJ utilizes a submicron CMOS silicon gate process technology, as well as advanced circuit techniques to provide wide operating margins, both internally and for the system user. Multiplexed address inputs permit the HYB 5116160BSJ to be packaged in a standard SOJ 42 400 mil plastic package. These packages provide high system bit densities and are compatible with commonly used automatic testing and insertion equipment. System-oriented features include single + 5 V (± 10 %) power supply, direct interfacing with high-performance logic device families such as Schottky TTL.

Pin Definitions and Functions

Pin No.	Function
A0 to A11	Row Address Inputs
A0 to A7	Column Addess Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{OE}$	Output Enable
I/O1-I/O16	Data Input/Output
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground (0 V)
N.C.	not connected

Pin Configuration
(top view)

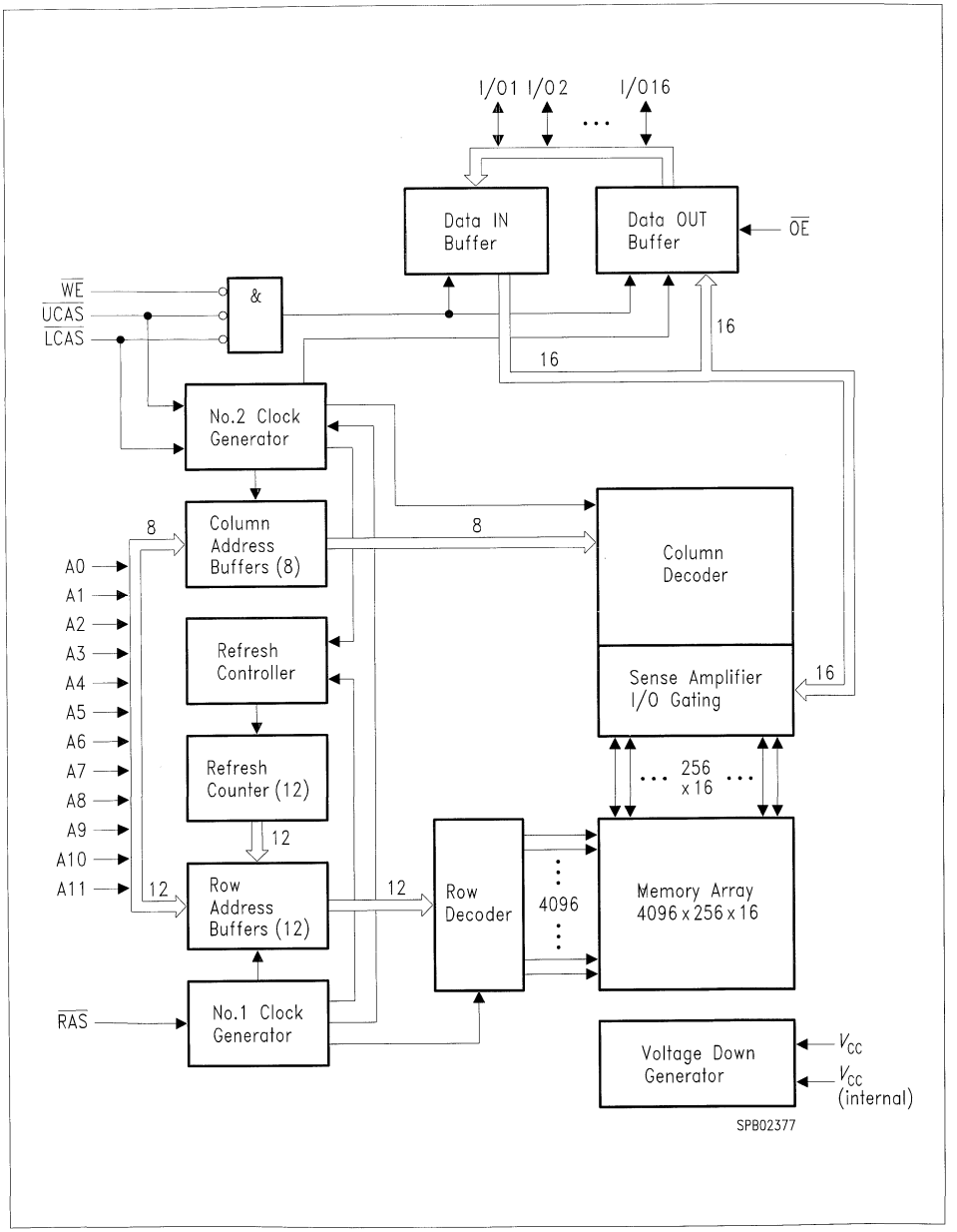
P-SOJ-42 (400 mil)



SPP02376

Truth Table

RAS	LCAS	UCAS	WE	OE	I/O1-I/O8	I/O9-I/O16	Operation
H	H	H	H	H	High-Z	High-Z	Standby
L	H	H	H	H	High-Z	High-Z	Refresh
L	L	H	H	L	Dout	High-Z	Lower byte read
L	H	L	H	L	High-Z	Dout	Upper byte read
L	L	L	H	L	Dout	Dout	Word read
L	L	H	L	H	Din	Don't care	Lower byte write
L	H	L	L	H	Don't care	Din	Upper byte write
L	L	L	L	H	Din	Din	Word write
L	L	L	H	H	High-Z	High-Z	NOP



Block Diagram

Absolute Maximum Ratings

Operating temperature range ..... 0 to 70 °C
Storage temperature range ..... – 55 to 150 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 0.5 to min (V_{CC} + 0.5, 7.0) V
Power supply voltage ..... – 1.0 V to 7.0 V
Power dissipation ..... 1.0 W
Data out current (short circuit) ..... 50 mA

Note:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	V_{CC} + 0.5	V	1)
Input low voltage	V_{IL}	– 0.5	0.8	V	1)
Output high voltage (I_{OUT} = – 5 mA)	V_{OH}	2.4	–	V	1)
Output low voltage (I_{OUT} = 4.2 mA)	V_{OL}	–	0.4	V	1)
Input leakage current, any input (0 V ≤ V_{IH} ≤ V_{CC} + 0.3 V, all other pins = 0 V)	$I_{I(L)}$	– 10	10	µA	1)
Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ V_{CC} + 0.3 V)	$I_{O(L)}$	– 10	10	µA	1)
Average V_{CC} supply current:	I_{CC1}				
-50 ns version		–	100	mA	2) 3) 4)
-60 ns version		–	90	mA	2) 3) 4)
-70 ns version		–	80	mA	2) 3) 4)
($\overline{RAS}$, $\overline{CAS}$, address cycling, t_{RC} = t_{RC} min.)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	2	mA	–
Average V_{CC} supply current, during $\overline{RAS}$-only refresh cycles:	I_{CC3}				
-50 ns version		–	100	mA	2) 4)
-60 ns version		–	90	mA	2) 4)
-70 ns version		–	80	mA	2) 4)
($\overline{RAS}$ cycling: $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)					

DC Characteristics (cont'd)

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current, during fast page mode: -50 ns version	I_{CC4}	–	85	mA	2) 3) 4)
-60 ns version		–	75	mA	2) 3) 4)
-70 ns version		–	65	mA	2) 3) 4)
($\overline{RAS}$ = V_{IL}, CAS, address cycling, t_{PC} = t_{PC} min.)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	–	1	mA	1)
Average V_{CC} supply current, during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode: -50 ns version	I_{CC6}	–	100	mA	2) 4)
-60 ns version		–	90	mA	2) 4)
-70 ns version		–	80	mA	2) 4)
($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min.)					
Average Self Refresh Current ($\overline{CBR}$ cycle with t_{RAS} > t_{RASS}min., $\overline{CAS}$ held low, $\overline{WE}$ = V_{cc} – 0.2 V, Address and Din = V_{cc} – 0.2 V or 0.2 V)	I_{CC7}	–	1	mA	

AC Characteristics 5)

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		HYB 5116160 BSJ -50		HYB 5116160 BSJ -60		HYB 5116160 BSJ -70		
		min.	max.	min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	95	–	110	–	130	–	ns
Read-write cycle time	t_{RWC}	135	–	150	–	180	–	ns
Fast page mode cycle time	t_{PC}	35	–	40	–	45	–	ns
Fast page mode read-write cycle time	t_{PRWC}	75	–	80	–	95	–	ns
Access time from $\overline{RAS}$ 7) 12)	t_{RAC}	–	50	–	60	–	70	ns

AC Characteristics (cont'd) [5]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		HYB 5116160 BSJ -50		HYB 5116160 BSJ -60		HYB 5116160 BSJ -70		
		min.	max.	min.	max.	min.	max.	
Access time from $\overline{CAS}$ [7) 12)]	t_{CAC}	–	15	–	15	–	20	ns
Access time from column address [7) 13)]	t_{AA}	–	25	–	30	–	35	ns
Access time from $\overline{CAS}$ precharge [7)]	t_{CPA}	–	30	–	35	–	40	ns
$\overline{CAS}$ to output in low-Z [7)]	t_{CLZ}	0	–	0	–	0	–	ns
Output buffer turn-off delay [8)]	t_{OFF}	0	15	0	15	0	20	ns
Transition time (rise and fall) [6)]	t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	35	–	40	–	50	–	ns
$\overline{RAS}$ pulse width	t_{RAS}	50	10k	60	10k	70	10k	ns
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	50	200k	60	200k	70	200k	ns
$\overline{CAS}$ precharge to $\overline{RAS}$ Delay	t_{RHCP}	30	–	35	–	40	–	ns
$\overline{CAS}$ precharge to $\overline{WE}$ (FPMR RMW)	t_{CPWD}	50	–	55	–	65	–	ns
$\overline{RAS}$ hold time	t_{RSH}	15		15	–	20	–	ns
$\overline{CAS}$ hold time	t_{CSH}	50		60	–	70	–	ns
$\overline{CAS}$ pulse width	t_{CAS}	15	10k	15	10k	20	10k	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time [12)]	t_{RCD}	20	35	20	45	20	50	
$\overline{RAS}$ to column address delay time [13)]	t_{RAD}	15	25	15	30	15	35	ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	5	–	ns
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns

AC Characteristics (cont'd) [5]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		HYB 5116160 BSJ -50		HYB 5116160 BSJ -60		HYB 5116160 BSJ -70		
		min.	max.	min.	max.	min.	max.	
Row address hold time	t_{RAH}	10	–	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns
Column address hold time	t_{CAH}	10	–	15	–	15	–	ns
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	–	30	–	35	–	ns
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns
Read command hold time [9]	t_{RCH}	0	–	0	–	0	–	ns
Read command hold time referenced to $\overline{RAS}$ [9]	t_{RRH}	0	–	0	–	0	–	ns
Write command hold time	t_{WCH}	10	–	15	–	15	–	ns
Write command pulse width	t_{WP}	10	–	15	–	15	–	ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	–	15	–	20	–	ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	–	15	–	20	–	ns
Data setup time [10]	t_{DS}	0	–	0	–	0	–	ns
Data hold time [10]	t_{DH}	10	–	15	–	15	–	ns
Refresh period	t_{REF}	–	64	–	64	–	64	ms
Write command setup time [11]	t_{WCS}	0	–	0	–	0	–	ns
$\overline{CAS}$ to $\overline{WE}$ delay time [11]	t_{CWD}	35	–	35	–	45	–	ns
$\overline{RAS}$ to $\overline{WE}$ delay time [11]	t_{RWD}	70	–	80	–	95	–	ns

AC Characteristics (cont'd) [5]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		HYB 5116160 BSJ -50		HYB 5116160 BSJ -60		HYB 5116160 BSJ -70		
		min.	max.	min.	max.	min.	max.	
Column address to $\overline{WE}$ delay time [11]	t_{AWD}	45	–	50	–	60	–	ns
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CSR}	10	–	10	–	10	–	ns
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CHR}	10	–	10	–	10	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	0	–	0	–	0	–	ns
$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ counter test cycle)	t_{CPT}	35	–	40	–	40	–	ns
Write to $\overline{RAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{WRP}	10	–	10	–	10	–	ns
Write hold time referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{WRH}	10	–	10	–	10	–	ns
$\overline{OE}$ command hold time	t_{OEH}	15	–	15	–	20	–	ns
$\overline{OE}$ access time	t_{OEA}	–	15	–	15	–	20	ns
Output buffer turn-off delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	ns
Data to $\overline{CAS}$ low delay [15]	t_{DZC}	0	–	0	–	0	–	ns
Data to $\overline{OE}$ low delay [15]	t_{DZO}	0	–	0	–	0	–	ns
$\overline{CAS}$ high to data delay [16]	t_{CDD}	15	–	15	–	20	–	ns
$\overline{OE}$ high to data delay [16]	t_{ODD}	15	–	15	–	20	–	ns
$\overline{RAS}$ pulse width during self refresh	t_{RASS}	100k	–	100k	–	10 k	–	ns

AC Characteristics (cont'd) [5]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		HYB 5116160 BSJ -50		HYB 5116160 BSJ -60		HYB 5116160 BSJ -70		
		min.	max.	min.	max.	min.	max.	
$\overline{RAS}$ precharge time during self refresh	t_{RPS}	95	–	110	–	130	–	ns
$\overline{CAS}$ hold time during self refresh	t_{CHS}	– 50	–	– 50	–	– 50	–	ns

Capacitance

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A11)	C_{I1}	–	5	pF
Input capacitance ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}	–	7	pF
I/O capacitance (I/O1-I/O16)	C_{IO}	–	7	pF

Notes:

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.

4) Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4} it can be changed once or less during a fast page mode cycle (t_{PC}).

5) An initial pause of 200 µs is required after power-up followed by 8 RAS cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS cycles are required.

6) $V_{IH\ (min.)}$ and $V_{IL\ (max.)}$ are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.

7) Measured with a load equivalent to 2 TTL loads and 100 pF.

8) $t_{OFF\ (max.)}$ and $t_{OEZ\ (max.)}$ define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.

9) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

10) These parameters are referenced to the CAS leading edge in early write cycles and to the WE leading edge in read-write cycles.

11) t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS\ (min.)}$, the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} > t_{RWD\ (min.)}$, $t_{CWD} > t_{CWD\ (min.)}$, $t_{AWD} > t_{AWD\ (min.)}$ and $t_{CPWD} > t_{CPWD\ (min.)}$, the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.

12) Operation within the $t_{RCD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RCD\ (max.)}$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD\ (max.)}$ limit, then access time is controlled by t_{CAC}.

13) Operation within the $t_{RAD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RAD\ (max.)}$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD\ (max.)}$ limit, then access time is controlled by t_{AA}.

14) AC measurements assume t_T = 5 ns.

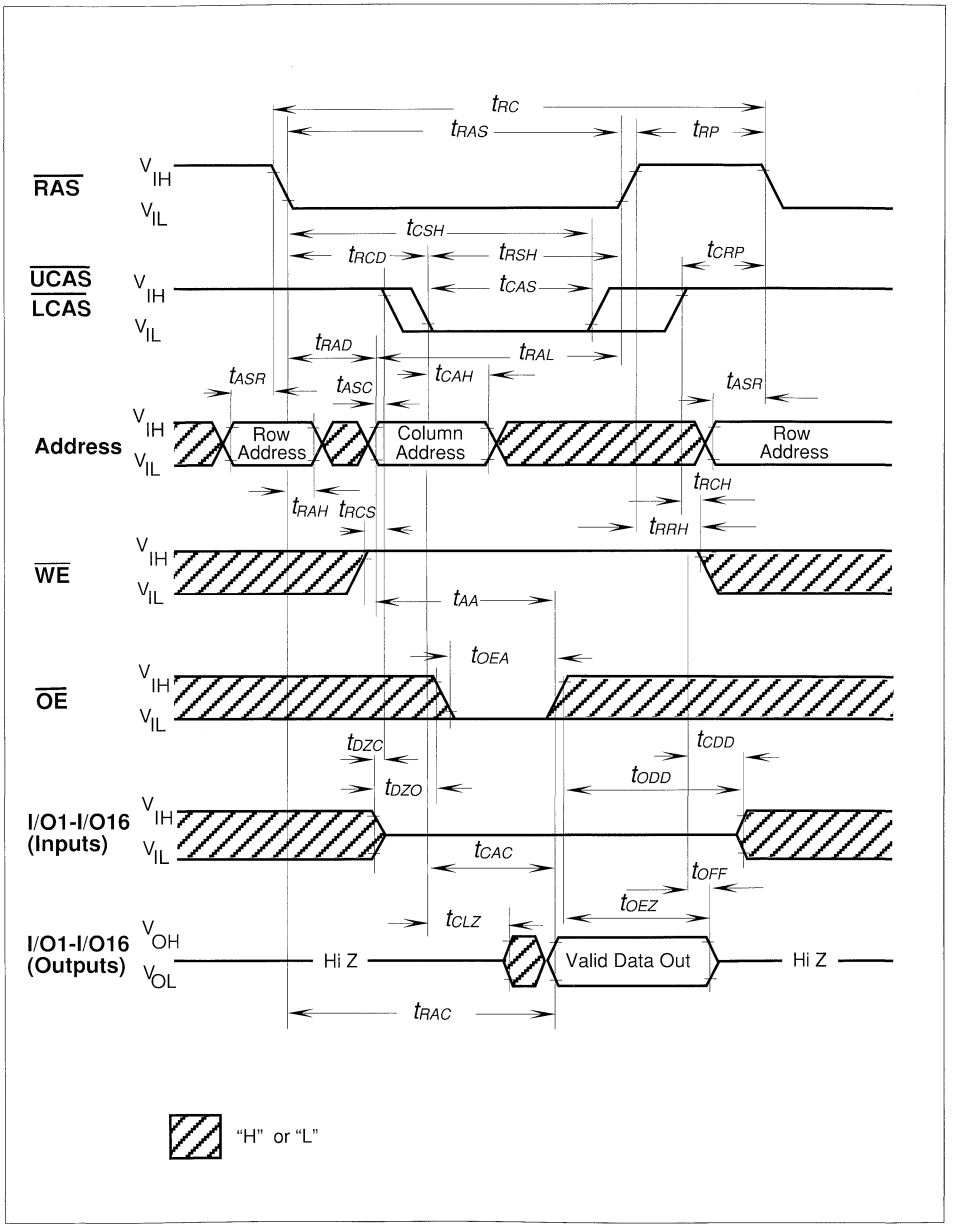
15) Either t_{DZC} or t_{DZO} must be satisfied.

16) Either t_{CDD} or t_{ODD} must be satisfied.

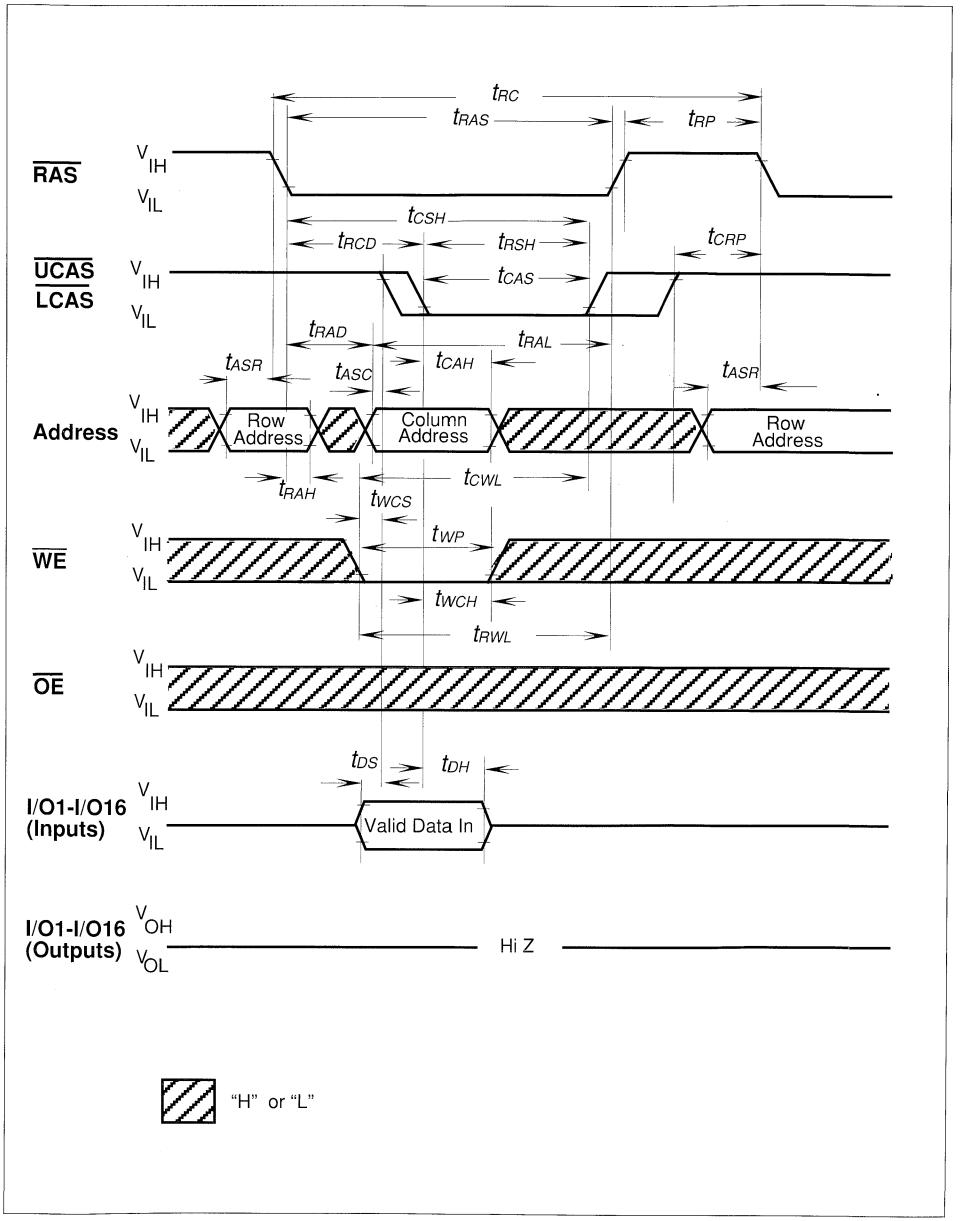
17) When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:

If row addresses are being refreshed on an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh.

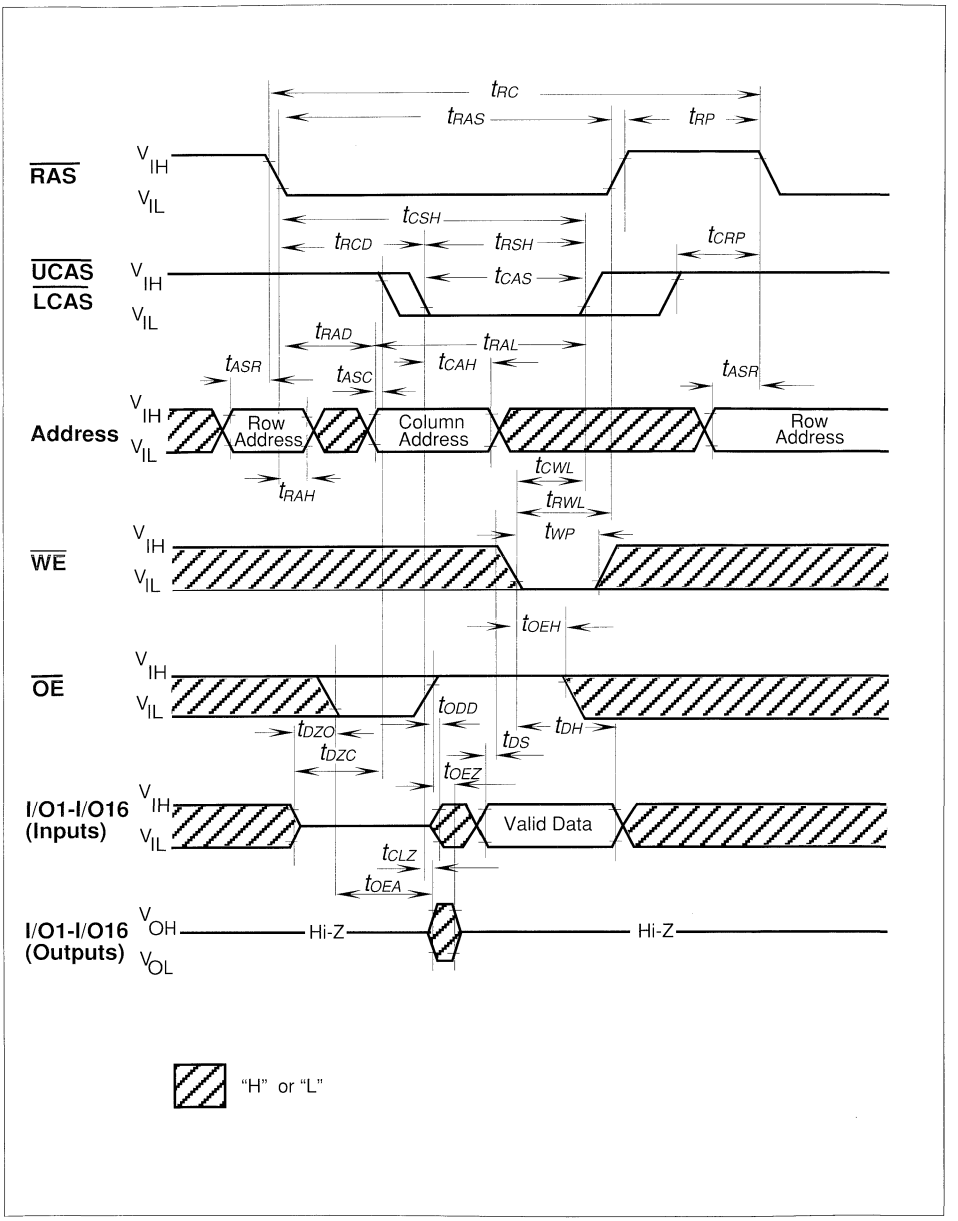
If row addresses are being refreshed in any other manner (ROR - Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh.


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
UCAS
LCAS
tCAS
tRAD
tRAL
tASR
tASC
tCAH
tASR
Address
Row Address
Column Address
Row Address
tRCH
tRAH
tRCS
tRRH
WE
tAA
tOEA
OE
tDZC
tCDD
tDZO
tODD
I/O1-I/O16 (Inputs)
tCAC
tOFF
tOEZ
tCLZ
I/O1-I/O16 (Outputs)
VOH
VOL
Hi Z
Valid Data Out
Hi Z
tRAC
"H" or "L"

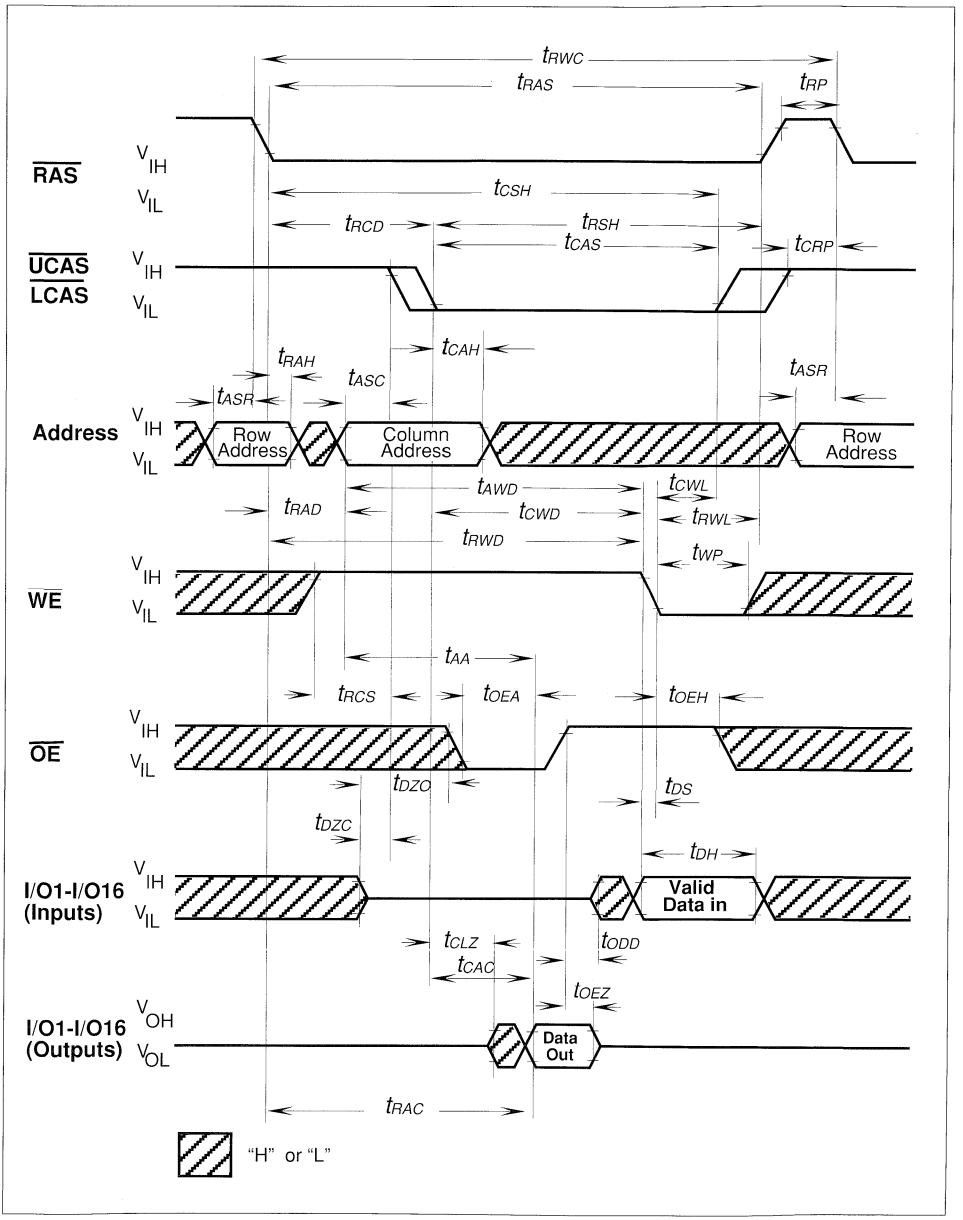
Read Cycle



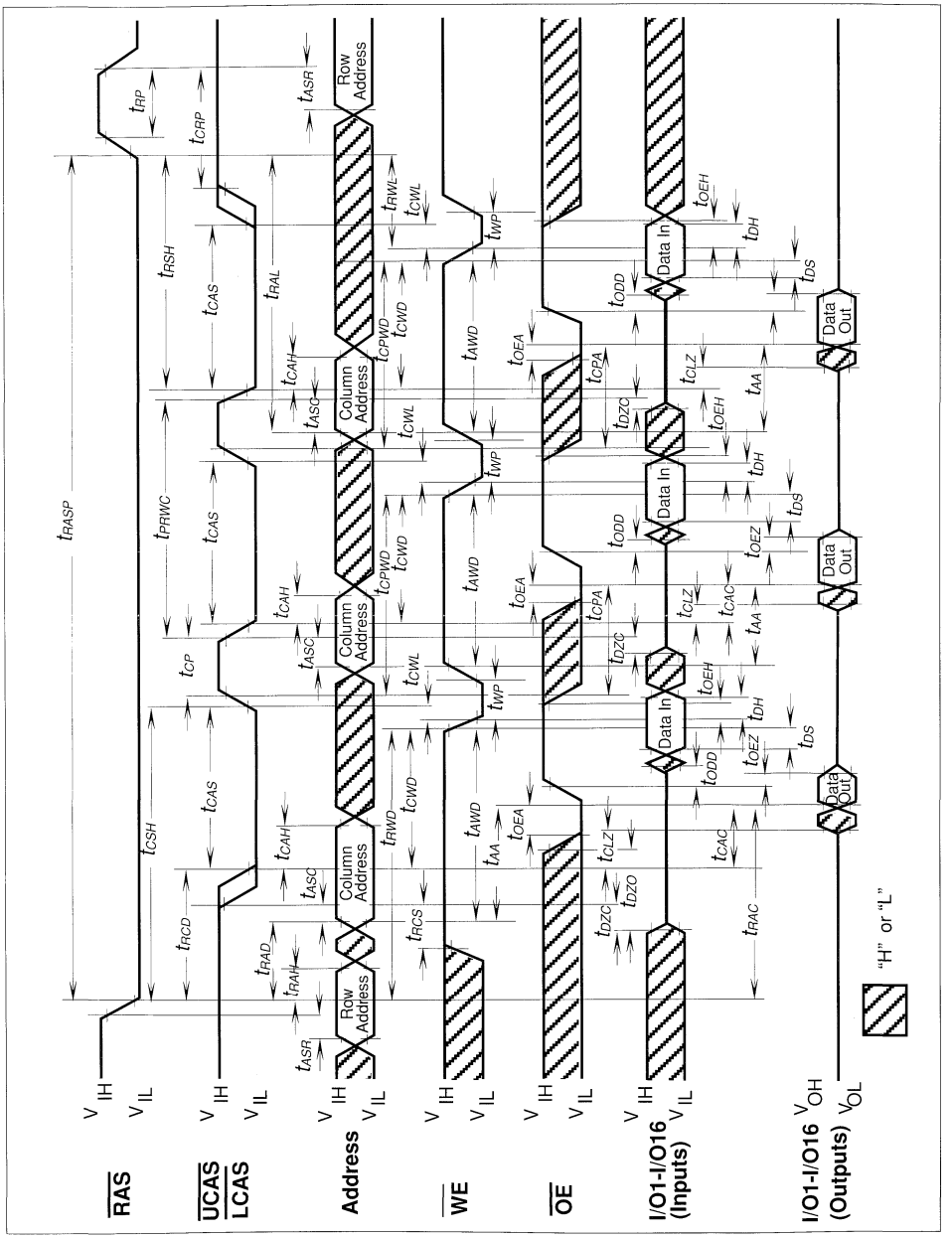
Write Cycle (Early Write)



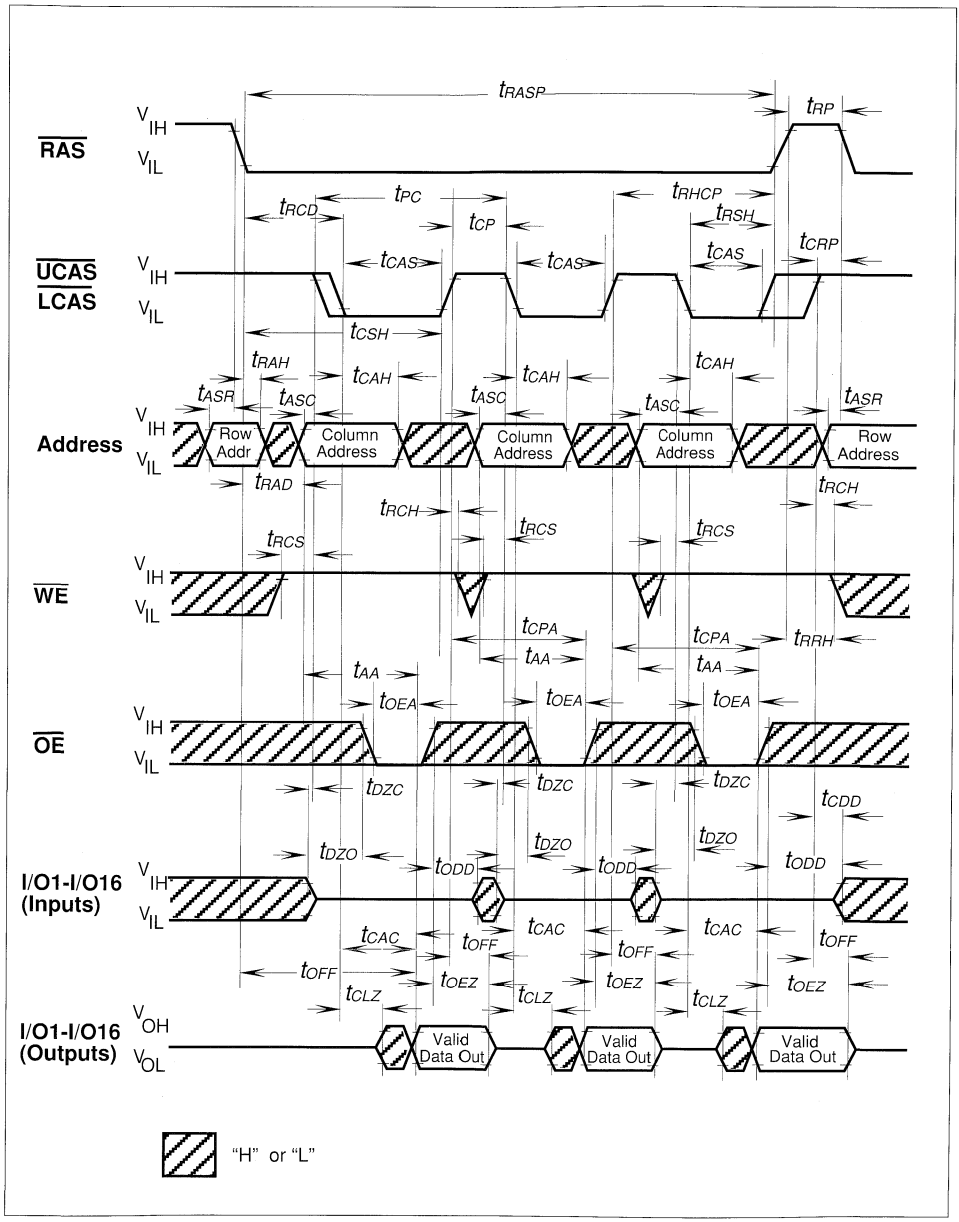
Write Cycle ($\overline{OE}$ Controlled Write)



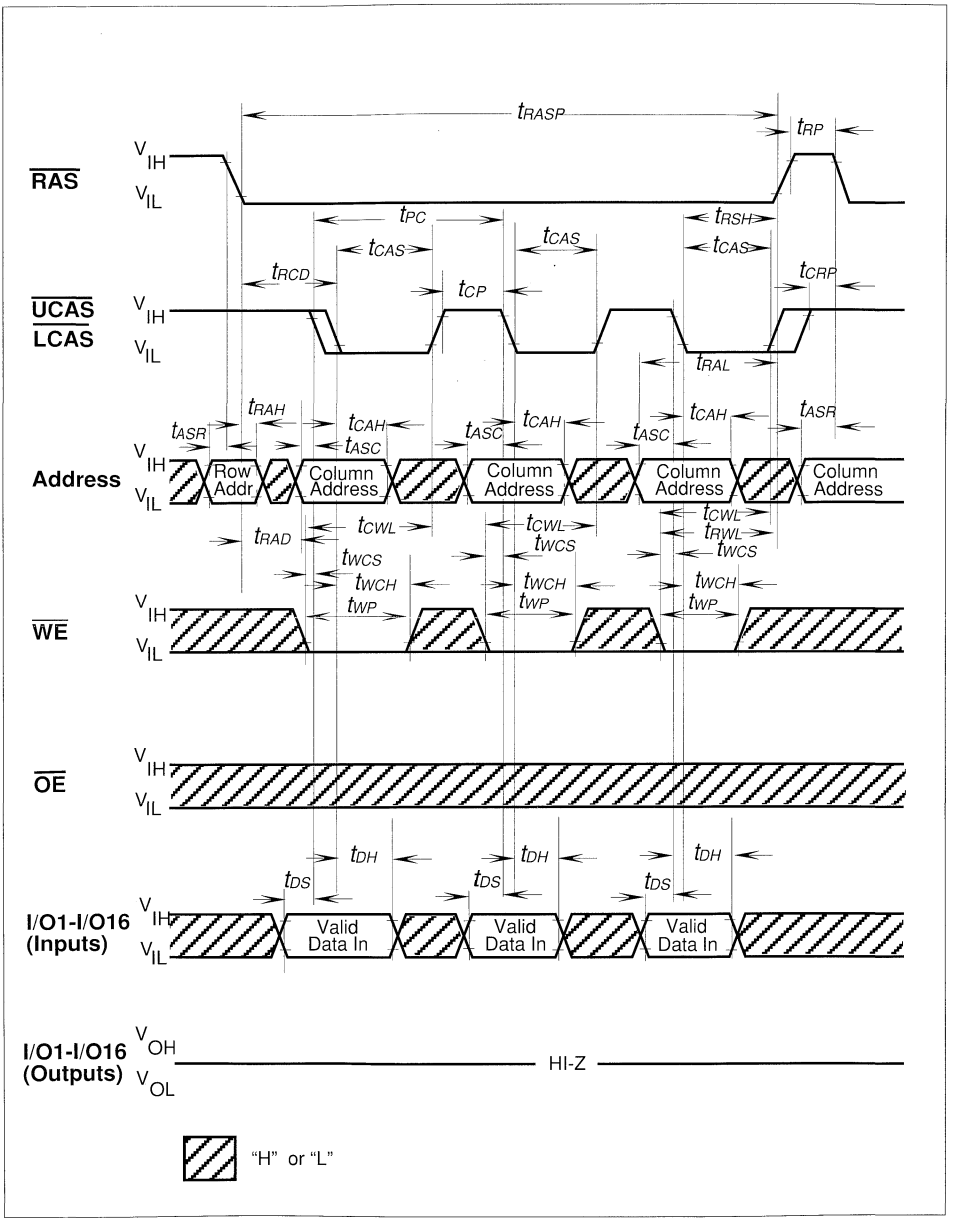
Read-Write (Read-Modify-Write) Cycle



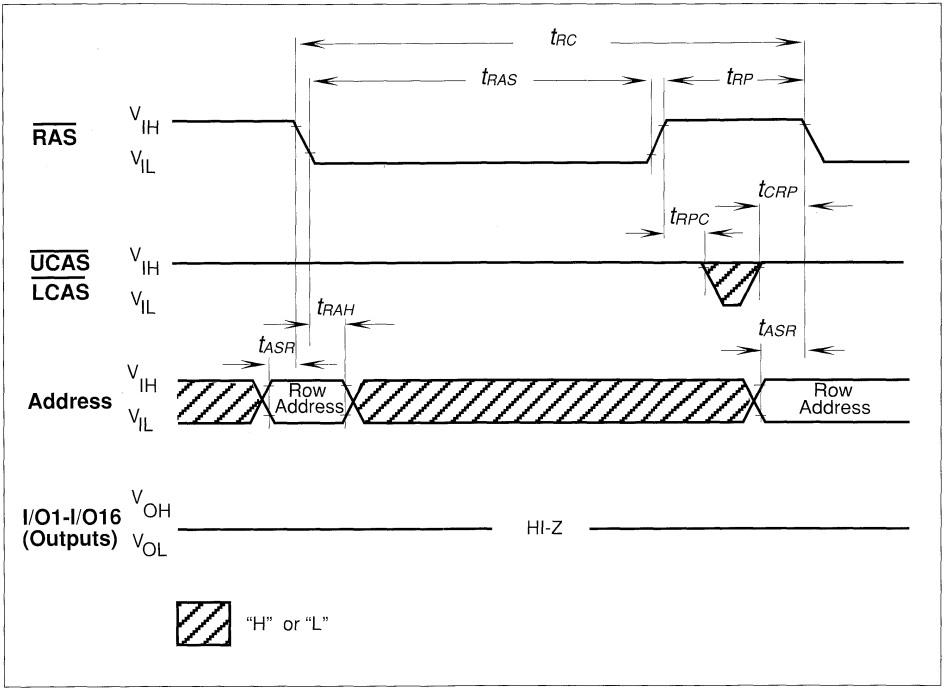
Fast Page Mode Read-Modify-Write Cycle



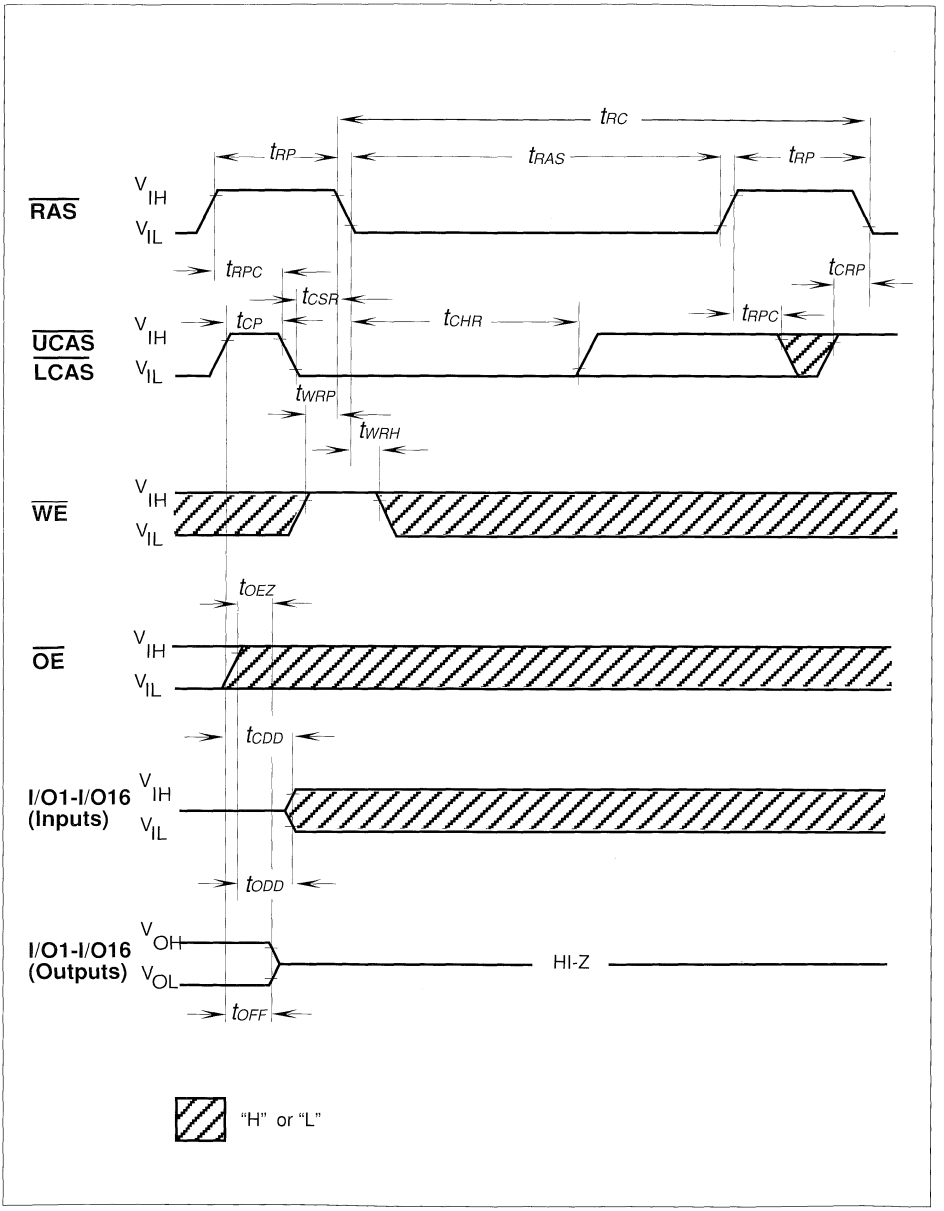
Fast Page Mode Read Cycle



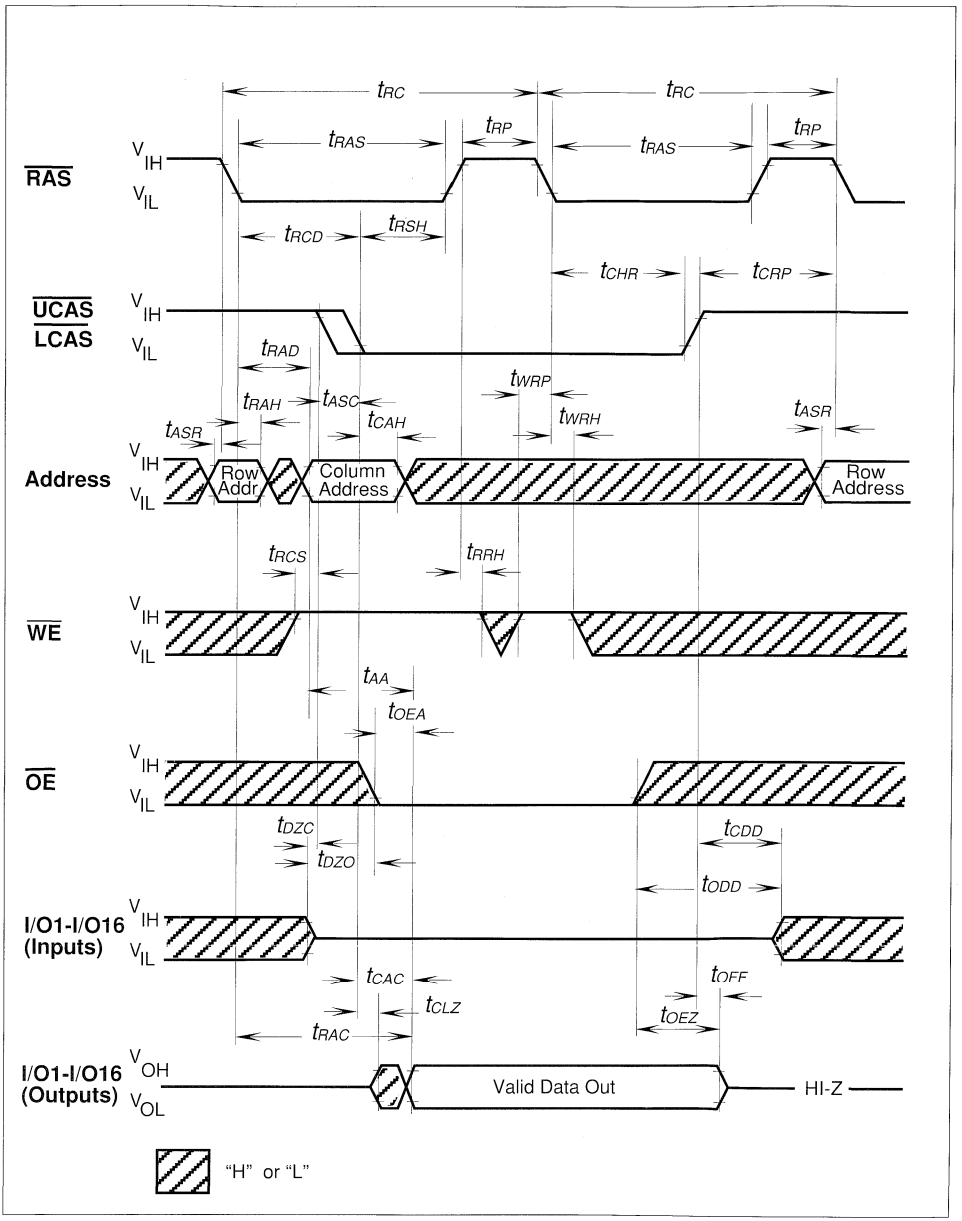
Fast Page Mode Early Write Cycle



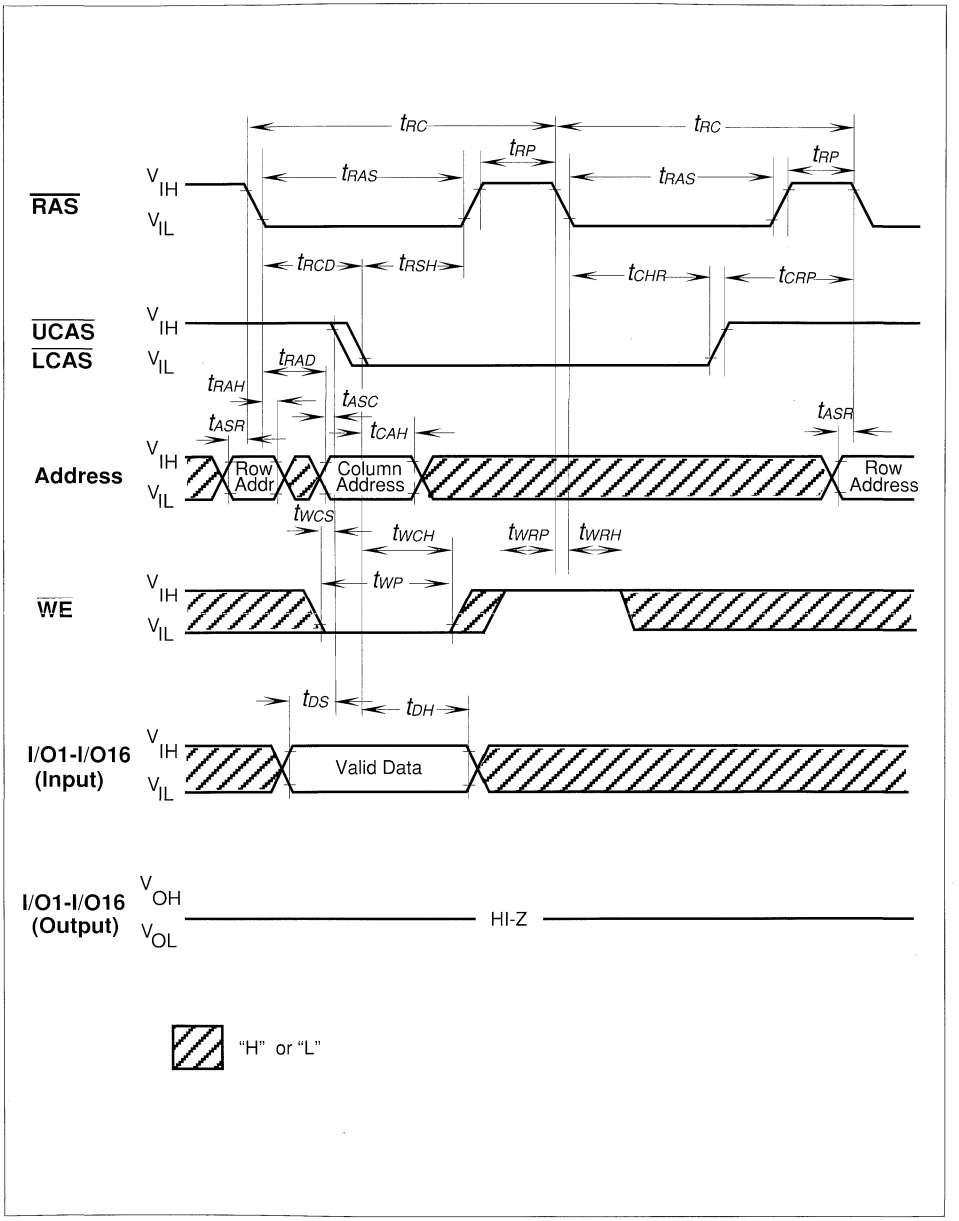
$\overline{RAS}$-Only Refresh Cycle



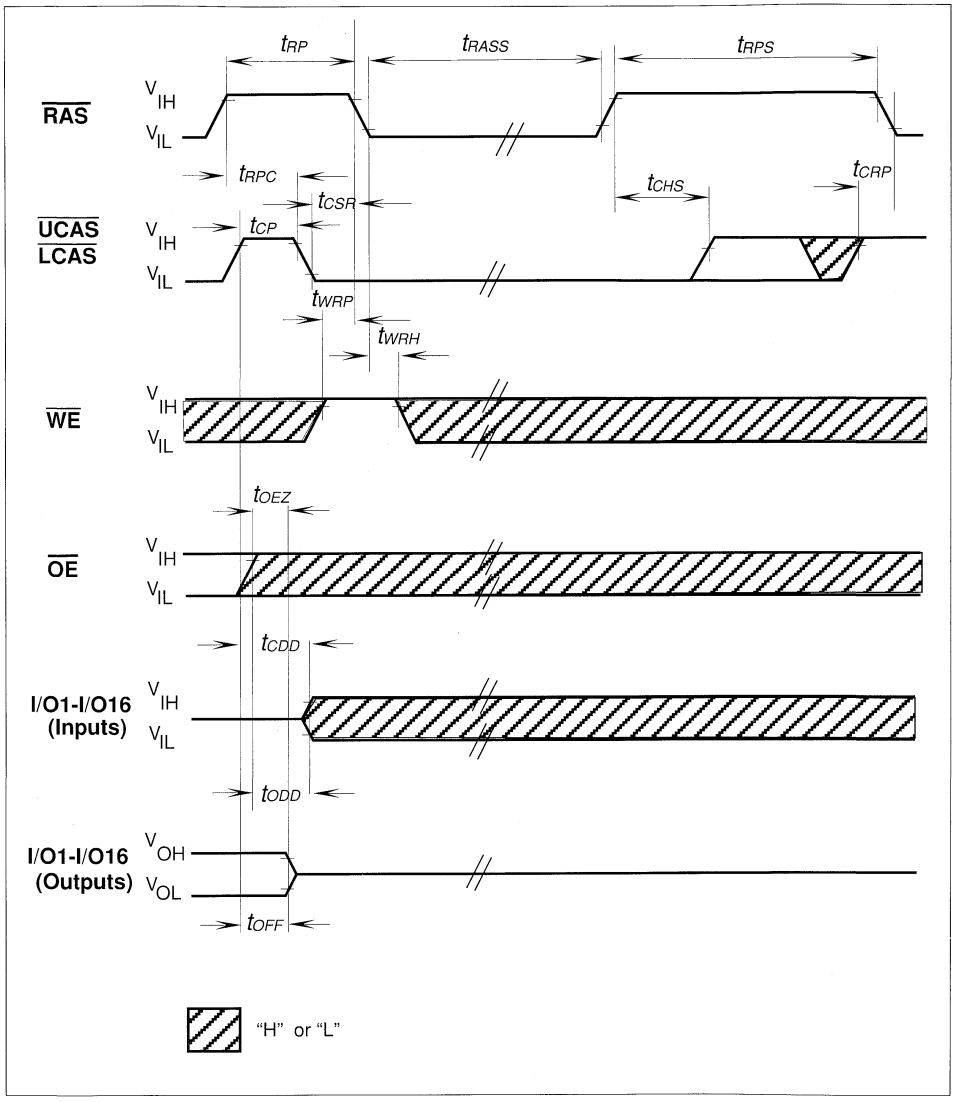
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



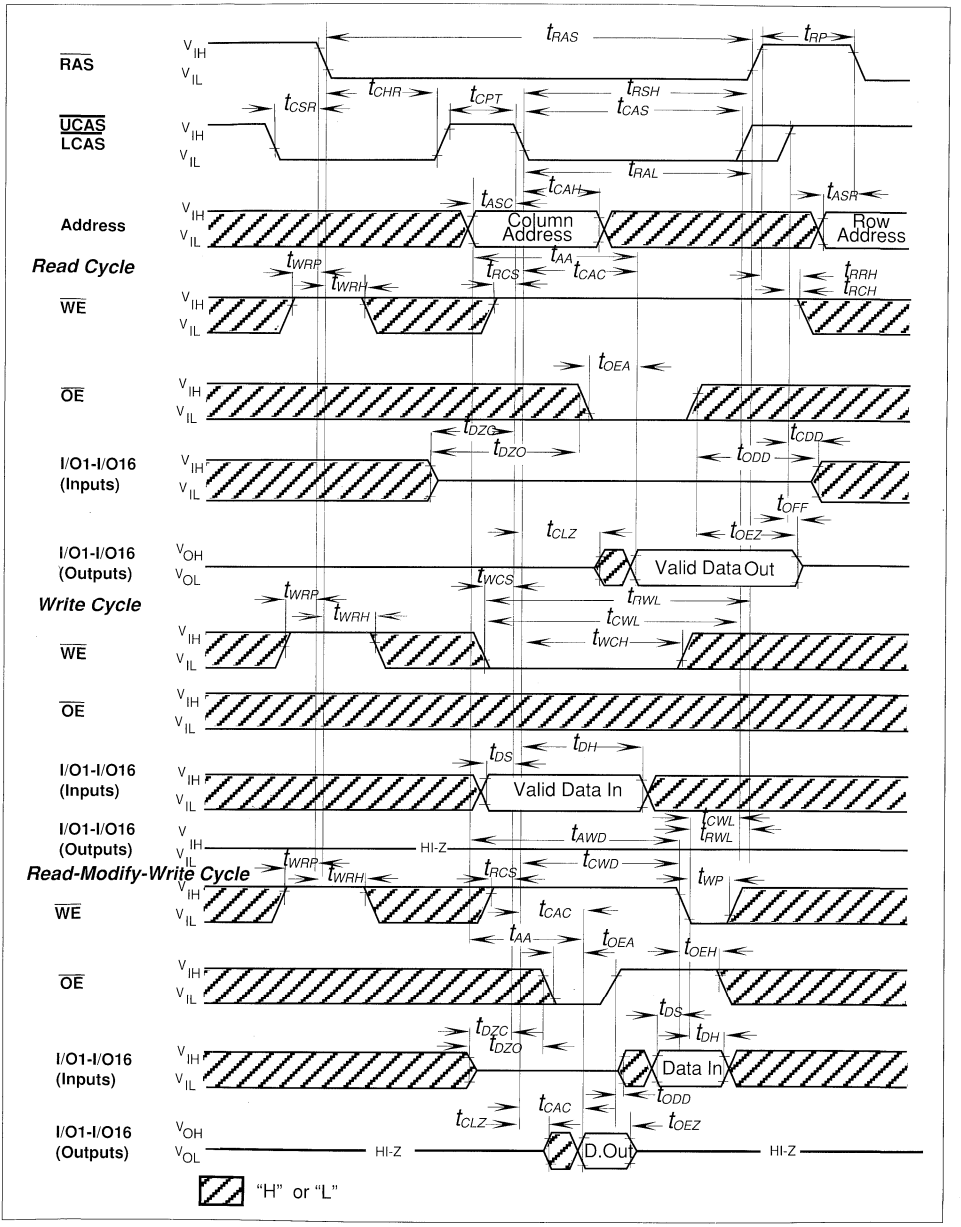
Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Early Write)



Self Refresh



CAS-Before-RAS Refresh Counter Test Cycle

1M x 16-Bit Dynamic RAM (1k & 4k-Refresh)

HYB 3116160BSJ-50/-60/-70
HYB 3118160BSJ-50/-60/-70

Advanced Information

- 1 048 576 words by 16-bit organization
- 0 to 70 °C operating temperature
- Fast access and cycle time
  $\overline{RAS}$ access time:
  50 ns (-50 version)
  60 ns (-60 version)
  70 ns (-70 version)
  Cycle time:
  95 ns (-50 version)
  110 ns (-60 version)
  130 ns (-70 version)
  $\overline{CAS}$ access time:
  15 ns (-50,-60 version)
  20 ns (-70 version)
- Fast page mode cycle time
  35 ns (-50 version)
  40 ns (-60 version)
  45 ns (-70 version)
- Single + 3.3 V (± 0.3 V) supply
- Low power dissipation
  max. 990 active mW (HYB3118160BSJ-50)
  max. 935 active mW (HYB3118160BSJ-60)
  max. 880 active mW (HYB3118160BSJ-70)
  max. 550 active mW (HYB3116160BSJ-50)
  max. 495 active mW (HYB3116160BSJ-60)
  max. 440 active mW (HYB3116160BSJ-70)
  11 mW standby (TTL)
  5.5 mW standby (MOS)
- Output unlatched at cycle end allows two-dimensional chip selection
- Read, write, read-modify-write, $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, hidden refresh, self refresh
- Fast page mode capability
- 2 $\overline{CAS}$ / 1 $\overline{WE}$
- All inputs, outputs and clocks fully TTL-compatible
- 1024 refresh cycles / 16 ms for HYB 3118160BSJ
- 4096 refresh cycles / 64 ms for HYB 3116160BSJ
- Plastic Package: P-SOJ-42-1 400 mil

Ordering Information

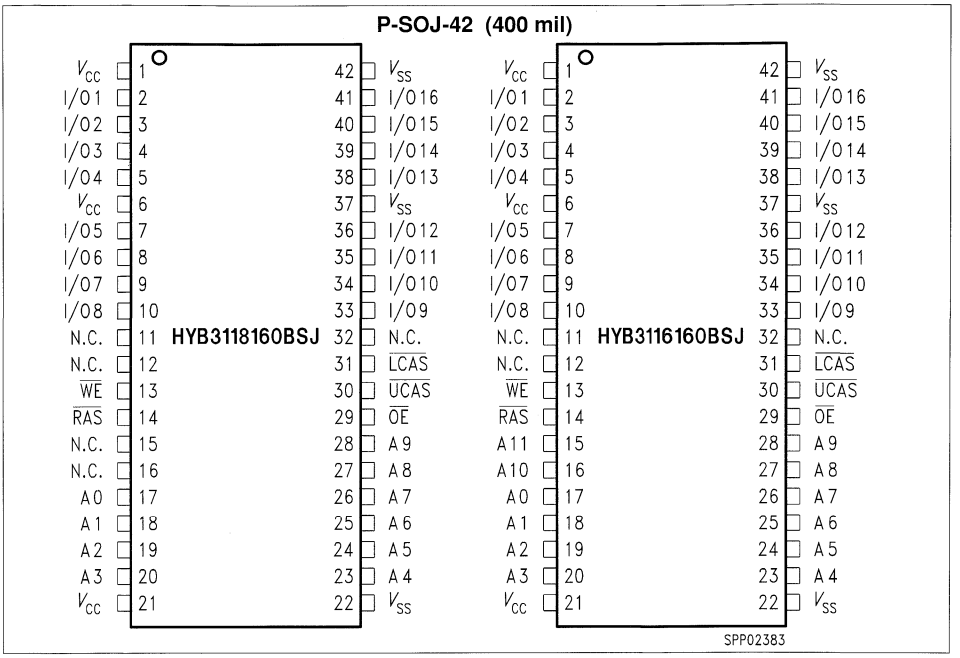
Type	Ordering Code	Package	Descriptions
HYB 3116160BSJ-50	on request	P-SOJ-42-1 400 mil	DRAM (access time 50 ns)
HYB 3116160BSJ-60	on request	P-SOJ-42-1 400 mil	DRAM (access time 60 ns)
HYB 3116160BSJ-70	on request	P-SOJ-42-1 400 mil	DRAM (access time 70 ns)
HYB 3118160BSJ-50	on request	P-SOJ-42-1 400 mil	DRAM (access time 50 ns)
HYB 3118160BSJ-60	on request	P-SOJ-42-1 400 mil	DRAM (access time 60 ns)
HYB 3118160BSJ-70	on request	P-SOJ-42-1 400 mil	DRAM (access time 70 ns)

The HYB 3116(8)160BSJ is the new generation dynamic RAM organized as 1 048 576 words by 16 bits. The HYB 3116(8)160BSJ utilizes a submicron CMOS silicon gate process technology, as well as advanced circuit techniques to provide wide operating margins, both internally and for the system user. Multiplexed address inputs permit the HYB 3116(8)160BSJ to be packaged in a standard SOJ 42 400 mil plastic package. These packages provide high system bit densities and are compatible with commonly used automatic testing and insertion equipment. System-oriented features include single + 3.3 V (± 0.3 V) power supply, direct interfacing with high-performance logic device families such as Schottky TTL.

Pin Definitions and Functions

Pin No.	Function
A0 to A9	Row Address Inputs for HYB3118160BSJ
A0 to A9	Column Addess Inputs for HYB3118160BSJ
A0 to A11	Row Address Inputs for HYB3116160BSJ
A0 to A7	Column Address Inputs for HYB3116160BSJ
$\overline{RAS}$	Row Address Strobe
$\overline{OE}$	Output Enable
I/O1-I/O16	Data Input/Output
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power Supply (+ 3.3 V)
V_{SS}	Ground (0 V)
N.C.	not connected

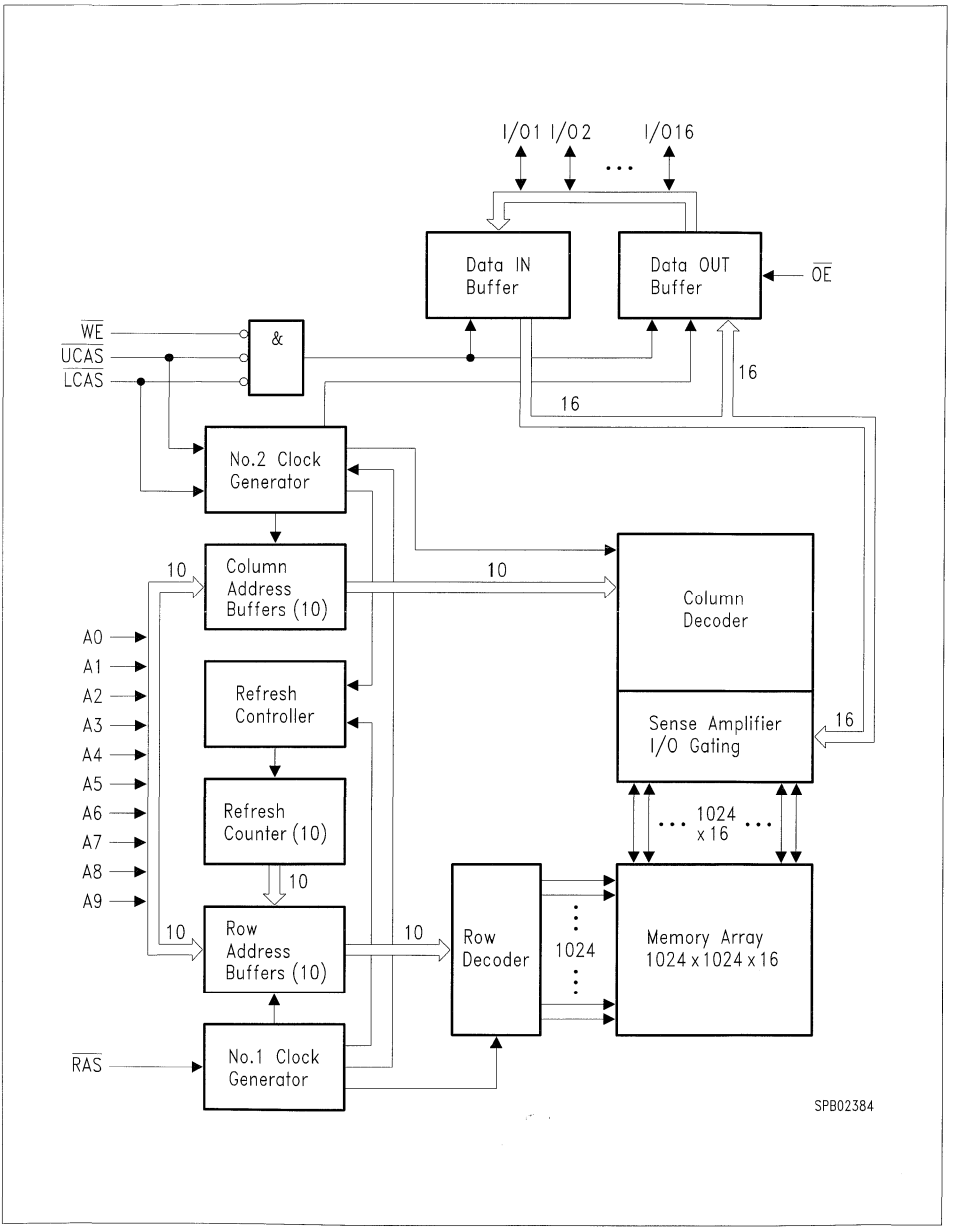
Pin Configuration
(top view)



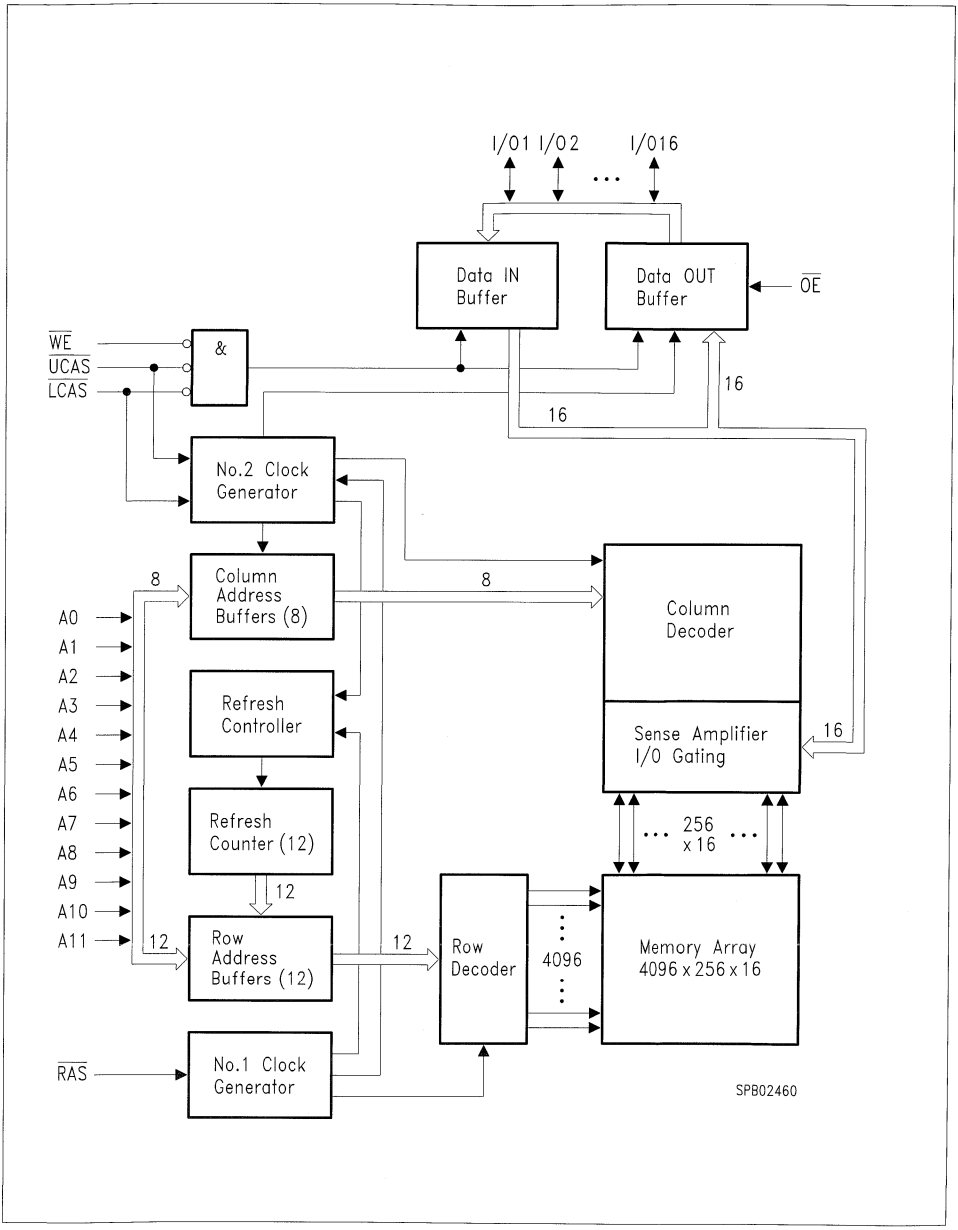
V_{CC}	1	42	V_{SS}	V_{CC}	1	42	V_{SS}
I/O1	2	41	I/O16	I/O1	2	41	I/O16
I/O2	3	40	I/O15	I/O2	3	40	I/O15
I/O3	4	39	I/O14	I/O3	4	39	I/O14
I/O4	5	38	I/O13	I/O4	5	38	I/O13
V_{CC}	6	37	V_{SS}	V_{CC}	6	37	V_{SS}
I/O5	7	36	I/O12	I/O5	7	36	I/O12
I/O6	8	35	I/O11	I/O6	8	35	I/O11
I/O7	9	34	I/O10	I/O7	9	34	I/O10
I/O8	10	33	I/O9	I/O8	10	33	I/O9
N.C.	11	32	N.C.	N.C.	11	32	N.C.
N.C.	12	31	$\overline{LCAS}$	N.C.	12	31	$\overline{LCAS}$
$\overline{WE}$	13	30	$\overline{UCAS}$	$\overline{WE}$	13	30	$\overline{UCAS}$
$\overline{RAS}$	14	29	$\overline{OE}$	$\overline{RAS}$	14	29	$\overline{OE}$
N.C.	15	28	A9	A11	15	28	A9
N.C.	16	27	A8	A10	16	27	A8
A0	17	26	A7	A0	17	26	A7
A1	18	25	A6	A1	18	25	A6
A2	19	24	A5	A2	19	24	A5
A3	20	23	A4	A3	20	23	A4
V_{CC}	21	22	V_{SS}	V_{CC}	21	22	V_{SS}

Truth Table

$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	I/O1-I/O8	I/O9-I/O16	Operation
H	H	H	H	H	High-Z	High-Z	Standby
L	H	H	H	H	High-Z	High-Z	Refresh
L	L	H	H	L	Dout	High-Z	Lower byte read
L	H	L	H	L	High-Z	Dout	Upper byte read
L	L	L	H	L	Dout	Dout	Word read
L	L	H	L	H	Din	Don't care	Lower byte write
L	H	L	L	H	Don't care	Din	Upper byte write
L	L	L	L	H	Din	Din	Word write
L	L	L	H	H	High-Z	High-Z	NOP



Block Diagram for HYB 3118160BSJ



Block Diagram for HYB3116160BSJ

Absolute Maximum Ratings

Operating temperature range ..... 0 to 70 °C
Storage temperature range ..... – 55 to 150 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 0.5 to min (V_{CC} + 0.5, 4.6) V
Power supply voltage ..... – 1.0 V to 7.0 V
Power dissipation ..... 1.0 W
Data out current (short circuit) ..... 50 mA

Note:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics (values in brackets for HYB3116160BSJ)
T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 3 V ± 0.3 V, t_T = 5 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.0	V_{CC} + 0.5	V	1)
Input low voltage	V_{IL}	– 0.5	0.8	V	1)
TTL Output high voltage (I_{OUT} = – 2 mA)	V_{OH}	2.4	–	V	1)
TTL Output low voltage (I_{OUT} = 2 mA)	V_{OL}	–	0.4	V	1)
CMOS Output high voltage (I_{OUT} = – 100 A)	V_{OH}	V_{CC} – 0.2	–	V	1)
CMOS Output low voltage (I_{OUT} = 100 A)	V_{OL}	–	0.2	V	1)
Input leakage current,any input (0 V ≤ V_{IH} ≤ V_{CC} + 0.3 V, all other pins = 0 V)	$I_{I(L)}$	– 10	10	µA	1)
Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ V_{CC} + 0.3 V)	$I_{O(L)}$	– 10	10	µA	1)
Average V_{CC} supply current:	I_{CC1}				
-50 ns version		–	200(100)	mA	2) 3) 4)
-60 ns version		–	180 (90)	mA	2) 3) 4)
-70 ns version		–	160 (80)	mA	2) 3) 4)
($\overline{RAS}$, $\overline{CAS}$, address cycling, t_{RC} = t_{RC} min.)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	2	mA	–

DC Characteristics (values in brackets for HYB3116160BSJ) (cont'd)
T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 3 V ± 0.3 V, t_T = 5 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current, during $\overline{RAS}$-only refresh cycles: -50 ns version	I_{CC3}	–	200(100)	mA	2) 4)
-60 ns version		–	180 (90)	mA	2) 4)
-70 ns version		–	160 (80)	mA	2) 4)
($\overline{RAS}$ cycling: $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)					
Average V_{CC} supply current, during fast page mode: -50 ns version	I_{CC4}	–	90 (85)	mA	2) 3) 4)
-60 ns version		–	80 (75)	mA	2) 3) 4)
-70 ns version		–	70 (65)	mA	2) 3) 4)
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling, t_{PC} = t_{PC} min.)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	–	1	mA	1)
Average V_{CC} supply current, during $\overline{CAS}$-before-RAS refresh mode: -50 ns version	I_{CC6}	–	200(100)	mA	2) 4)
-60 ns version		–	180 (90)	mA	2) 4)
-70 ns version		–	160 (80)	mA	2) 4)
($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min.)					
Average Self Refresh Current	I_{CC7}	–	1	mA	
($\overline{CBR}$ cycle with t_{RAS} > t_{RASS} min., $\overline{CAS}$ held low, $\overline{WE}$ = V_{CC} – 0.2 V, Address and Din = V_{CC} – 0.2 V or 0.2 V)					

AC Characteristics [5]

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3V , t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		HYB 3116(8)160 BSJ-50		HYB 3116(8)160 BSJ-60		HYB 3116(8)160 BSJ-70		
		min.	max.	min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	95	–	110	–	130	–	ns
Read-write cycle time	t_{RWC}	135	–	150	–	180	–	ns
Fast page mode cycle time	t_{PC}	35	–	40	–	45	–	ns
Fast page mode read-write cycle time	t_{PRWC}	75	–	80	–	95	–	ns
Access time from $\overline{RAS}$ [7) 12)]	t_{RAC}	–	50	–	60	–	70	ns
Access time from $\overline{CAS}$ [7) 12)]	t_{CAC}	–	15	–	15	–	20	ns
Access time from column address [7) 13)]	t_{AA}	–	25	–	30	–	35	ns
Access time from $\overline{CAS}$ precharge [7)]	t_{CPA}	–	30	–	35	–	40	ns
$\overline{CAS}$ to output in low-Z [7)]	t_{CLZ}	0	–	0	–	0	–	ns
Output buffer turn-off delay [8)]	t_{OFF}	0	15	0	15	0	20	ns
Transition time (rise and fall) [6)]	t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	35	–	40	–	50	–	ns
$\overline{RAS}$ pulse width	t_{RAS}	50	10k	60	10k	70	10k	ns
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	50	200k	60	200k	70	200k	ns
$\overline{CAS}$ precharge to $\overline{RAS}$ Delay	t_{RHCP}	30	–	35	–	40	–	ns
$\overline{CAS}$ precharge to $\overline{WE}$ (FPMR RMW)	t_{CPWD}	50	–	55	–	65	–	ns
$\overline{RAS}$ hold time	t_{RSH}	15		15	–	20	–	ns
$\overline{CAS}$ hold time	t_{CSH}	50		60	–	70	–	ns
$\overline{CAS}$ pulse width	t_{CAS}	15	10k	15	10k	20	10k	ns

AC Characteristics (cont'd) [5]

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3V , t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		HYB 3116(8)160 BSJ-50		HYB 3116(8)160 BSJ-60		HYB 3116(8)160 BSJ-70		
		min.	max.	min.	max.	min.	max.	
$\overline{RAS}$ to $\overline{CAS}$ delay time [12]	t_{RCD}	20	35	20	45	20	50	
$\overline{RAS}$ to column address delay time [13]	t_{RAD}	15	25	15	30	15	35	ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	5	–	ns
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns
Row address hold time	t_{RAH}	10	–	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns
Column address hold time	t_{CAH}	10	–	15	–	15	–	ns
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	–	30	–	35	–	ns
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns
Read command hold time [9]	t_{RCH}	0	–	0	–	0	–	ns
Read command hold time referenced to $\overline{RAS}$ [9]	t_{RRH}	0	–	0	–	0	–	ns
Write command hold time	t_{WCH}	10	–	15	–	15	–	ns
Write command pulse width	t_{WP}	10	–	15	–	15	–	ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	–	15	–	20	–	ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	–	15	–	20	–	ns
Data setup time [10]	t_{DS}	0	–	0	–	0	–	ns
Data hold time [10]	t_{DH}	10	–	15	–	15	–	ns

AC Characteristics (cont'd) [5]

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3V , t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		HYB 3116(8)160 BSJ-50		HYB 3116(8)160 BSJ-60		HYB 3116(8)160 BSJ-70		
		min.	max.	min.	max.	min.	max.	
Refresh period for HYB3118160	t_{REF}	–	16	–	16	–	16	ms
Refresh period for HYB3116160	t_{REF}	–	64	–	64	–	64	ms
Write command setup time [11]	t_{WCS}	0	–	0	–	0	–	ns
$\overline{CAS}$ to $\overline{WE}$ delay time [11]	t_{CWD}	35	–	35	–	45	–	ns
$\overline{RAS}$ to $\overline{WE}$ delay time [11]	t_{RWD}	70	–	80	–	95	–	ns
Column address to $\overline{WE}$ delay time [11]	t_{AWD}	45	–	50	–	60	–	ns
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CSR}	10	–	10	–	10	–	ns
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CHR}	10	–	10	–	10	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5	–	5	–	5	–	ns
$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ counter test cycle)	t_{CPT}	35	–	40	–	40	–	ns
Write to $\overline{RAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{WRP}	10	–	10	–	10	–	ns
Write hold time referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{WRH}	10	–	10	–	10	–	ns
$\overline{OE}$ command hold time	t_{OEH}	15	–	15	–	20	–	ns
$\overline{OE}$ access time	t_{OEA}	–	15	–	15	–	20	ns
Output buffer turn-off delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	ns
Data to $\overline{CAS}$ low delay [15]	t_{DZC}	0	–	0	–	0	–	ns

AC Characteristics (cont'd) [5]

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3V , t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		HYB 3116(8)160 BSJ-50		HYB 3116(8)160 BSJ-60		HYB 3116(8)160 BSJ-70		
		min.	max.	min.	max.	min.	max.	
Data to $\overline{OE}$ low delay [15]	t_{DZO}	0	–	0	–	0	–	ns
$\overline{CAS}$ high to data delay [16]	t_{CDD}	15	–	15	–	20	–	ns
$\overline{OE}$ high to data delay [16]	t_{ODD}	15	–	15	–	20	–	ns
$\overline{RAS}$ pulse width during self refresh	t_{RASS}	100k	–	100k	–	100k	–	ns
$\overline{RAS}$ precharge time during self refresh	t_{RPS}	95	–	110	–	130	–	ns
$\overline{CAS}$ hold time during self refresh	t_{CHS}	– 50	–	– 50	–	– 50	–	ns

Capacitance

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3 V, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A11)	C_{I1}	–	5	pF
Input capacitance ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}	–	7	pF
I/O capacitance (I/O1-I/O16)	C_{IO}	–	7	pF

Notes:

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.

4) Address can be changed once or less while $\overline{RAS} = V_{IL}$. In the case of I_{CC4} it can be changed once or less during a fast page mode cycle (t_{PC}).

5) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS cycles are required.

6) $V_{IH\ (min.)}$ and $V_{IL\ (max.)}$ are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.

7) Measured with a load equivalent to 100 pF and at V_{oh} = 2.0 V (I_{oh} = – 2 mA) , V_{ol} = 0.8 V (I_{ol} = 2 mA).

8) $t_{OFF\ (max.)}$ and $t_{OEZ\ (max.)}$ define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.

9) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

10) These parameters are referenced to the CAS leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.

11) t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS\ (min.)}$, the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} > t_{RWD\ (min.)}$, $t_{CWD} > t_{CWD\ (min.)}$, $t_{AWD} > t_{AWD\ (min.)}$ and $t_{CPWD} > t_{CPWD\ (min.)}$, the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.

12) Operation within the $t_{RCD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RCD\ (max.)}$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD\ (max.)}$ limit, then access time is controlled by t_{CAC}.

13) Operation within the $t_{RAD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RAD\ (max.)}$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD\ (max.)}$ limit, then access time is controlled by t_{AA}.

14) AC measurements assume t_T = 5 ns.

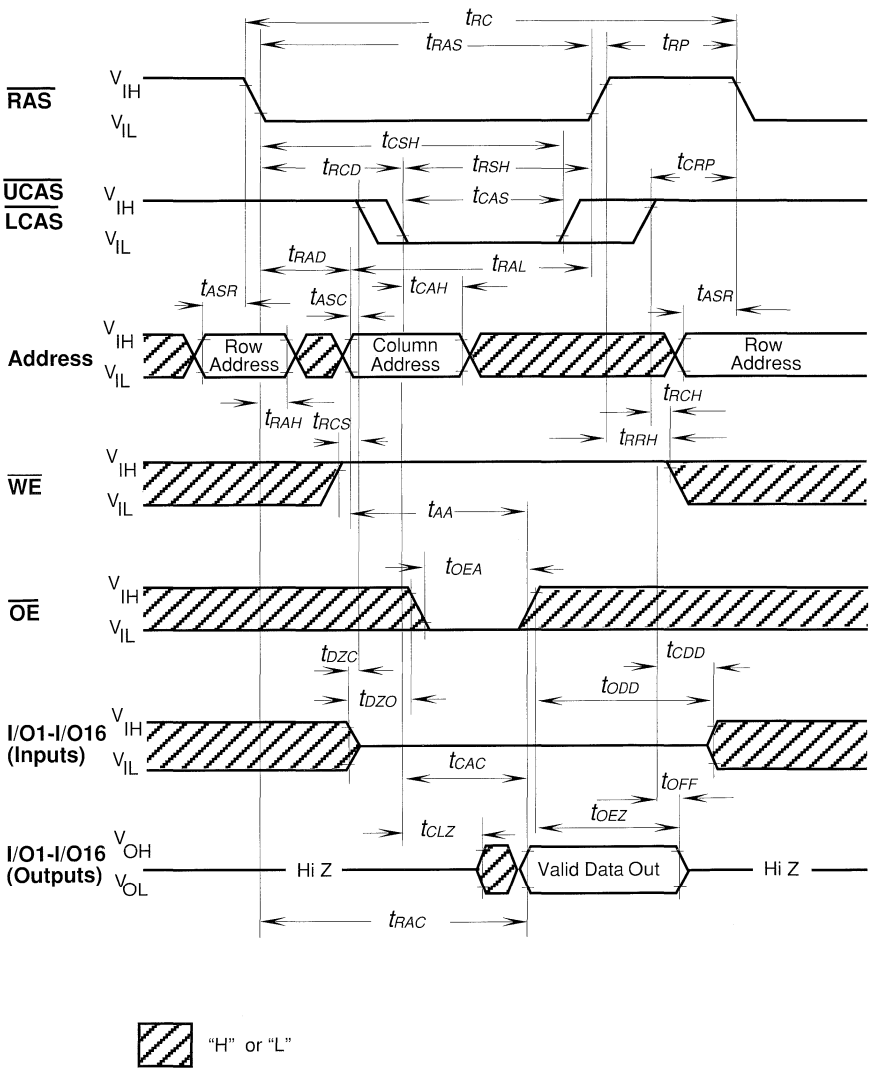
15) Either t_{DZC} or t_{DZO} must be satisfied.

16) Either t_{CDD} or t_{ODD} must be satisfied.

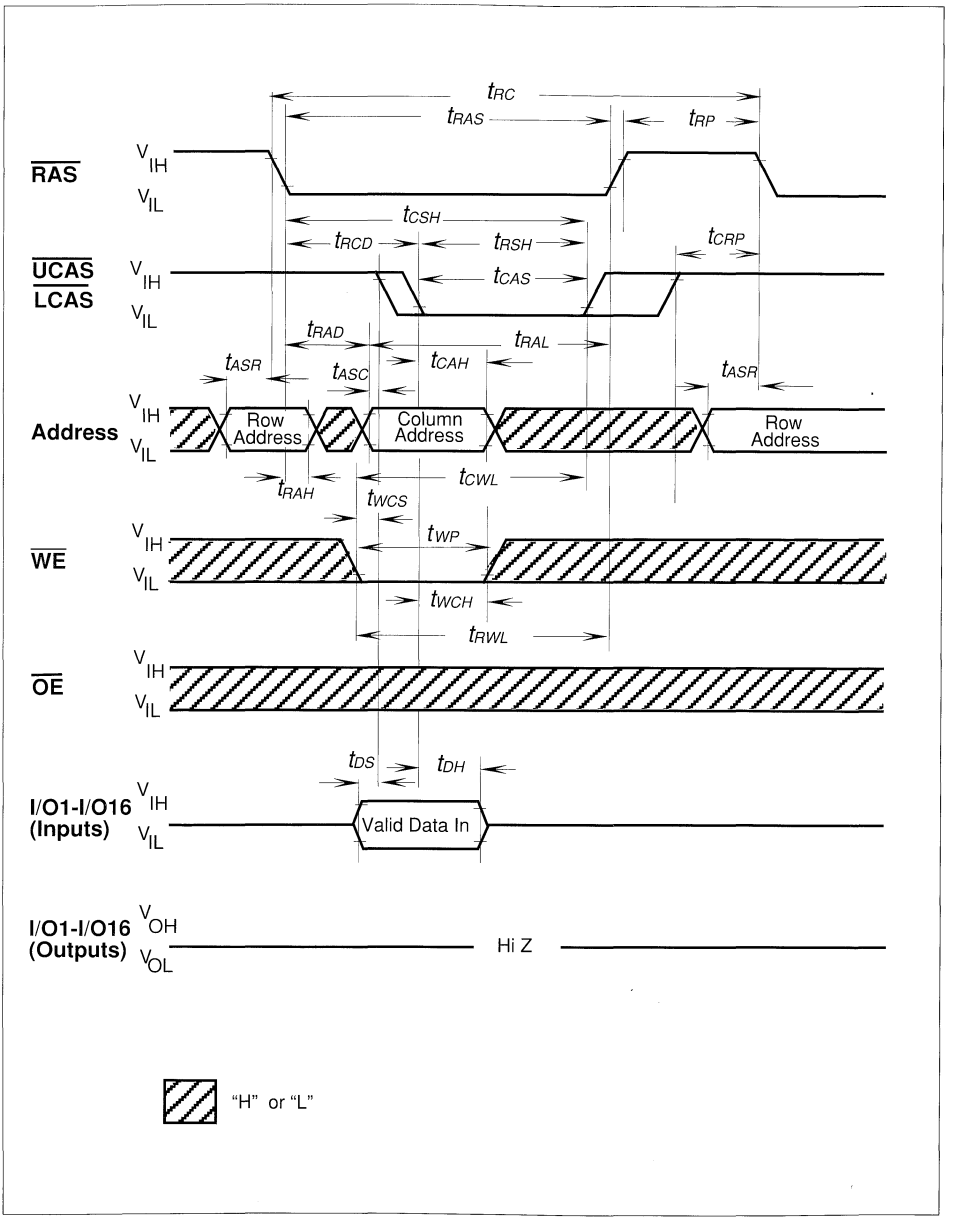
17) When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:

If row addresses are being refreshed on an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh.

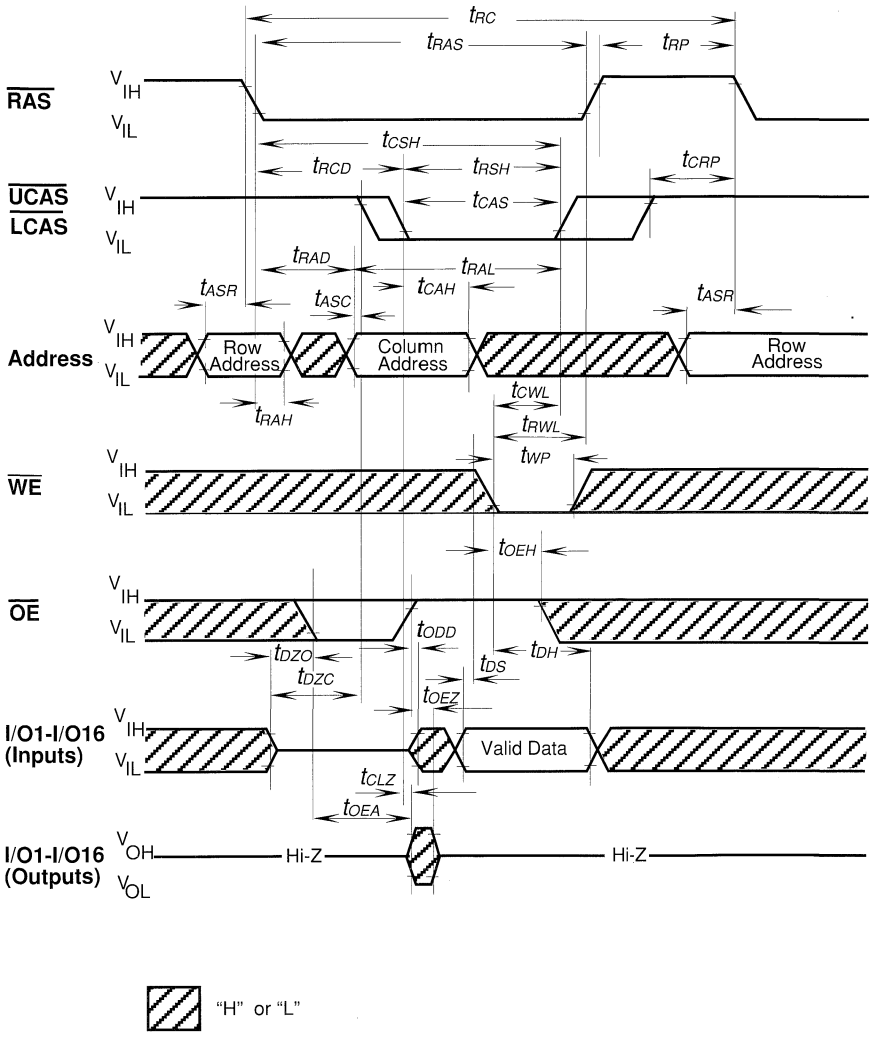
If row addresses are being refreshed in any other manner (ROR - Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh.


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
UCAS
LCAS
tCAS
tRAD
tRAL
tASR
tASC
tCAH
tASR
Address
Row Address
Column Address
Row Address
tRCH
tRAH
tRCS
tRRH
WE
tAA
tOEA
OE
tDZC
tCDD
tDZO
tODD
I/O1-I/O16 (Inputs)
tCAC
tOFF
tOEZ
tCLZ
I/O1-I/O16 (Outputs)
VOH
VOL
Hi Z
Valid Data Out
Hi Z
tRAC
"H" or "L"

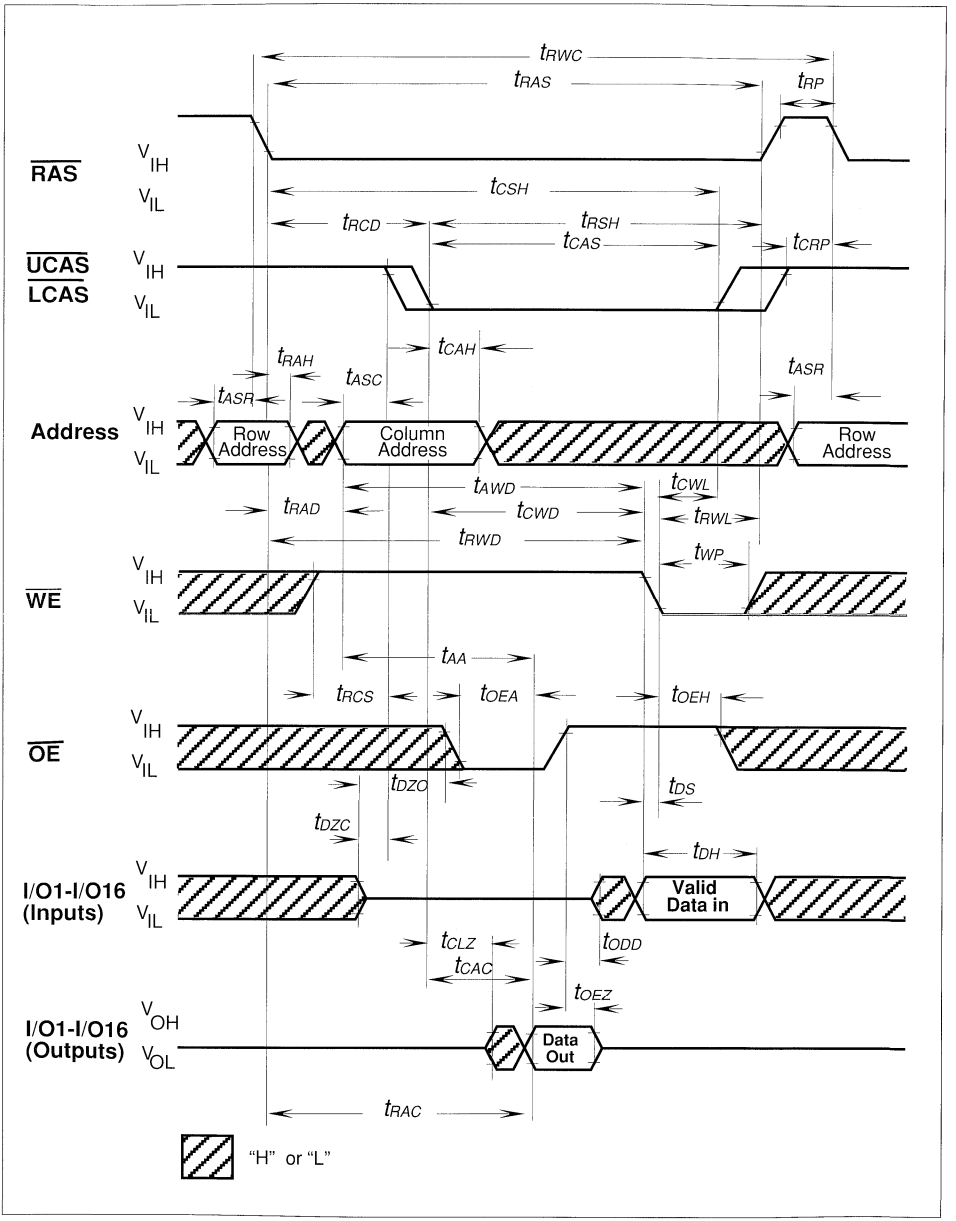
Read Cycle



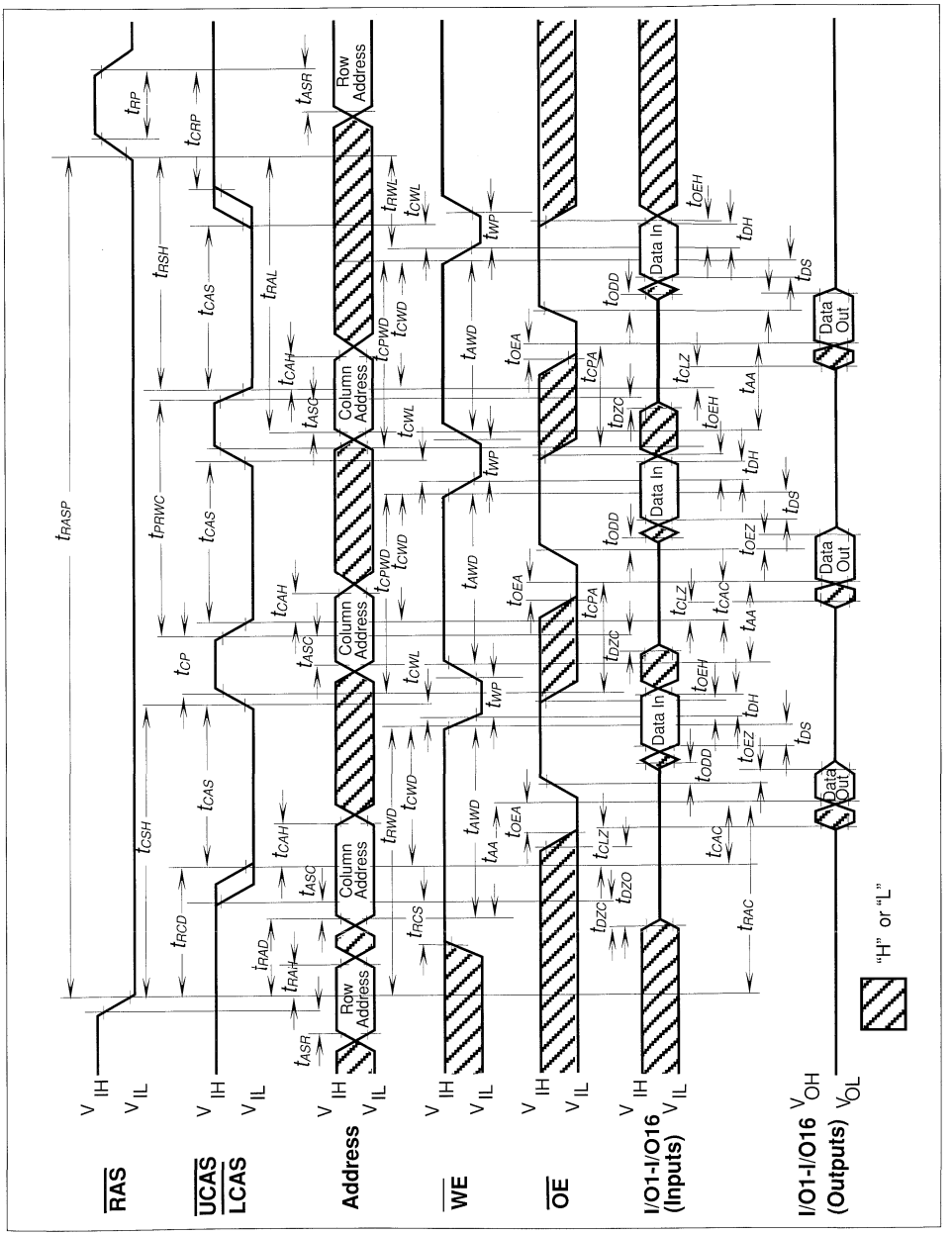
Write Cycle (Early Write)



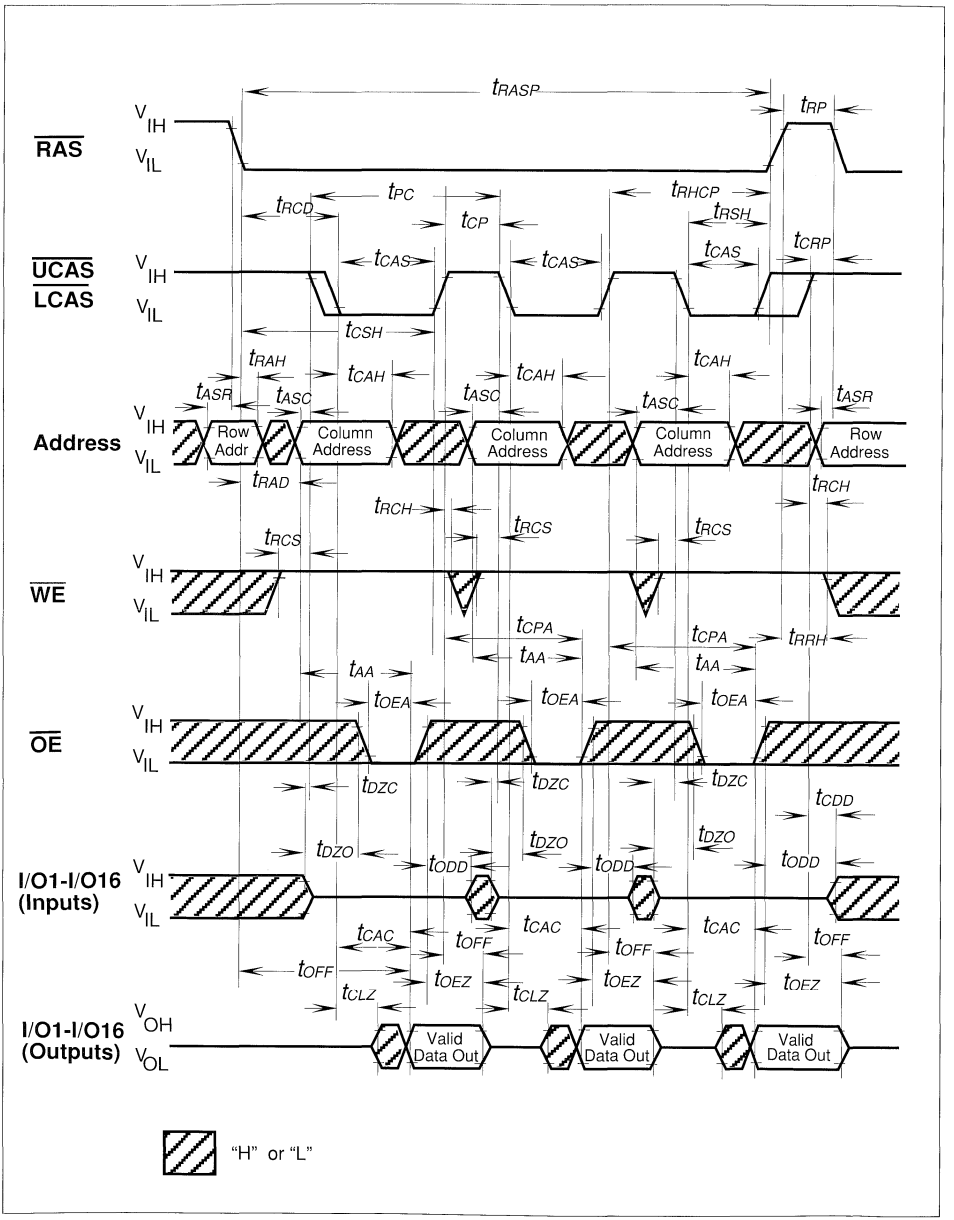
Write Cycle ($\overline{OE}$ Controlled Write)



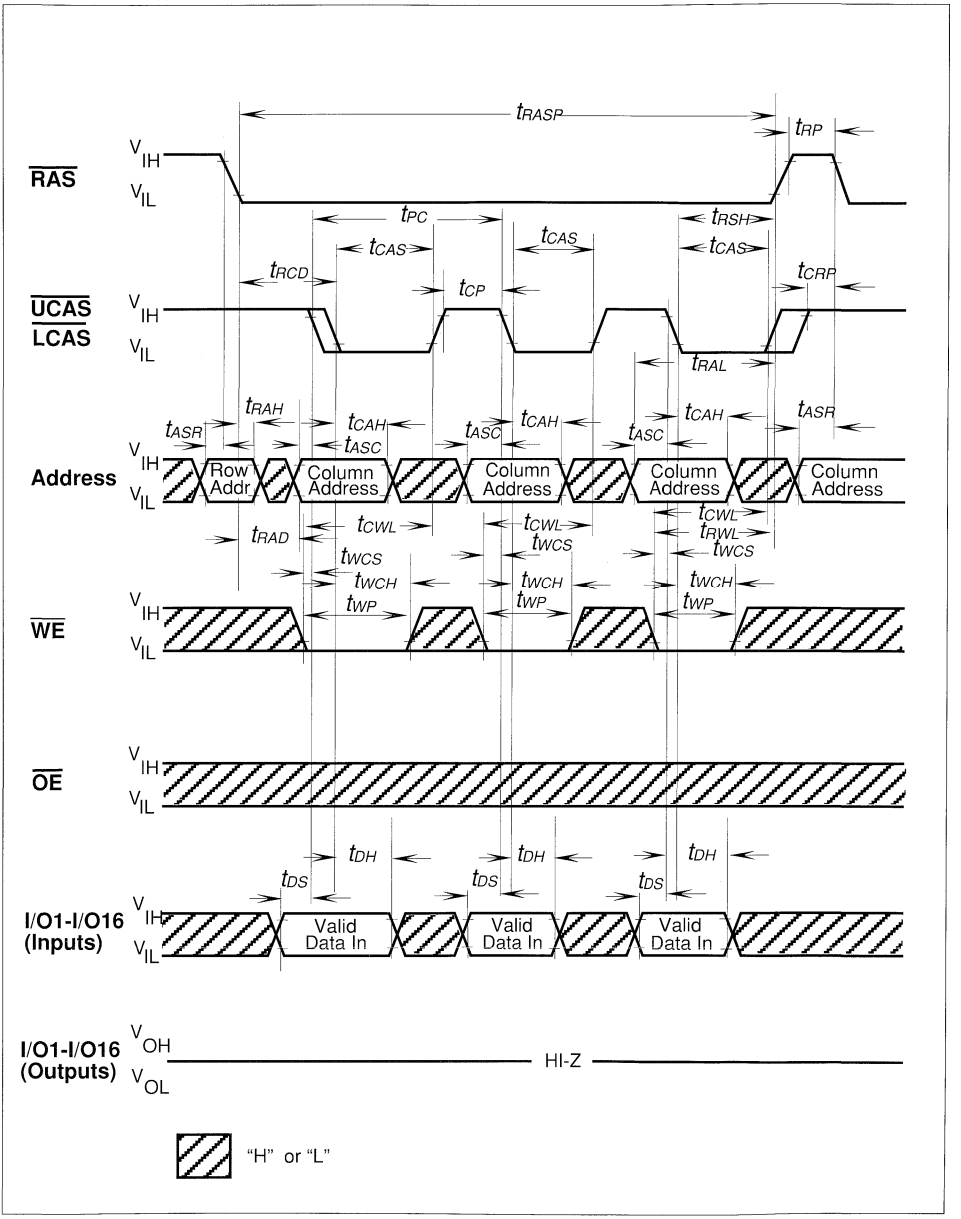
Read-Write (Read-Modify-Write) Cycle



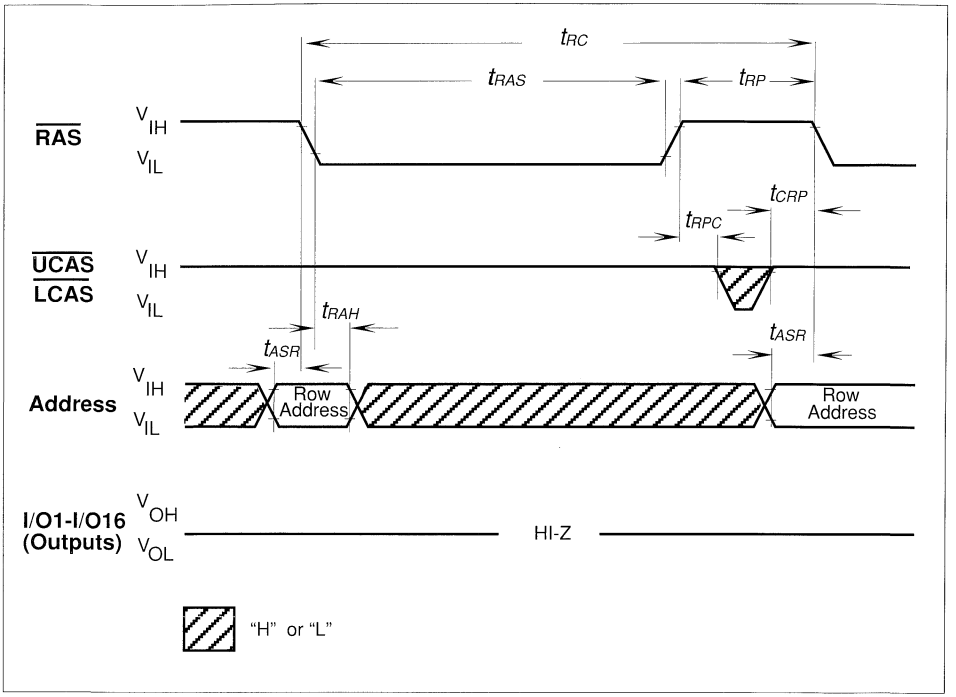
Fast Page Mode Read-Modify-Write Cycle



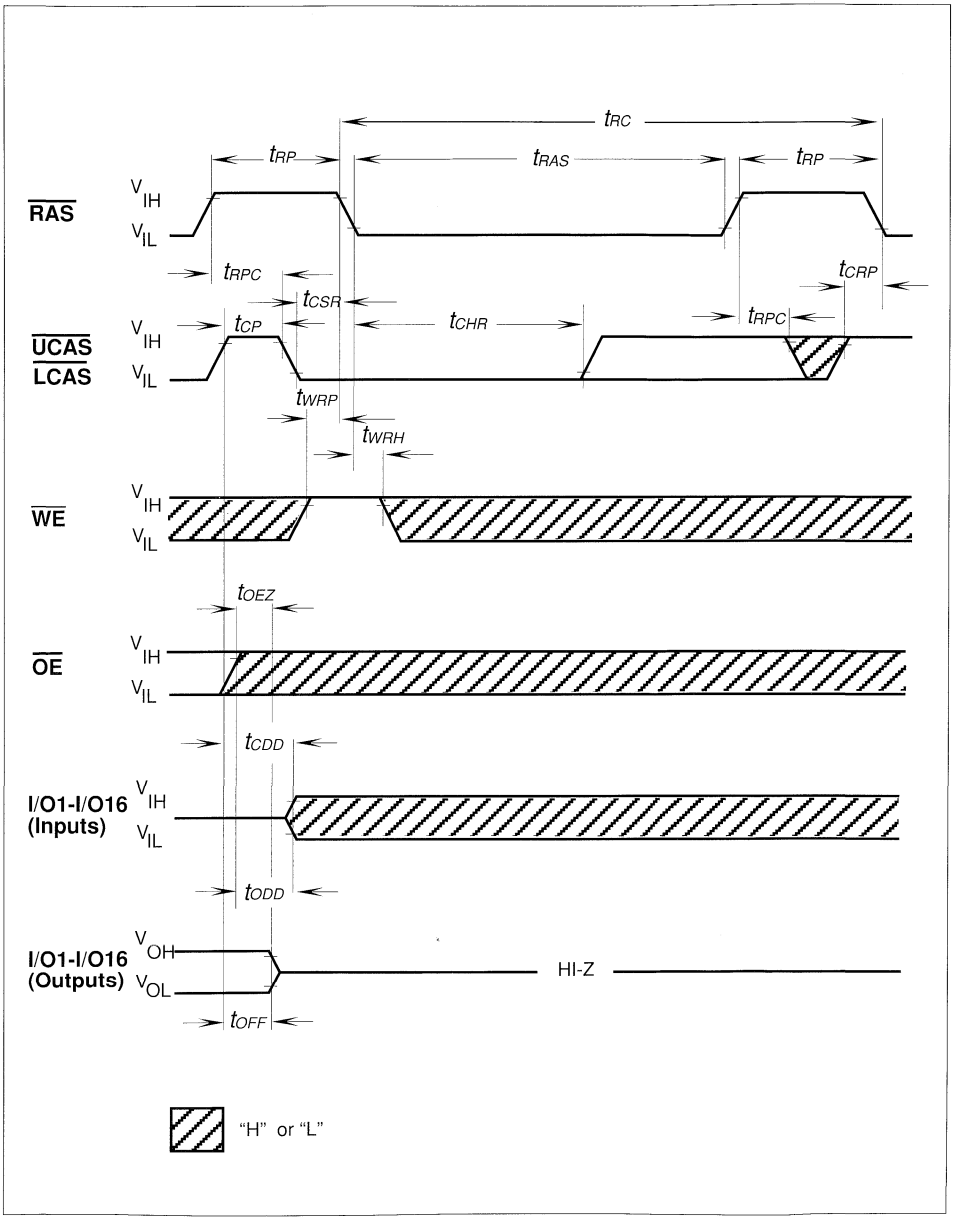
Fast Page Mode Read Cycle



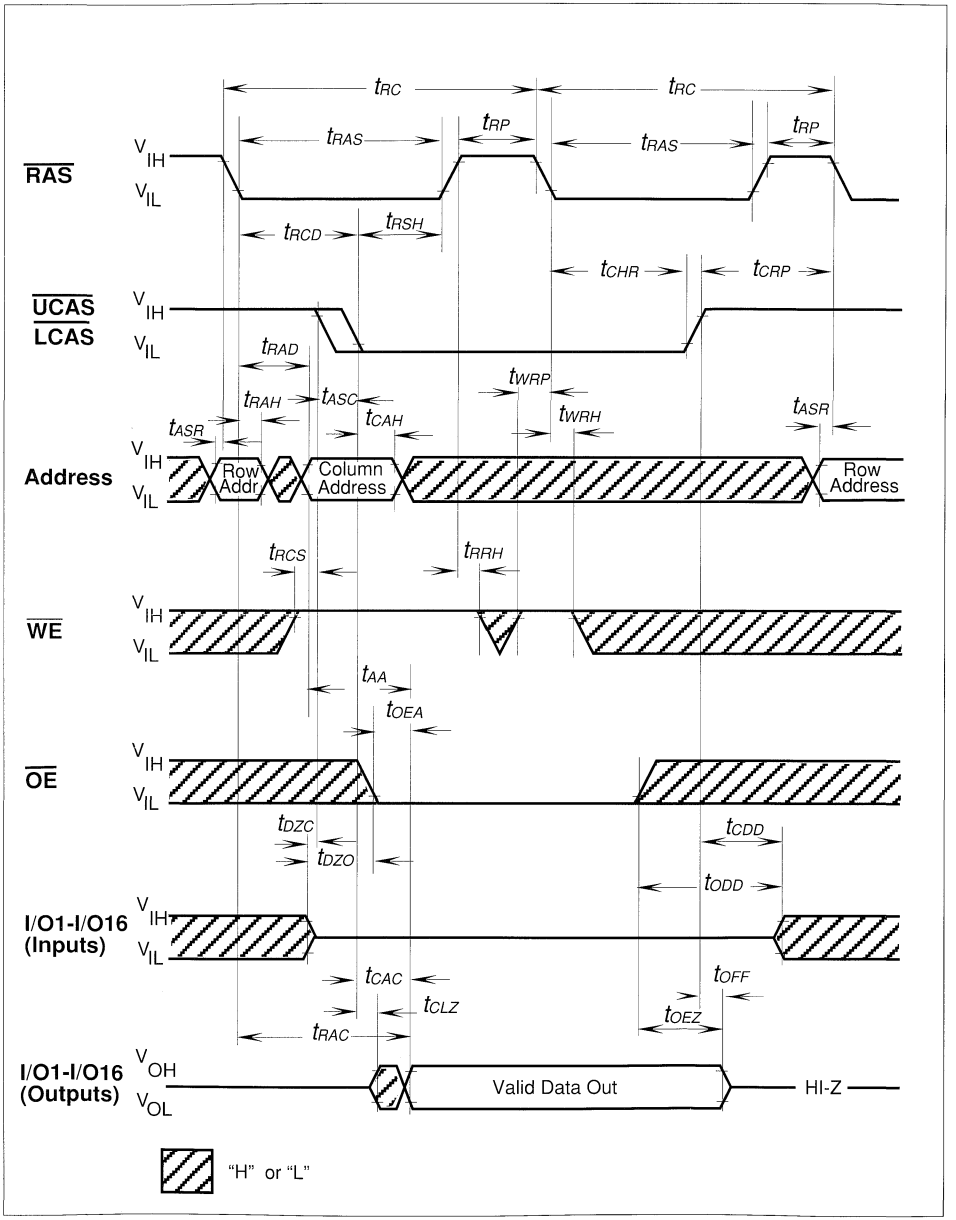
Fast Page Mode Early Write Cycle



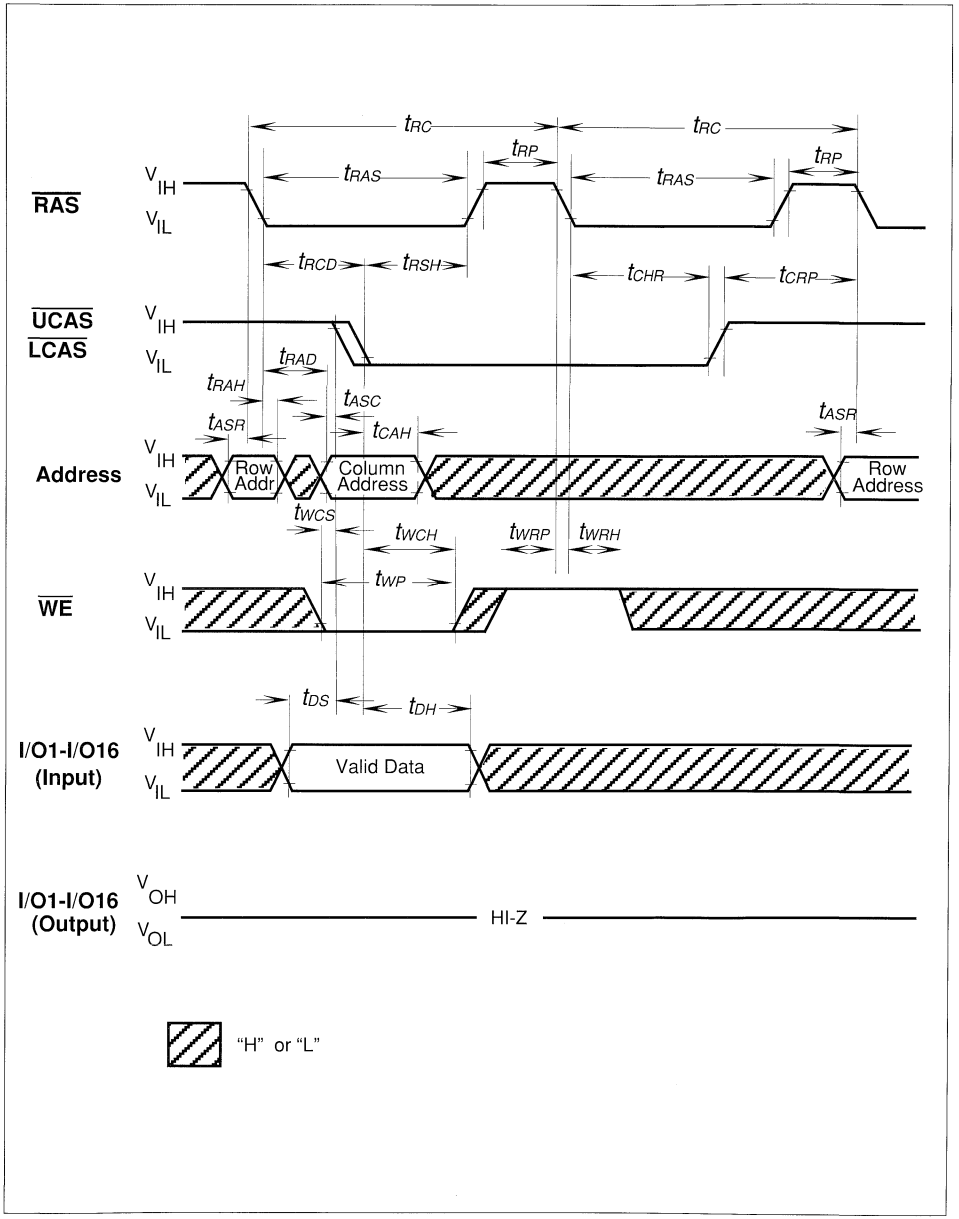
$\overline{RAS}$-Only Refresh Cycle



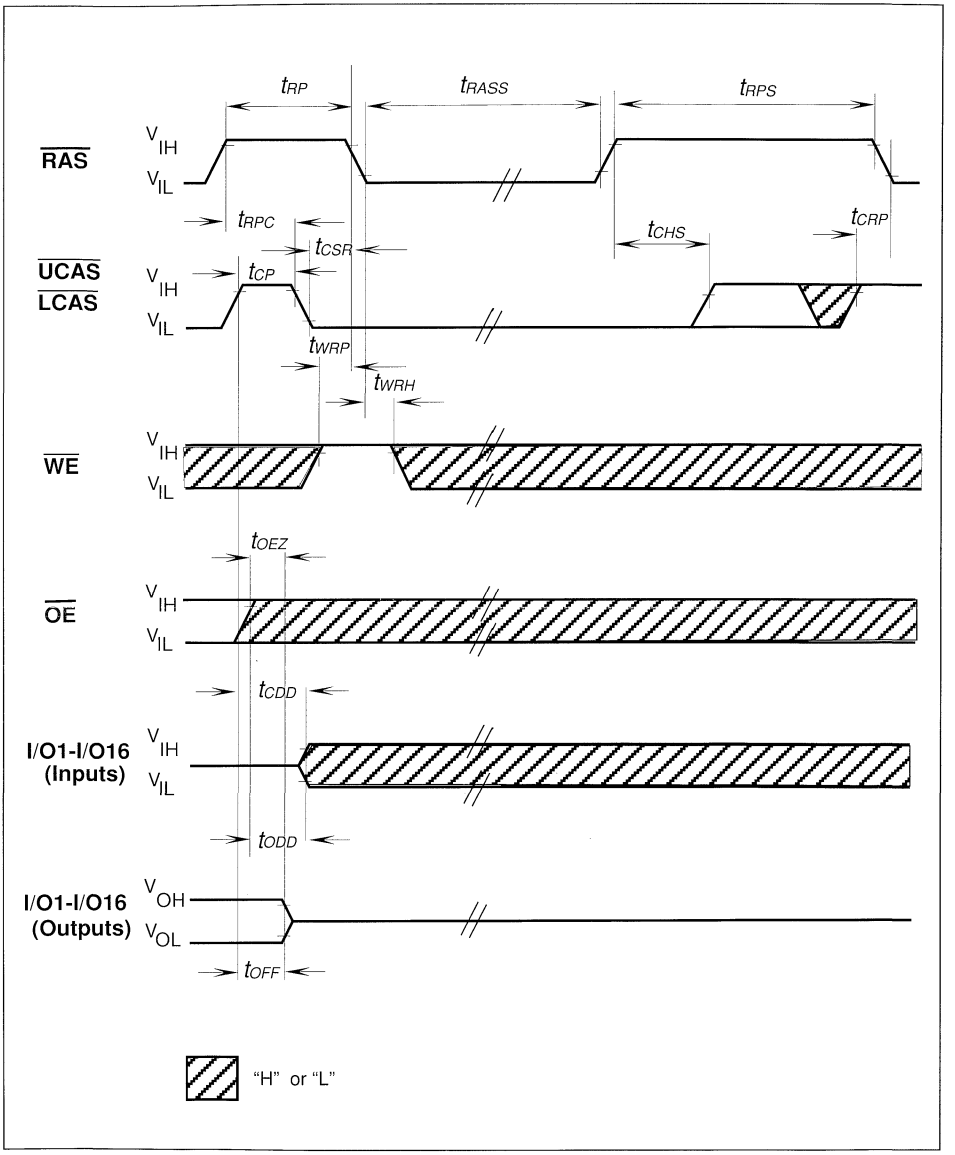
CAS-Before-RAS Refresh Cycle



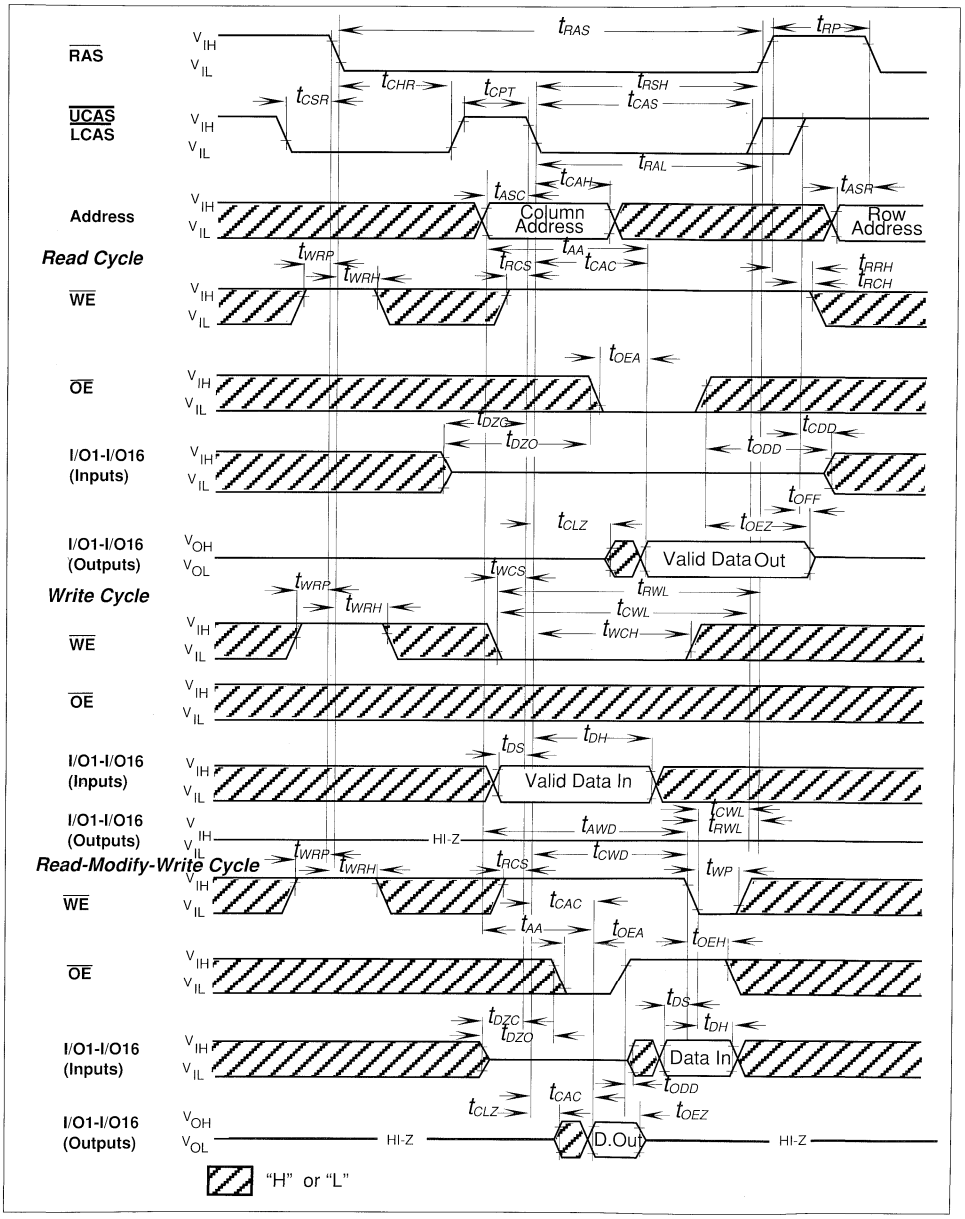
Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Early Write)



Self Refresh



CAS-Before-RAS Refresh Counter Test Cycle

1M x 16-Bit Dynamic RAM
1k & 4k Refresh
(Hyper Page Mode - EDO)

HYB 5116165BSJ -50/-60/-70
HYB 5118165BSJ -50/-60/-70

Preliminary Information

- 1 048 576 words by 16-bit organization
- 0 to 70 °C operating temperature
- Fast access and cycle time
  $\overline{RAS}$ access time:
  50 ns (-50 version)
  60 ns (-60 version)
  70 ns (-70 version)
  Cycle time:
  89 ns (-50 version)
  104 ns (-60 version)
  124 ns (-70 version)
  $\overline{CAS}$ access time:
  12 ns (-50 version)
  15 ns (-60 version)
  20 ns (-70 version)
- Hyper page mode (EDO) cycle time
  20 ns (-50 version)
  25 ns (-60 version)
  30 ns (-70 version)
- Single + 5 V (± 10 %) supply
- Low power dissipation
  max. 990 active mW (HYB3118165BSJ-50)
  max. 935 active mW (HYB3118165BSJ-60)
  max. 880 active mW (HYB3118165BSJ-70)
  max. 550 active mW (HYB3116165BSJ-50)
  max. 495 active mW (HYB3116165BSJ-60)
  max. 440 active mW (HYB3116165BSJ-70)
  11 mW standby (TTL)
  5.5 mW standby (MOS)
- Output unlatched at cycle end allows two-dimensional chip selection
- Read, write, read-modify-write, $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, hidden refresh and Self Refresh
- Hyper page mode (EDO) capability
- All inputs, outputs and clocks fully TTL-compatible
- 1024 refresh cycles / 16 ms
  for HYB5118165BSJ (1k-Refresh)
- 4096 refresh cycles / 64 ms
  for HYB5116165BSJ (4k-Refresh)
- Plastic Package: P-SOJ-42-1 400 mil

Ordering Information

Type	Ordering Code	Package	Descriptions
HYB 5116165BJ-50	on request	P-SOJ-42-1 400 mil	DRAM (access time 50 ns)
HYB 5116165BJ-60	on request	P-SOJ-42-1 400 mil	DRAM (access time 60 ns)
HYB 5116165BJ-70	on request	P-SOJ-42-1 400 mill	DRAM (access time 70 ns)
HYB 5118165BJ-50	Q67100-Q1107	P-SOJ-42-1 400 mil	DRAM (access time 50 ns)
HYB 5118165BJ-60	Q67100-Q1108	P-SOJ-42-1 400 mil	DRAM (access time 60 ns)
HYB 5118165BJ-70	Q67100-Q1109	P-SOJ-42-1 400 mil	DRAM (access time 70 ns)

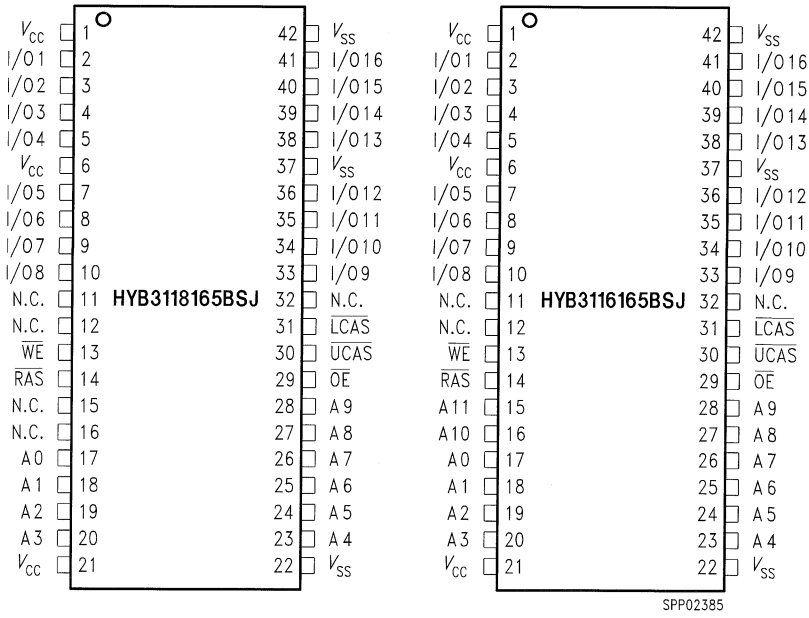
The HYB 5116(8)165BSJ is the new generation dynamic RAM organized as 1 048 576 words by 16-bits. The HYB 5116(8)165BSJ utilizes a submicron CMOS silicon gate process technology, as well as advanced circuit techniques to provide wide operating margins, both internally and for the system user. Multiplexed address inputs permit the HYB 5116(8)165BSJ to be packaged in a standard SOJ 42 plastic package with 400 mil width. These packages provide high system bit densities and are compatible with commonly used automatic testing and insertion equipment. System-oriented features include single + 5 V (± 10 %) power supply, direct interfacing with high-performance logic device families such as Schottky TTL.

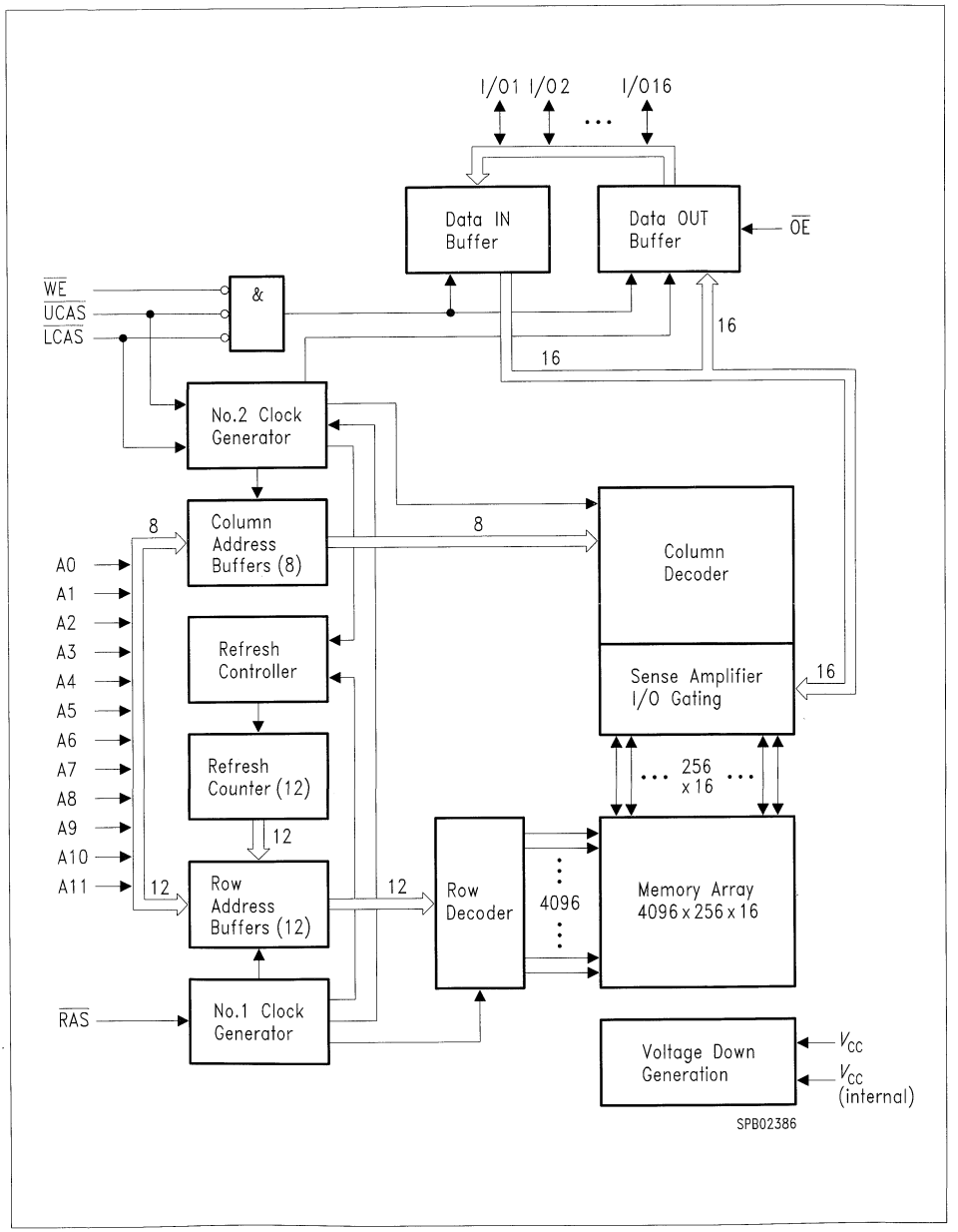
Pin Definitions and Functions

Pin No.	Function
A0-A9	Row Address Inputs for HYB5118165BSJ
A0-A9	Column Address Inputs for HYB5118165BSJ
A0-A11	Row Address Inputs for HYB5116165BSJ
A0 to A7	Column Address Inputs for HYB5116165BSJ
$\overline{RAS}$	Row Address Strobe
$\overline{OE}$	Output Enable
I/O1-I/O16	Data Input/Output
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground (0 V)
N.C.	not connected

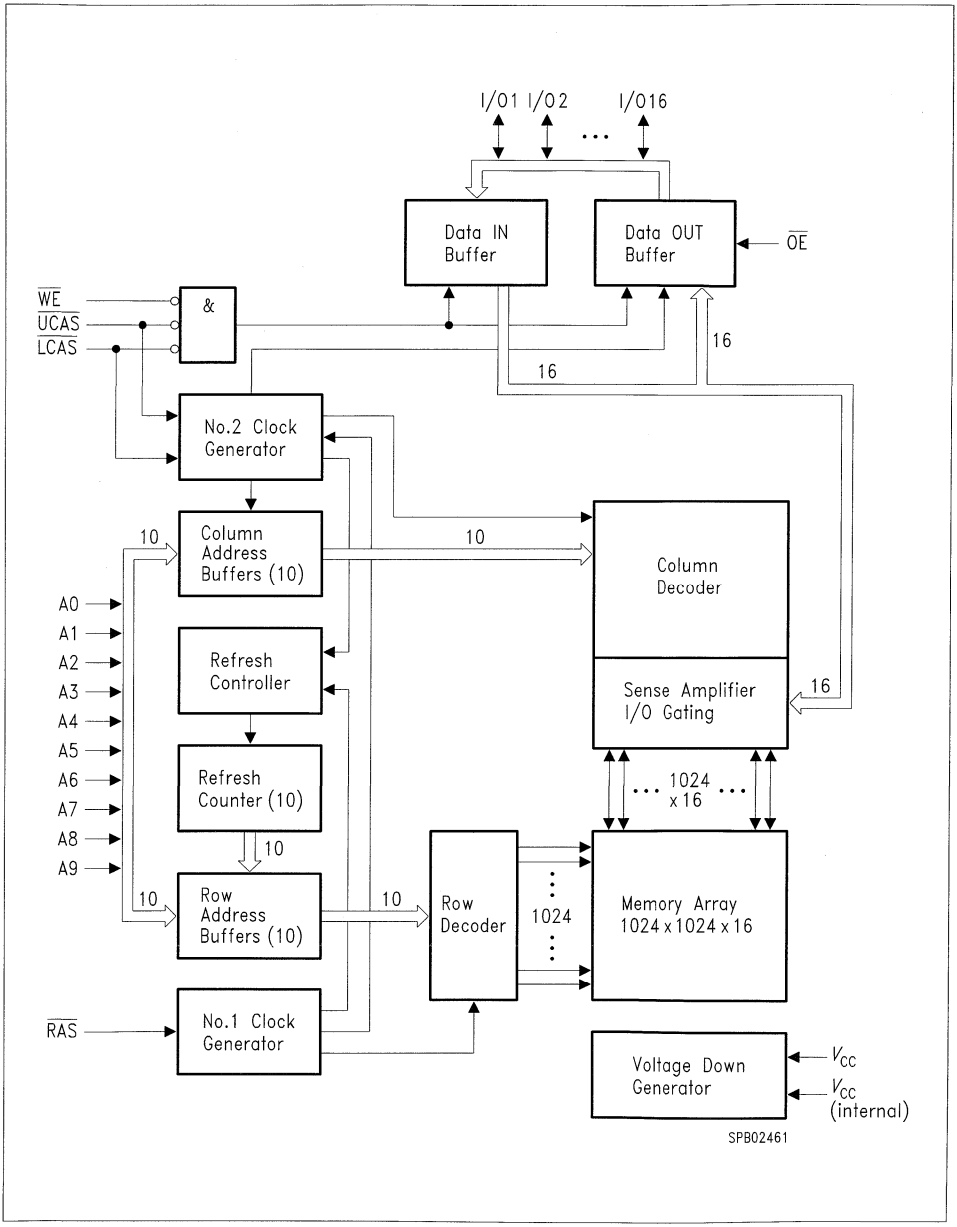
Pin Configuration
(top view)

P-SOJ-42-1 (400 mil)





Block Diagram for HYB 5116165BSJ



Block Diagram for HYB 5118165BSJ

Absolute Maximum Ratings

Operating temperature range ..... 0 to 70 °C
Storage temperature range ..... – 55 to 150 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 0.5 to min (V_{CC} + 0.5, 7.0) V
Power supply voltage ..... – 1.0 V to 7.0 V
Power dissipation ..... 1.0 W
Data out current (short circuit) ..... 50 mA

Note:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics (note : values in brackets for HYB5118165BSJ)
T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 5 V ± 10 %; t_T = 2 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	V_{CC} + 0.5	V	1)
Input low voltage	V_{IL}	– 0.5	0.8	V	1)
Output high voltage (I_{OUT} = – 5 mA)	V_{OH}	2.4	–	V	1)
Output low voltage (I_{OUT} = 4.2 mA)	V_{OL}	–	0.4	V	1)
Input leakage current (0 V ≤ V_{IH} ≤ V_{CC} + 0.3 V, all other pins = 0 V)	$I_{I(L)}$	– 10	10	µA	1)
Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ V_{CC} + 0.3 V)	$I_{O(L)}$	– 10	10	µA	1)
Average V_{CC} supply current:	I_{CC1}				
-50 ns version		–	100(200)	mA	2) 3) 4)
-60 ns version		–	90 (180)	mA	2) 3) 4)
-70 ns version		–	80 (160)	mA	2) 3) 4)
($\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = t_{RC} min.)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	2	mA	–
Average V_{CC} supply current, during $\overline{RAS}$-only refresh cycles:	I_{CC3}				
-50 ns version		–	100(200)	mA	2) 4)
-60 ns version		–	90 (180)	mA	2) 4)
-70 ns version		–	80 (160)	mA	2) 4)
($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)					

DC Characteristics (note : values in brackets for HYB5118165BSJ) (cont'd)
T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 5 V ± 10 %; t_T = 2 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current, during hyper page mode: -50 ns version -60 ns version -70 ns version ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling: t_{PC} = t_{PC} min.)	I_{CC4}	– – –	85 (90) 75 (80) 65 (70)	mA mA mA	2) 3) 4) 2) 3) 4) 2) 3) 4)
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	–	1	mA	1)
Average V_{CC} supply current, during $\overline{CAS}$-before-RAS refresh mode: -50 ns version -60 ns version -70 ns version ($\overline{RAS}$, $\overline{CAS}$ cycling: t_{RC} = t_{RC} min.)	I_{CC6}	– – –	100(200) 90 (180) 80 (160)	mA mA mA	2) 4) 2) 4) 2) 4)
Average Self Refresh Current (CBR cycle with t_{RAS} > t_{RASS}min., $\overline{CAS}$ held low, $\overline{WE}$ = V_{CC} – 0.2 V, Address and Din = V_{CC} – 0.2 V or 0.2 V)	I_{CC7}	–	1	mA	

AC Characteristics [5)7)]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 2 ns

Parameter	Symbol	Limit Values						Unit
		HYB 5116(8)165 BSJ-50		HYB 5116(8)165 BSJ-60		HYB 5116(8)165 BSJ-70		
		min.	max.	min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	89	–	104	–	124	–	ns
Read-write cycle time	t_{RWC}	117	–	138	–	162	–	ns
Hyper page mode (EDO) cycle time	t_{HPC}	20	–	25	–	30	–	ns
Hyper page mode (EDO) read-write cycle time	t_{PRWC}	57	–	68	–	77	–	ns
Access time from $\overline{RAS}$ [7) 12)]	t_{RAC}	–	50	–	60	–	70	ns
Access time from $\overline{CAS}$ [7) 12)]	t_{CAC}	–	12	–	15	–	17	ns
Access time from column address [7) 13)]	t_{AA}	–	25	–	30	–	35	ns
Access time from $\overline{CAS}$ precharge [7)]	t_{CPA}	–	27	–	32	–	37	ns
$\overline{CAS}$ to output in low-Z [7)]	t_{CLZ}	0	–	0	–	0	–	ns
Output buffer turn-off delay [8) 18)]	t_{OFF}	0	15	0	15	0	20	ns
Transition time (rise and fall) [6)]	t_T	1	50	1	50	1	50	ns
$\overline{RAS}$ precharge time	t_{RP}	35	–	40	–	50	–	ns
$\overline{RAS}$ pulse width	t_{RAS}	50	10k	60	10k	70	10k	ns
$\overline{RAS}$ pulse width (Hyper page mode- EDO)	t_{RASP}	50	200k	60	200k	70	200k	ns
$\overline{CAS}$ pulse width	t_{CAS}	7	10k	10	10k	12	10k	ns
$\overline{CAS}$ precharge to $\overline{RAS}$ Delay (Hyper Page Mode)	t_{RHCP}	27	–	32	–	37	–	ns
$\overline{CAS}$ precharge to $\overline{WE}$ (HPM RMW)	t_{CPWD}	41	–	49	–	56	–	ns
$\overline{RAS}$ hold time	t_{RSH}	12		15	–	17	–	ns
$\overline{CAS}$ hold time	t_{CSH}	50		60	–	70	–	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time [12)]	t_{RCD}	12	38	14	45	14	53	

AC Characteristics (cont'd) [5)7)]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 2 ns

Parameter	Symbol	Limit Values						Unit
		HYB 5116(8)165 BSJ-50		HYB 5116(8)165 BSJ-60		HYB 5116(8)165 BSJ-70		
		min.	max.	min.	max.	min.	max.	
$\overline{RAS}$ to column address delay time [13)]	t_{RAD}	10	25	12	30	12	35	ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	5	–	ns
$\overline{CAS}$ precharge time	t_{CP}	9	–	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns
Row address hold time	t_{RAH}	8	–	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns
Column address hold time	t_{CAH}	5	–	7	–	10	–	ns
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	–	30	–	35	–	ns
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns
Read command hold time [9)]	t_{RCH}	0	–	0	–	0	–	ns
Read command hold time referenced to $\overline{RAS}$ [9)]	t_{RRH}	0	–	0	–	0	–	ns
Write command hold time	t_{WCH}	5	–	7	–	10	–	ns
Write command pulse width	t_{WP}	5	–	7	–	10	–	ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	12	–	15	–	17	–	ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	12	–	15	–	17	–	ns
Data setup time [10)]	t_{DS}	0	–	0	–	0	–	ns
Data hold time [10)]	t_{DH}	5	–	7	–	10	–	ns
Refresh period for HYB5116165	t_{REF}	–	64	–	64	–	64	ms
Refresh period for HYB5118165	t_{REF}	–	16	–	16	–	16	ms
Write command setup time [11)]	t_{WCS}	0	–	0	–	0	–	ns
$\overline{CAS}$ to $\overline{WE}$ delay time [11)]	t_{CWD}	26	–	32	–	36	–	ns
$\overline{RAS}$ to WE delay time [11)]	t_{RWD}	64	–	77	–	89	–	ns

AC Characteristics (cont'd) [5)7)]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 2 ns

Parameter	Symbol	Limit Values						Unit
		HYB 5116(8)165 BSJ-50		HYB 5116(8)165 BSJ-60		HYB 5116(8)165 BSJ-70		
		min.	max.	min.	max.	min.	max.	
Column address to $\overline{WE}$ delay time [11)]	t_{AWD}	39	–	47	–	54	–	ns
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CSR}	10	–	10	–	10	–	ns
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CHR}	10	–	10	–	10	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5	–	5	–	5	–	ns
$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ counter test cycle)	t_{CPT}	35	–	40	–	40	–	ns
Write to $\overline{RAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{WRP}	10	–	10	–	10	–	ns
Write hold time referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{WRH}	10	–	10	–	10	–	ns
Output data hold time	t_{COH}	5	–	5	–	5	–	ns
$\overline{OE}$ command hold time	t_{OEH}	12	–	15	–	17	–	ns
$\overline{OE}$ access time	t_{OEA}	–	12	–	15	–	17	ns
Output buffer turn-off delay from $\overline{OE}$	t_{OEZ}	0	12	0	15	0	17	ns
Data to $\overline{CAS}$ low delay [15)]	t_{DZC}	0	–	0	–	0	–	ns
Data to $\overline{OE}$ low delay [15)]	t_{DZO}	0	–	0	–	0	–	ns
$\overline{CAS}$ high to data delay [16)]	t_{CDD}	12	–	15	–	17	–	ns
$\overline{OE}$ high to data delay [16)]	t_{ODD}	12	–	15	–	17	–	ns
$\overline{RAS}$ pulse width during self refresh	t_{RASS}	100k	_	100k	_	100k	_	ns
$\overline{RAS}$ precharge time during self refresh	t_{RPS}	95	_	110	_	130	_	ns
$\overline{CAS}$ hold time during self refresh	t_{CHS}	-50	_	-50	_	-50	_	ns

Capacitance

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A11)	C_{I1}	–	5	pF
Input capacitance ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}	–	7	pF
I/O capacitance (I/O1-I/O16)	C_{IO}	–	7	pF

Notes:

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.

4) Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4} it can be changed once or less during a hyper page mode cycle (t_{HPC}).

5) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6) $V_{IH\ (min.)}$ and $V_{IL\ (max.)}$ are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.

7) Measured with a load equivalent to 2 TTL gates and 50 pF (V_{ol} = 0.8V and V_{oh} = 2.0V).

8) $t_{OFF\ (max.)}$ and $t_{OEZ\ (max.)}$ define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.

9) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

10) These parameters are referenced to the CAS leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.

11) t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS\ (min.)}$, the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} > t_{RWD\ (min.)}$, $t_{CWD} > t_{CWD\ (min.)}$, $t_{AWD} > t_{AWD\ (min.)}$ and $t_{CPWD} > t_{CPWD\ (min.)}$, the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.

12) Operation within the $t_{RCD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RCD\ (max.)}$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD\ (max.)}$ limit, then access time is controlled by t_{CAC}.

13) Operation within the $t_{RAD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RAD\ (max.)}$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD\ (max.)}$ limit, then access time is controlled by t_{AA}.

14) AC measurements assume t_T = 2 ns.

15) Either t_{DZC} or t_{DZO} must be satisfied.

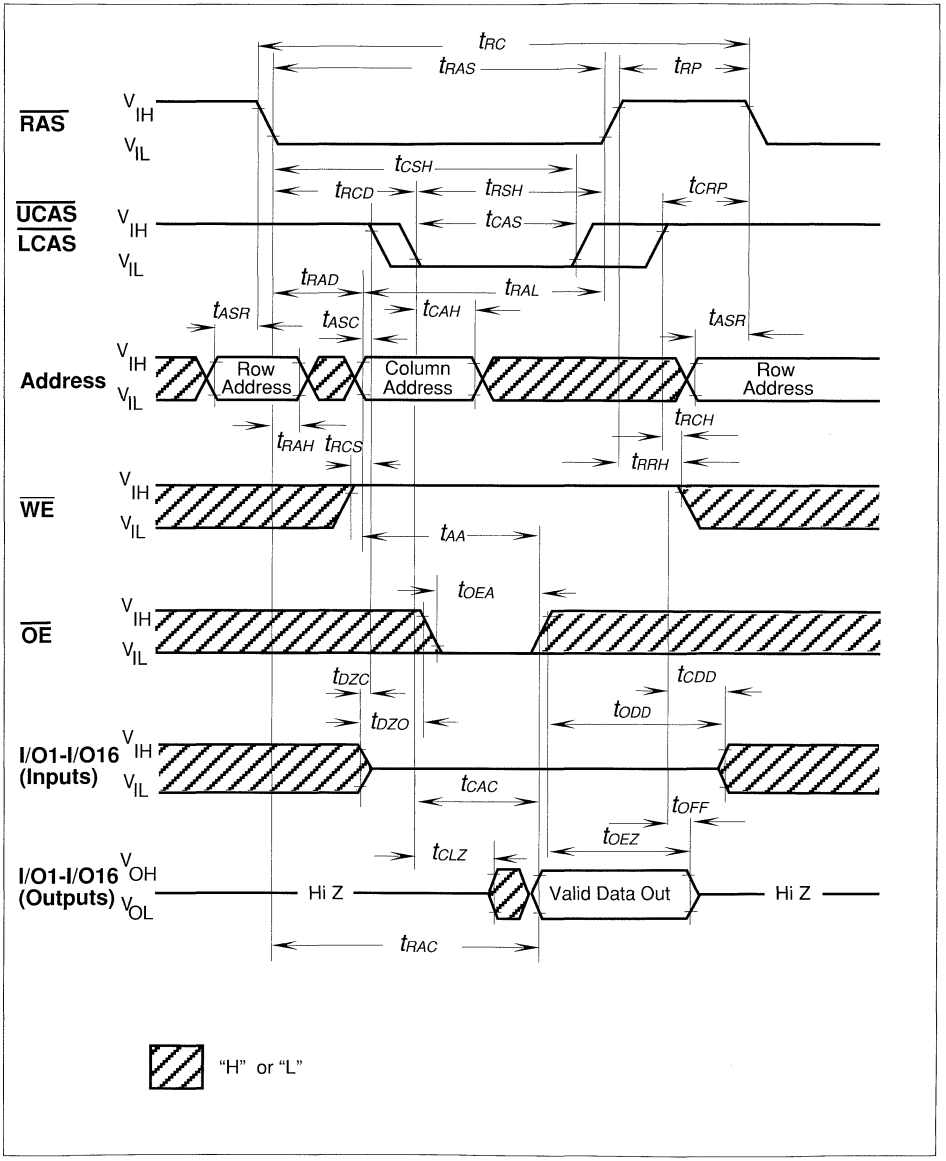
16)Either t_{CDD} or t_{ODD} must be satisfied.

17)When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:

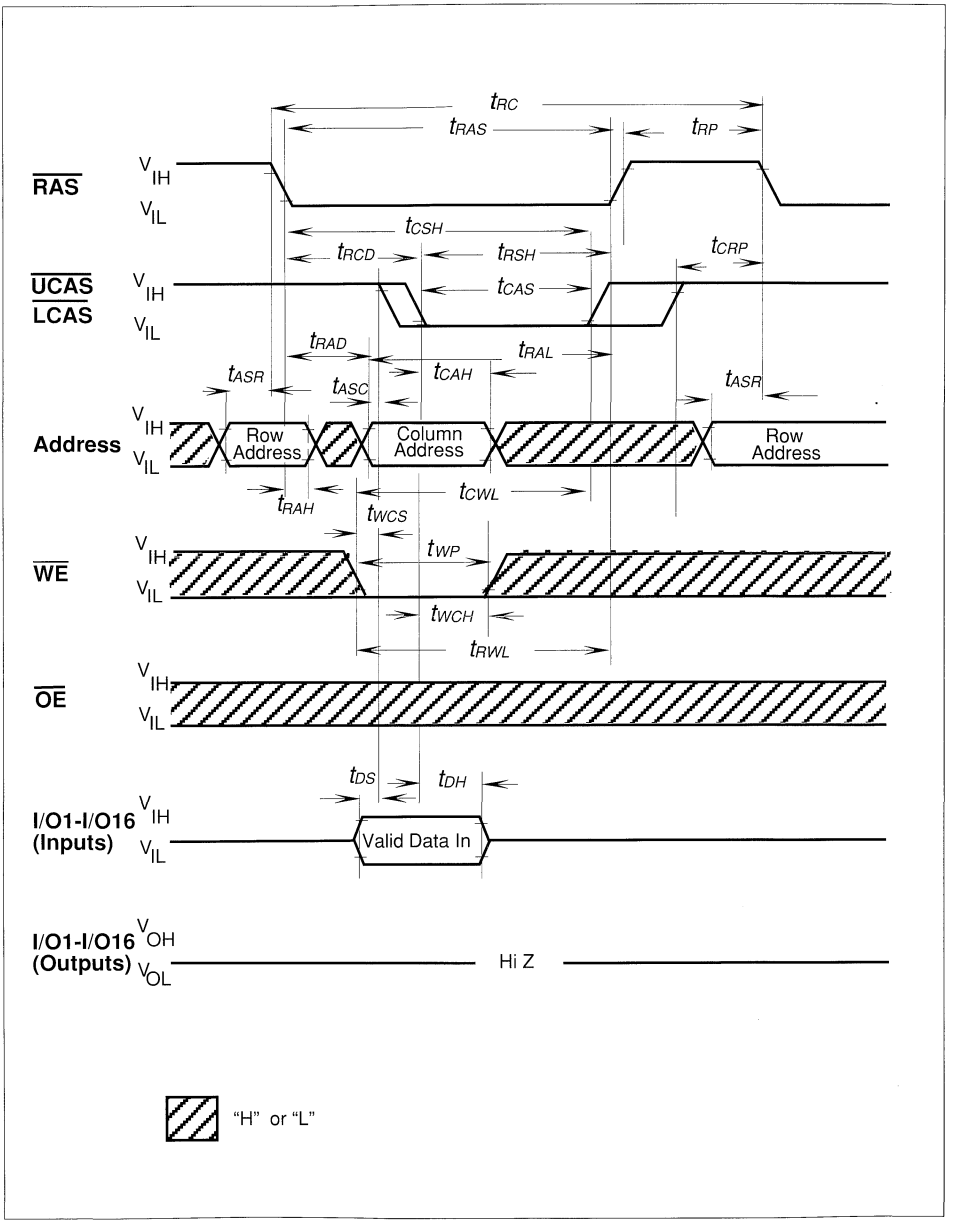
If row addresses are being refreshed on an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh.

If row addresses are being refreshed in any other manner (ROR - Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh

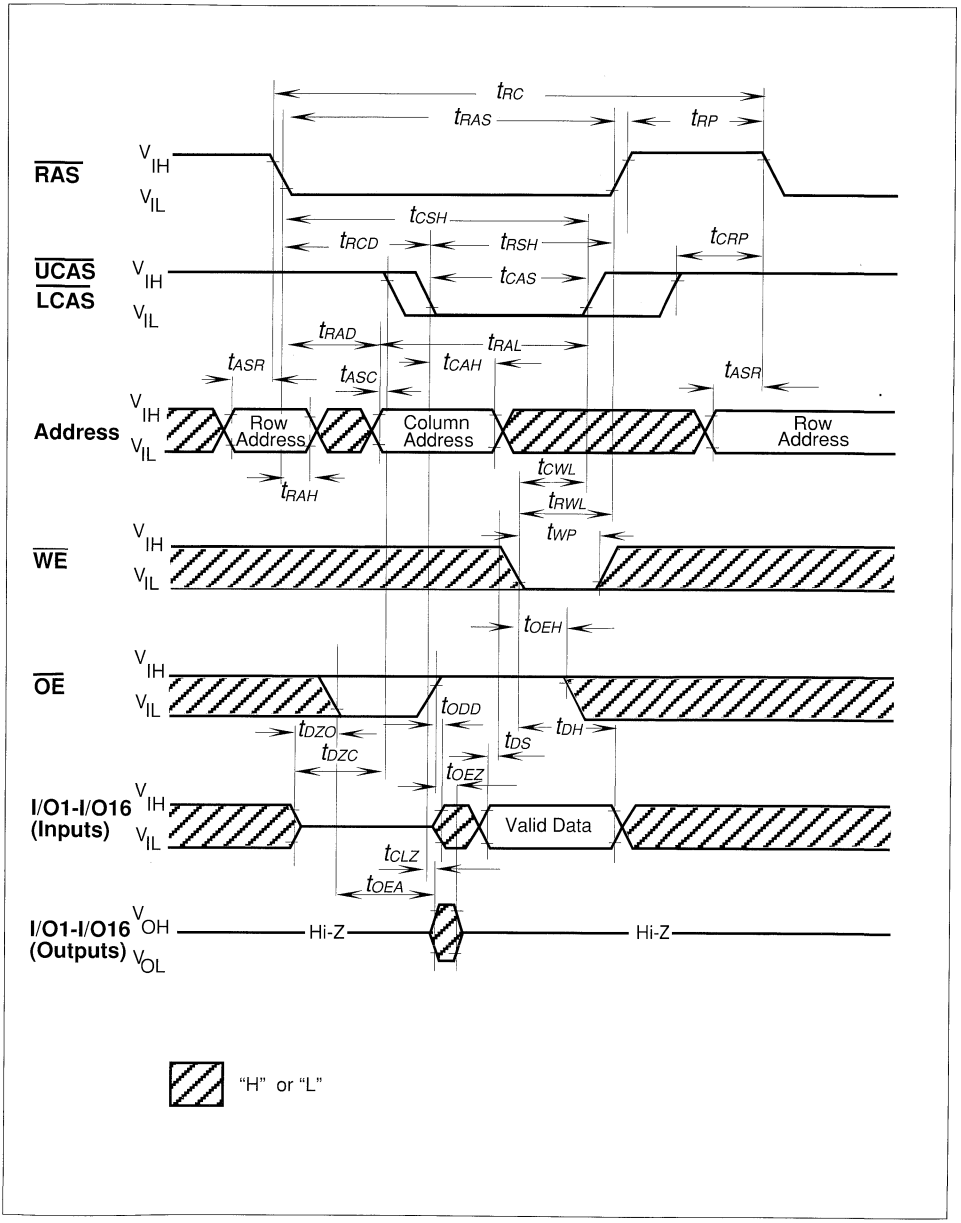
18)t_{off} is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
UCAS
LCAS
tCAS
tRAD
tRAL
tASR
tASC
tCAH
tASR
Address
Row Address
Column Address
Row Address
tRCH
tRAH
tRCS
tRRH
WE
tAA
tOEA
OE
tDZC
tCDD
tDZO
tODD
I/O1-I/O16 (Inputs)
tCAC
tOFF
tOEZ
tCLZ
I/O1-I/O16 (Outputs)
VOH
VOL
Hi Z
Valid Data Out
Hi Z
tRAC
"H" or "L"

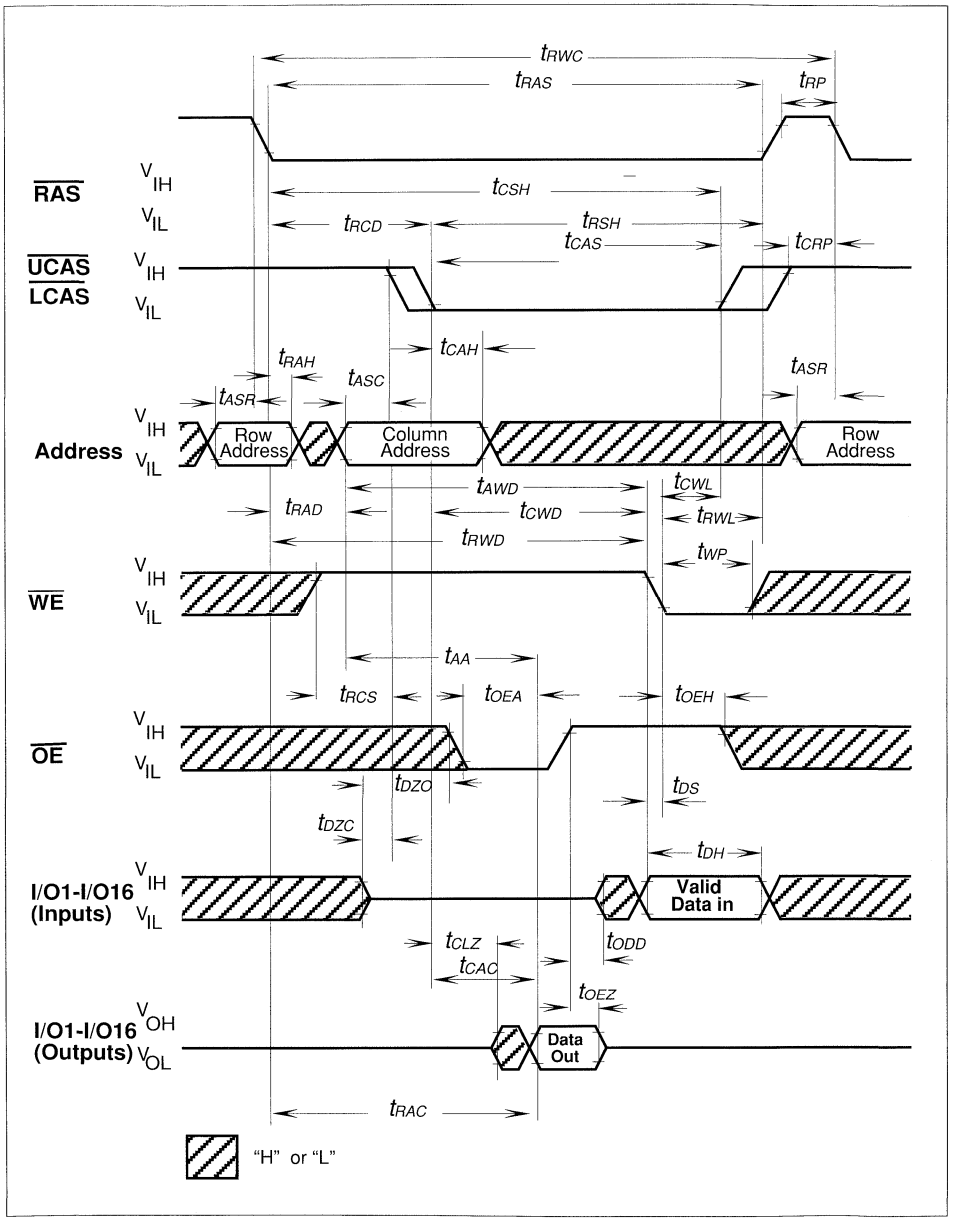
Read Cycle



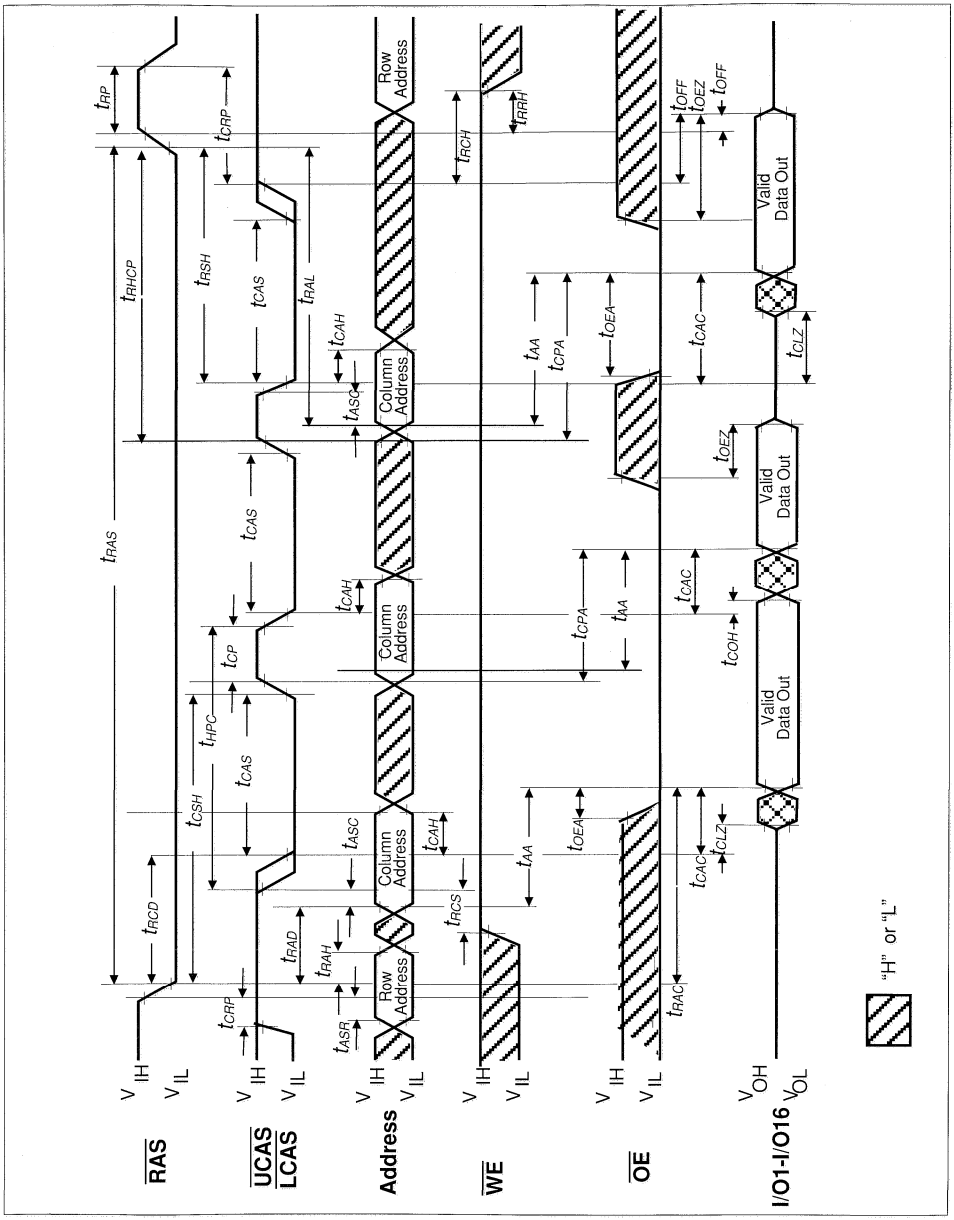
Write Cycle (Early Write)



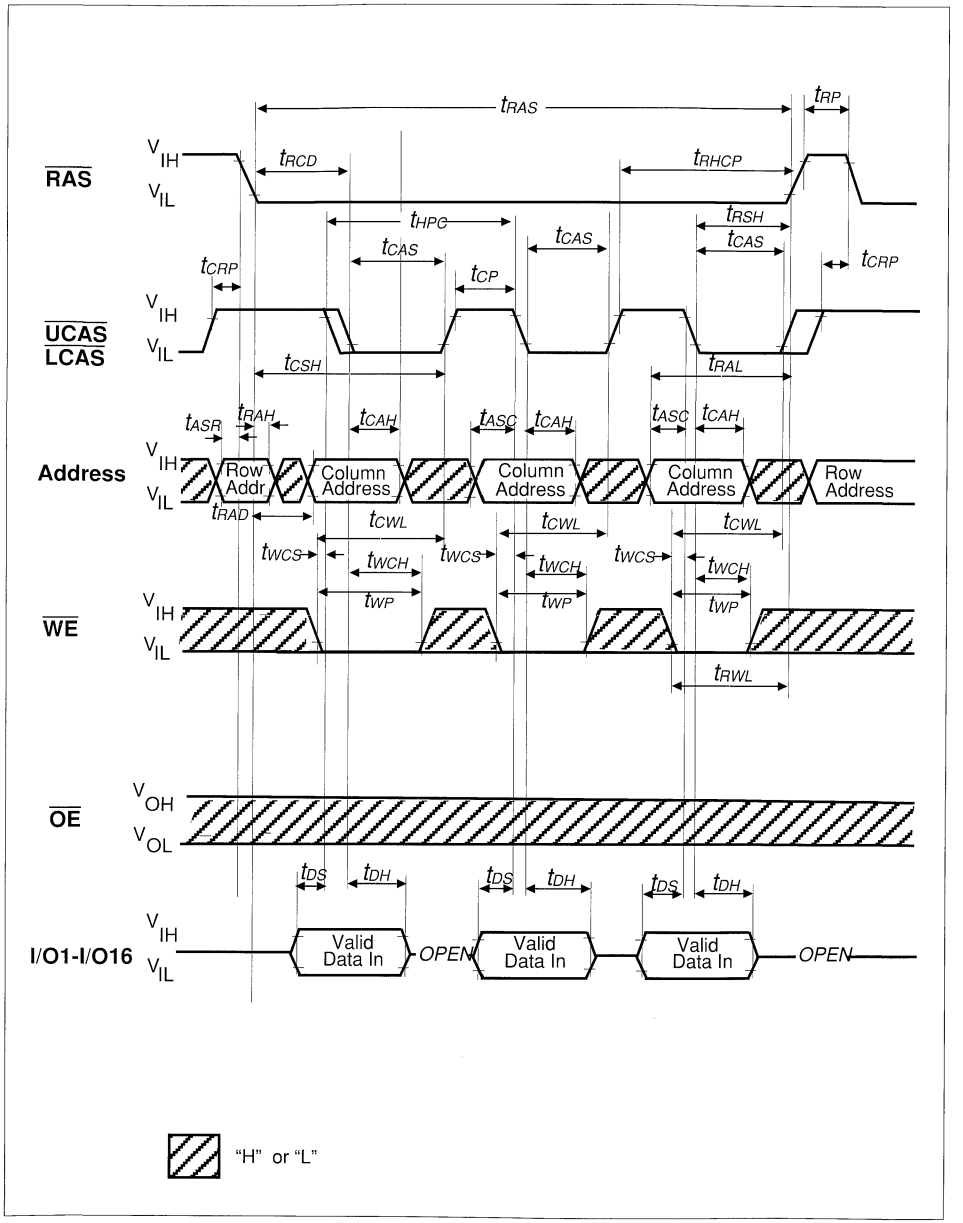
Write Cycle ($\overline{OE}$ Controlled Write)



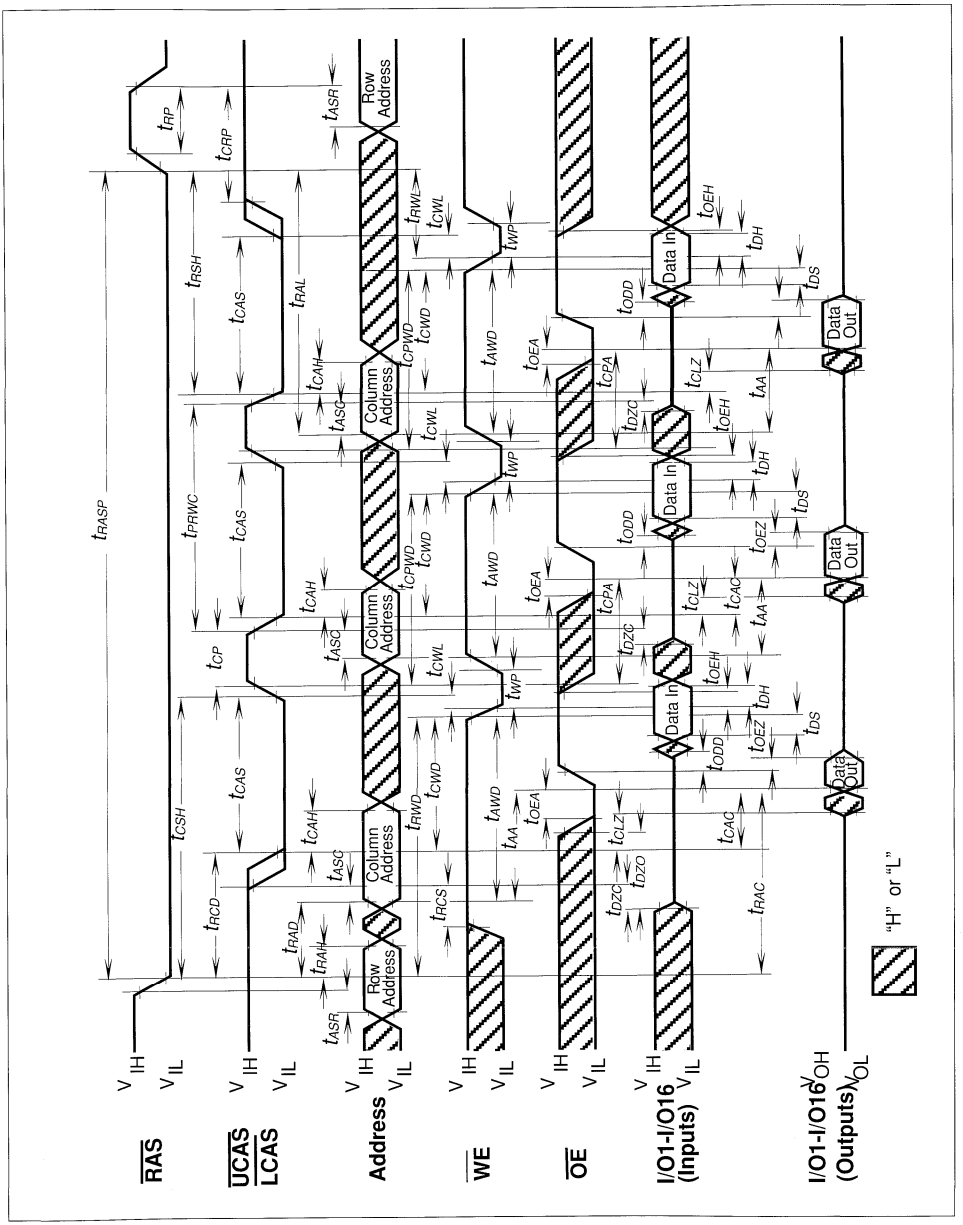
Read-Write (Read-Modify-Write) Cycle



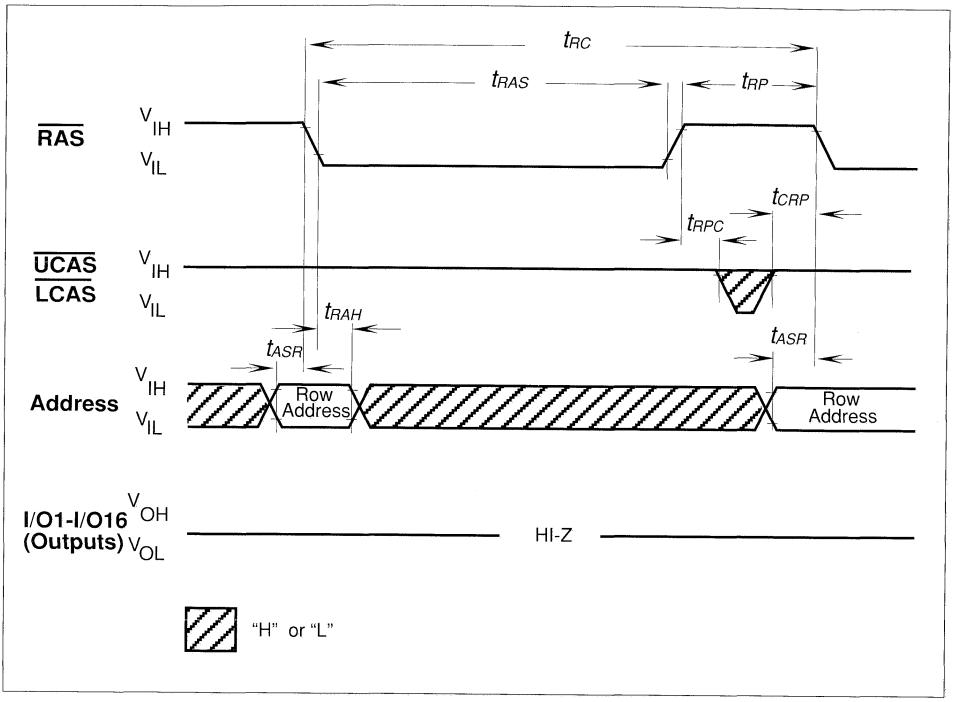
Hyper Page Mode (EDO) Read Cycle



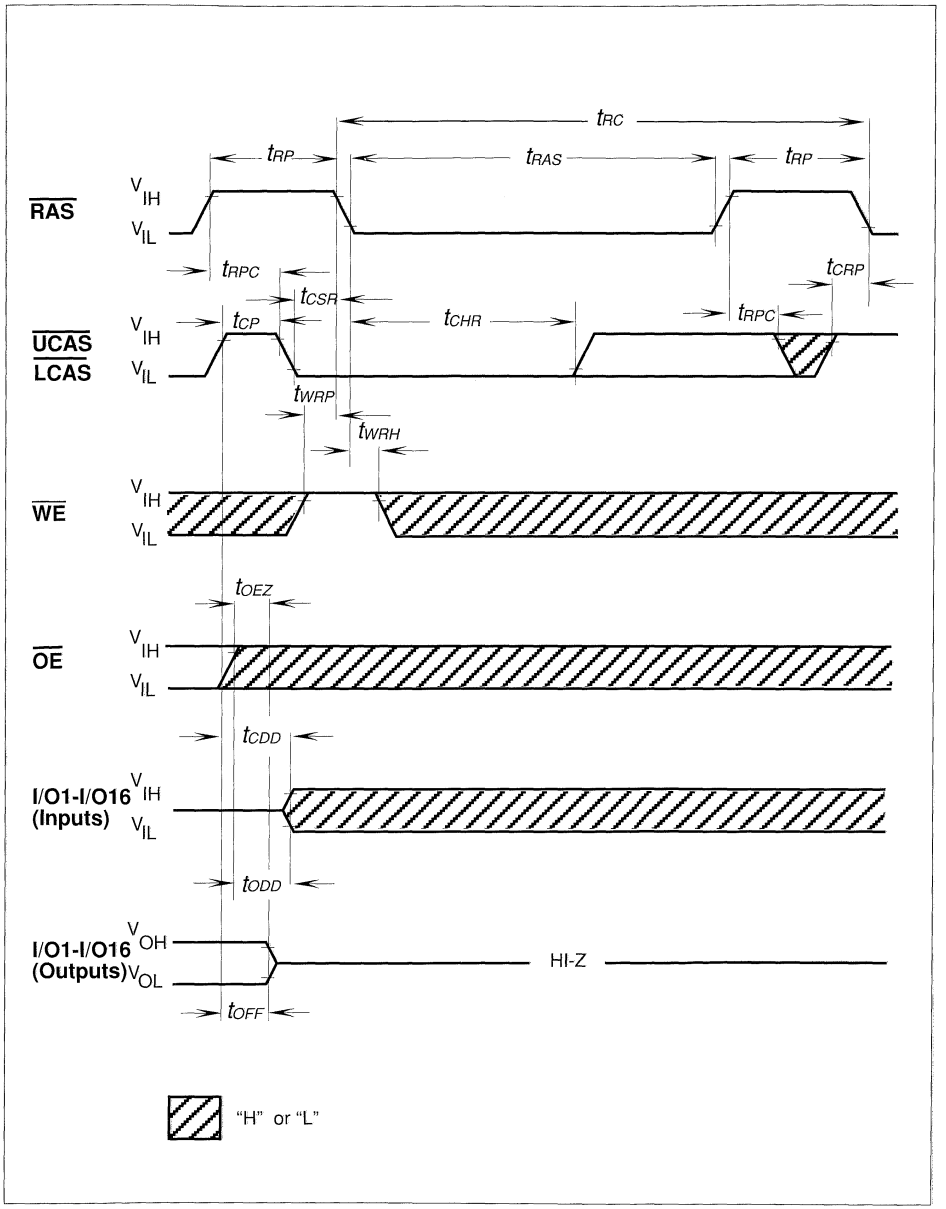
Hyper Page Mode (EDO) Write Cycle



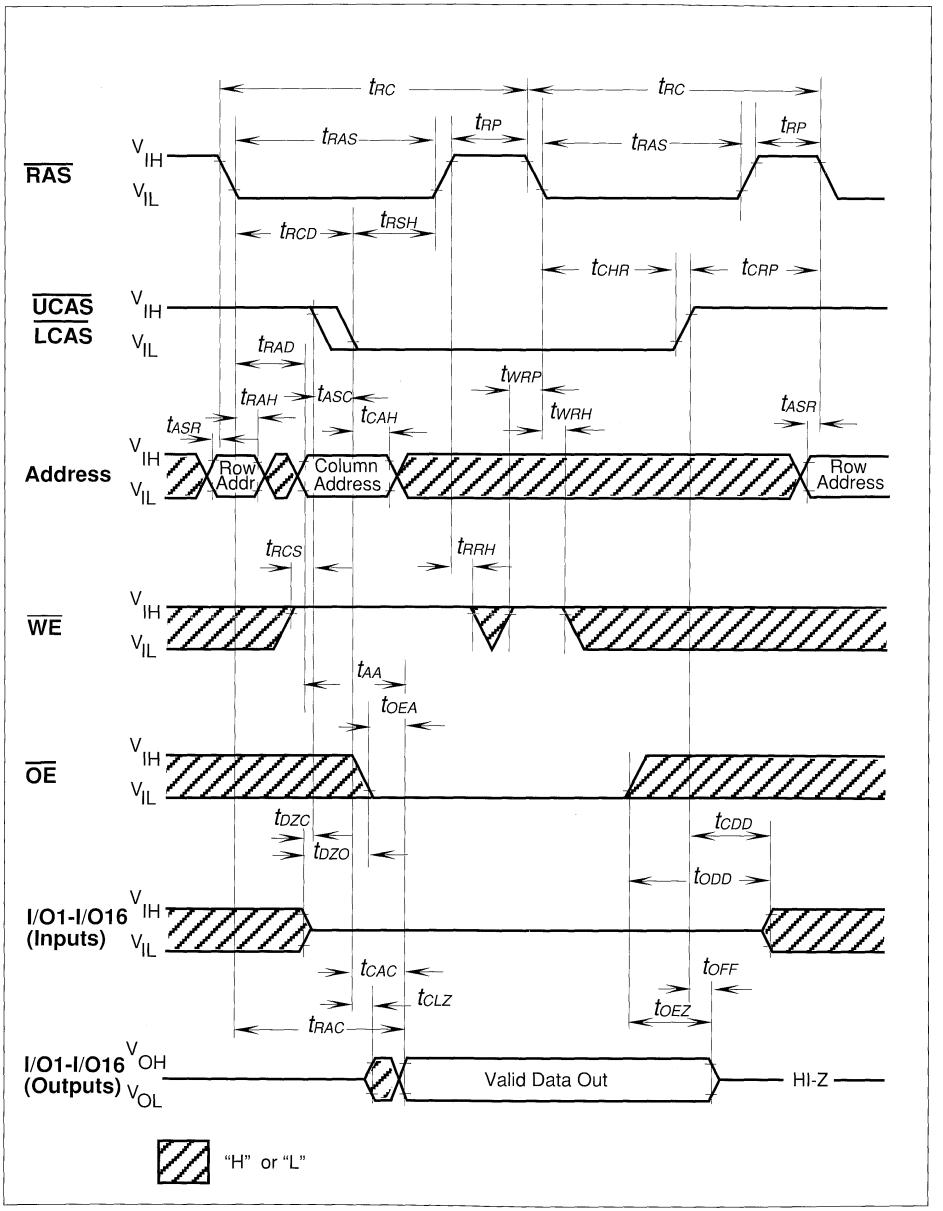
Hyper Page Mode (EDO) Late Write and Read-Modify Write Cylce



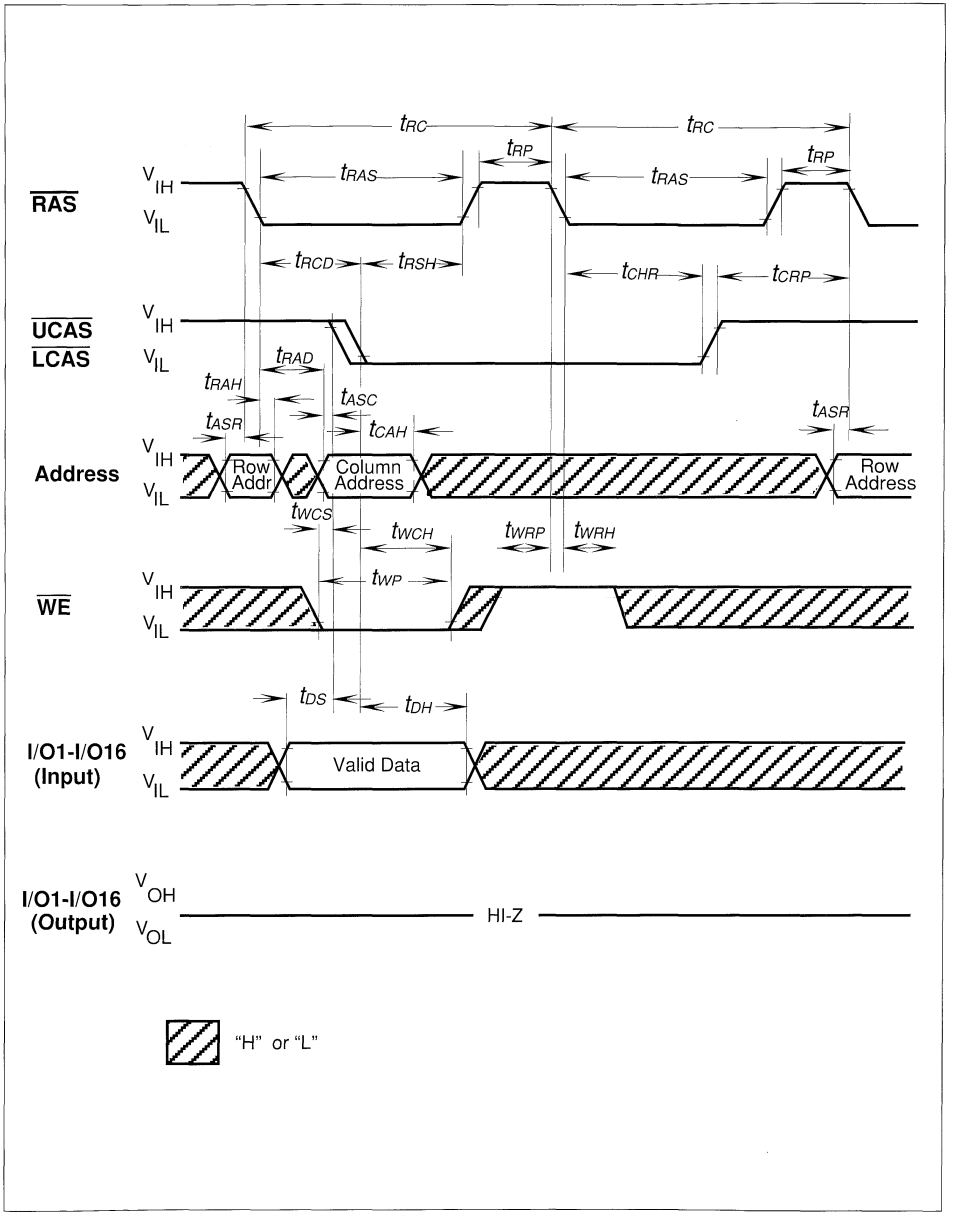
RAS-Only Refresh Cycle



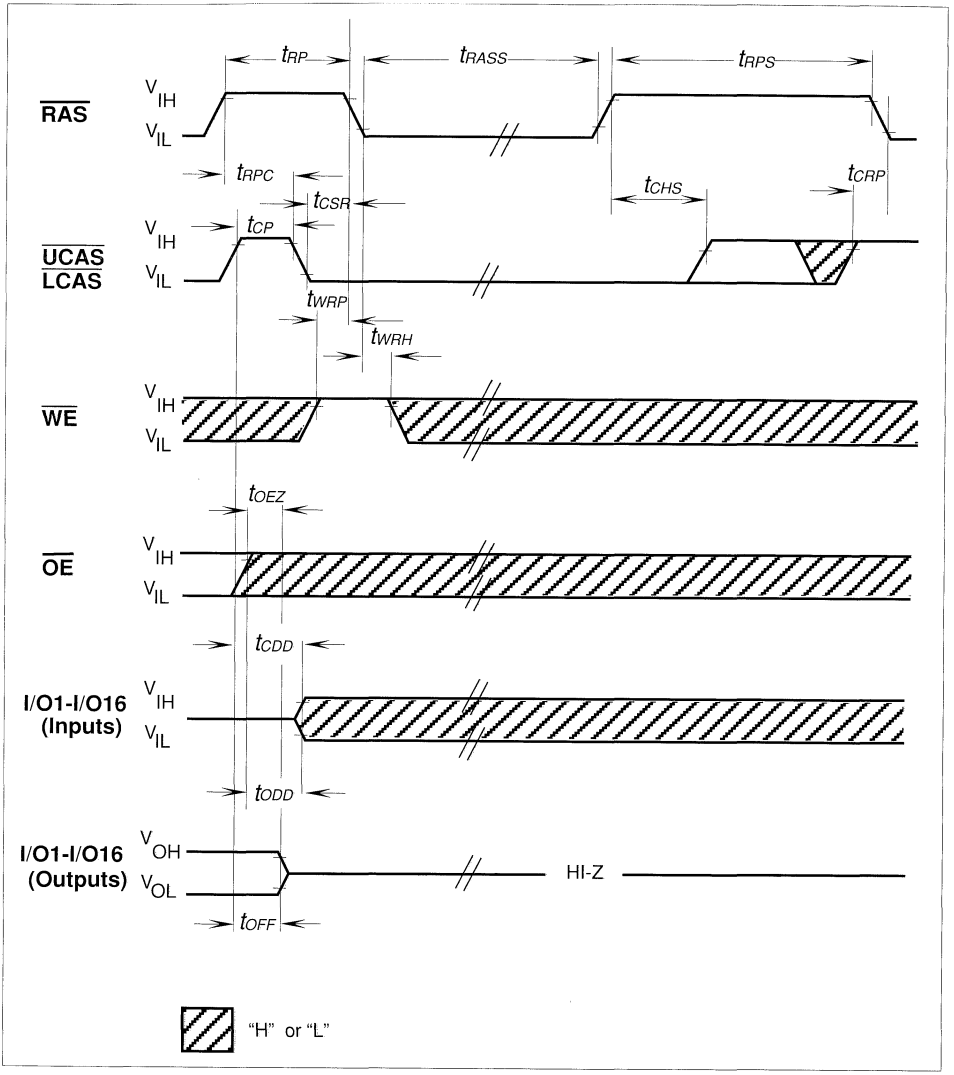
CAS-Before-RAS Refresh Cycle



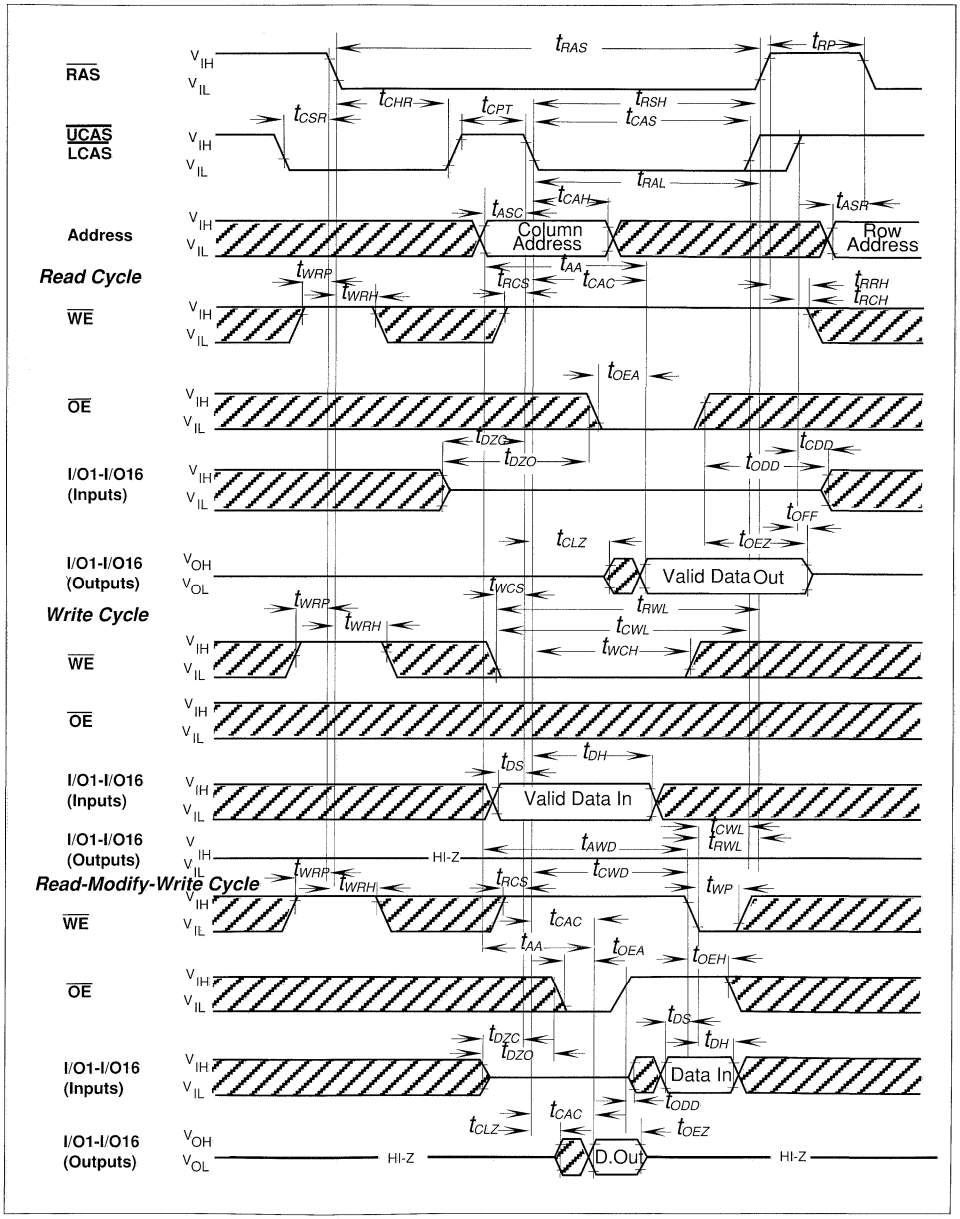
Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Early Write)



$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self Refresh Cycle



CAS-Before-RAS Refresh Counter Test Cycle

16M x 4-Bit Dynamic RAM (4k & 8k Refresh)

HYB 3164400J/T -50/-60
HYB 3165400J/T -50/-60

Preliminary Information

- 16 777 216 words by 4-bit organization
- 0 to 70 °C operating temperature
- Fast access and cycle time
  RAS access time:
  50 ns (-50 version)
  60 ns (-60 version)
  Cycle time:
  90 ns (-50 version)
  110 ns (-60 version)
  CAS access time:
  13 ns (-50 version)
  15 ns (-60 version)
- Fast page mode cycle time
  35 ns (-50 version)
  40 ns (-60 version)
- Single + 3.3 V (± 0.3V) power supply
- Low power dissipation
  max. 396 active mW (HYB 3164400J/T-50)
  max. 360 active mW (HYB 3164400J/T-60)
  max. 504 active mW (HYB 3165400J/T-50)
  max. 432 active mW (HYB 3165400J/T-60)
- 7.2 mW standby (TTL)
  720 µW standby (MOS)
- Read, write, read-modify-write, $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh (CBR),
  $\overline{\text{RAS}}$-only refresh, hidden refresh and self refresh modes
- Fast page mode capability
- 8192 refresh cycles/128 ms , 13 R/ 11C addresses (HYB 3164400J/T)
- 4096 refresh cycles/ 64 ms , 12 R/ 12C addresses (HYB 3165400J/T)
- Plastic Package:
  P-SOJ-34-1 500 mil HYB 3164(5)400J
  P-TSOPII-34-1 500 mil HYB 3164(5)400T

Ordering Information

Type	Ordering Code	Package		Descriptions
HYB 3164400J-50	on request	P-SOJ-34-1	500 mil	DRAM (access time 50 ns)
HYB 3164400J-60	on request	P-SOJ-34-1	500 mil	DRAM (access time 60 ns)
HYB 3164400T-50	on request	P-TSOPII-34-1	500 mil	DRAM (access time 50 ns)
HYB 3164400T-60	on request	P-TSOPII-34-1	500 mil	DRAM (access time 60 ns)
HYB 3165400J-50	on request	P-SOJ-34-1	500 mil	DRAM (access time 50 ns)
HYB 3165400J-60	on request	P-SOJ-34-1	500 mil	DRAM (access time 60 ns)
HYB 3165400T-50	on request	P-TSOPII-34-1	500 mil	DRAM (access time 50 ns)
HYB 3165400T-60	on request	P-TSOPII-34-1	500 mil	DRAM (access time 60 ns)

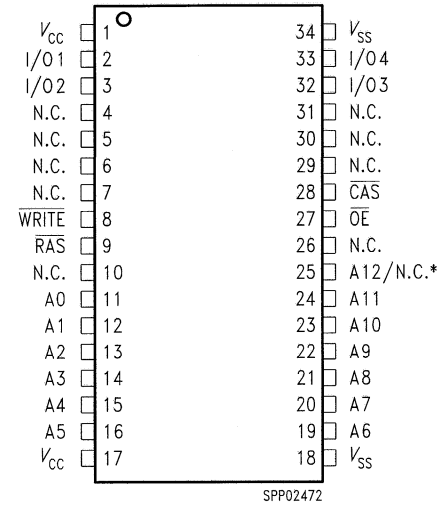
This device is a dynamic RAM organized 16 777 216 by 4 bits. The device is fabricated in SIEMENS/IBM most advanced first generation 64Mbit CMOS silicon gate process technology. The circuit and process design allow this device to achieve high performance and low power dissipation. This DRAM operates with a single 3.3 ± 0.3 V power supply and interfaces with either LVTTL or LVCMOS levels. Multiplexed address inputs permit the HYB 3164(5)400J/T to be packaged in a 500mil wide SOJ-34 or TSOP-34 plastic package. These packages provide high system bit densities and are compatible with commonly used automatic testing and insertion equipment.

Pin Definition and Functions

Pin No.	Function
A0-A12	Address Inputs for HYB 3164400J/T
A0-A11	Address Inputs for HYB 3165400J/T
$\overline{RAS}$	Row Address Strobe
$\overline{OE}$	Output Enable
I/O1-I/O4	Data Input/Output
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power Supply (+ 3.3 V)
V_{SS}	Ground

Pin Configuration
(top view)

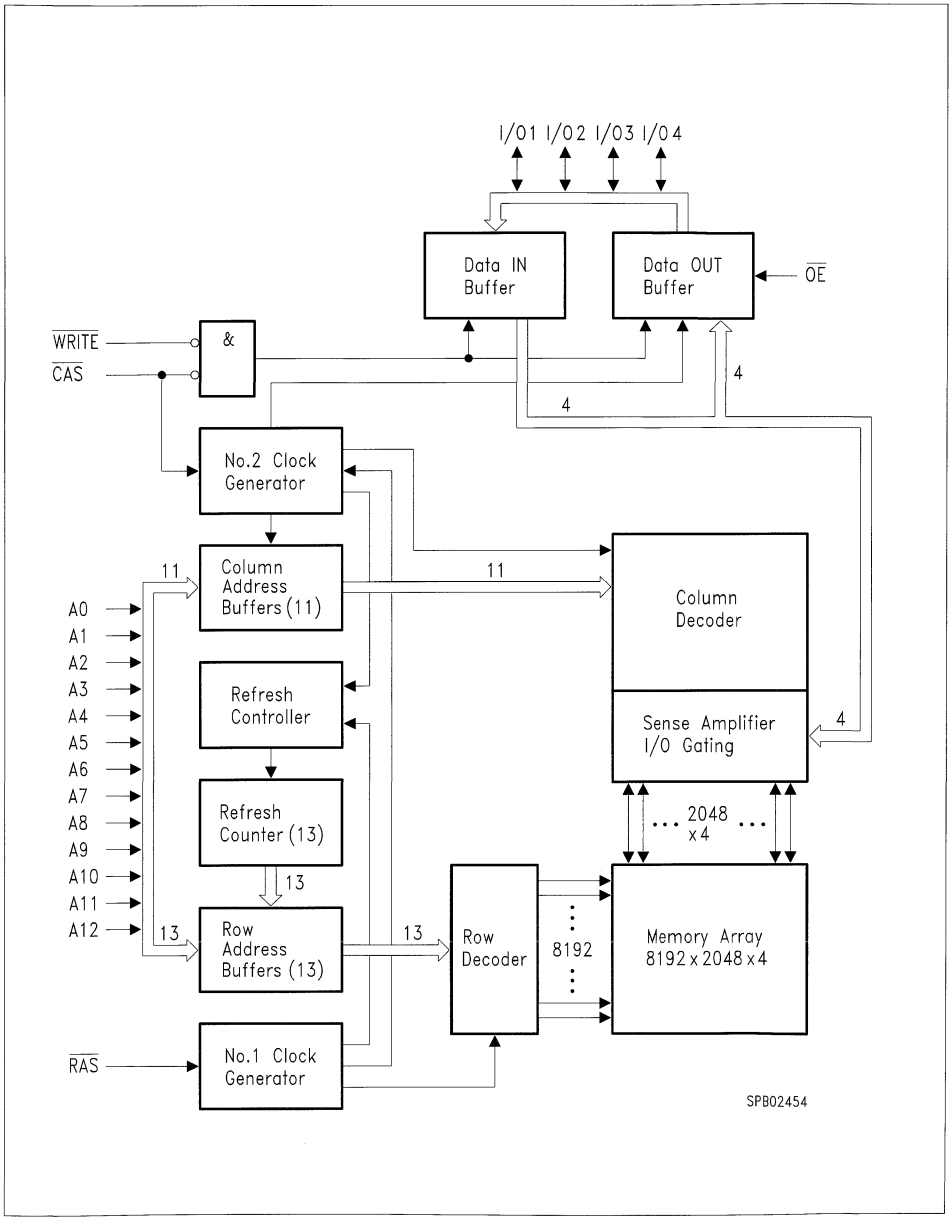
P-SOJ-34-1 (500 mil)
P-TSOPII-34-1 (500 mil)



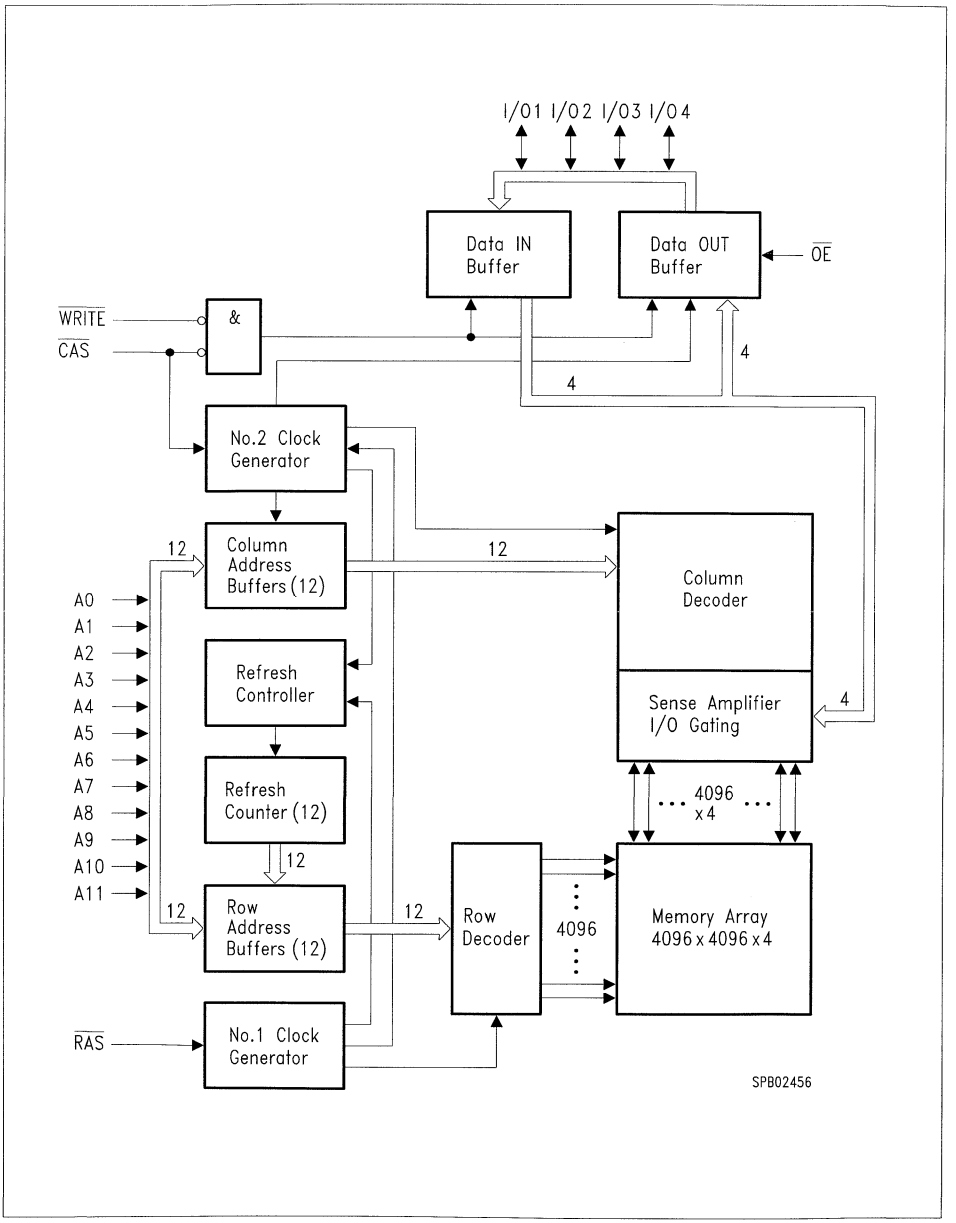
* Pin 25 is A12 for HYB 3164400J/T and N.C. for HYB 3165400J/T

TRUTH TABLE

FUNCTION		RAS	CAS	WRITE	OE	ROW ADDR	COL ADDR	I/O1-I/O4
Standby		H	H - X	X	X	X	X	High Impedance
Read		L	L	H	L	ROW	COL	Data Out
Early-Write		L	L	L	X	ROW	COL	Data In
Delayed-Write		L	L	H - L	H	ROW	COL	Data In
Read-Modify-Write		L	L	H - L	L - H	ROW	COL	Data Out, Data In
Fast Page Mode Read	1st Cycle	L	H - L	H	L	ROW	COL	Data Out
	2nd Cycle	L	H - L	H	L	n/a	COL	Data Out
Fast Page Mode Early Write	1st Cycle	L	H - L	L	X	ROW	COL	Data In
	2nd Cycle	L	H - L	L	X	n/a	COL	Data In
Fast Page Mode RMW	1st Cycle	L	H - L	H - L	L - H	ROW	COL	Data Out, Data In
	2st Cycle	L	H - L	H - L	L - H	n/a	COL	Data Out, Data In
RAS only refresh		L	H	X	X	ROW	n/a	High Impedance
CAS-before-RAS refresh		H - L	L	H	X	X	n/a	High Impedance
Test Mode Entry		H - L	L	L	X	X	n/a	High Impedance
Hidden Refresh	READ	L-H-L	L	H	L	ROW	COL	Data Out
	WRITE	L-H-L	L	L	X	ROW	COL	Data In



Block Diagram for HYB 3164400J/T



Block Diagram for HYB 3165400J/T

Absolute Maximum Ratings [1]

Operating temperature range ..... 0 to 70 °C
Storage temperature range ..... – 55 to 150 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 0.5 to min (V_{CC} + 0.5, 4.6) V
Power supply voltage ..... – 0.5 V to 4.6 V
Power dissipation ..... 1.0 W
Data out current (short circuit) ..... 50 mA

DC Characteristics

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 3 V ± 0.3 V, (values in brackets for HYB 3165400J/T)

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
Input high voltage	V_{IH}	2.0	V_{CC} + 0.3	V	2)
Input low voltage	V_{IL}	– 0.3	0.8	V	2)
Output high voltage (LVTTL) Output „H" level voltage (I_{out} = – 2m A)	V_{OH}	2.4	–	V	
Output low voltage (LVTTL) Output „L"level voltage (I_{out} = + 2m A)	V_{OL}	–	0.4	V	
Output high voltage (LVCMOS) Output „H" level voltage (I_{out} = – 100 uA)	V_{OH}	V_{CC} – 0.2	-	V	6)
Ouput low voltage (LVCMOS) Output „L" level voltage (I_{out} = + 100uA)	V_{OL}	–	0.2	V	6)
Input leakage current,any input (0 V < V_{in} < V_{CC} , all other pins = 0 V	$I_{I(L)}$	– 2	2	µA	
Output leakage current (DO is disabled, 0 V < V_{out} < V_{CC})	$I_{O(L)}$	– 2	2	µA	
Average V_{CC} supply current: -50 ns version -60 ns version ($\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = t_{RC} min.)	I_{CC1}	 – –	 110 (140) 100 (120)	 mA mA	3) 4) 5)
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{ih})	I_{CC2}	–	2	mA	–
Average V_{CC} supply current, during RAS-only refresh cycles: -50 ns version -60 ns version (RAS cycling: CAS = V_{IH}: t_{RC} = t_{RC} min.)	I_{CC3}	 – –	 110 (140) 100 (120)	 mA mA	3) 5)

DC Characteristics (cont'd)

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 3 V ± 0.3 V, (values in brackets for HYB 3165400J/T)

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
Average V_{CC} supply current, during fast page mode: -50 ns version -60 ns version ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling: t_{PC}=t_{PC} min.)	I_{CC4}	– –	85 (85) 75 (75)	mA mA	3) 4) 5)
Standby V_{CC} supply current ($\overline{RAS}$=$\overline{CAS}$= V_{CC} – 0.2 V)	I_{CC5}	–	200	A	–
Average V_{CC} supply current, during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode: -50 ns version -60 ns version ($\overline{RAS}$, $\overline{CAS}$ cycling: t_{RC} = t_{RC} min.)	I_{CC6}	– –	110 (140) 100 (120)	mA mA	3) 4)
Self Refresh Current Average Power Supply Current during Self Refresh. ($\overline{CBR}$ cycle with t_{RAS}>t_{RASS} min, $\overline{CAS}$ held low, $\overline{WE}$ = V_{CC} – 0.2 V, Address and Din=V_{cc} – 0.2 V or 0.2 V)	I_{CC7}	–	200	A	

AC Characteristics (Notes: 7,8,9,10)
T_A = 0 to 70 °C, V_{CC} = 3.3 ± 0.3 V

Parameter	Symbol	Limit Values				Unit	Note
		HYB 3164(5)400 J/T-50		HYB 3164(5)400 J/T-60			
		min.	max.	min.	max.		
Random read or write cycle time	t_{RC}	90	–	110	–	ns	11
Read-write cycle time	t_{RWC}	126	–	150	–	ns	
Fast page mode cycle time	t_{PC}	35	–	40	–	ns	11
Fast page mode read-write cycle time	t_{PRWC}	71	–	80	–	ns	11
Access time from RAS	t_{RAC}	–	50	–	60	ns	11,12 13,18
Access time from CAS	t_{CAC}	–	13	–	15	ns	11,12 18
Access time from column address	t_{AA}	–	25	–	30	ns	11,12 18
Access time from CAS precharge	t_{CPA}	–	30	–	35	ns	11 18
CAS to output in low-Z	t_{CLZ}	0	–	0	–	ns	18
Output buffer turn-off delay	t_{OFF}	–	13	–	15	ns	20
Transition time (rise and fall)	t_T	3	30	3	30	ns	8
RAS precharge time	t_{RP}	30	–	40	–	ns	
RAS pulse width	t_{RAS}	50	100k	60	100k	ns	11
RAS pulse width (fast page mode)	t_{RASP}	50	200k	60	200k	ns	11
$\overline{CAS}$ precharge to $\overline{RAS}$ Delay (fast page mode)	t_{RHCP}	30	–	35	–	ns	
$\overline{CAS}$ precharge to $\overline{WE}$ (FPM RMW)	t_{CPW}	48	–	55	–	ns	16
RAS hold time	t_{RSH}	13	–	15	–	ns	
CAS hold time	t_{CSH}	50	–	60	–	ns	
CAS pulse width	t_{CAS}	13	100k	15	100k	ns	11
RAS to CAS delay time	t_{RCD}	18	37	20	45		12
RAS to column address delay time	t_{RAD}	13	25	15	30	ns	13

AC Characteristics (Notes: 7,8,9,10) (cont'd)
T_A = 0 to 70 °C, V_{CC} = 3.3 ± 0.3 V

Parameter	Symbol	Limit Values				Unit	Note
		HYB 3164(5)400 J/T-50		HYB 3164(5)400 J/T-60			
		min.	max.	min.	max.		
CAS to RAS precharge time	t_{CRP}	5	–	5	–	ns	11
CAS precharge time	t_{CP}	10	–	10	–	ns	
Row address setup time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	8	–	10	–	ns	
Column address setup time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	10	–	10	–	ns	
Column address to RAS lead time	t_{RAL}	25	–	30	–	ns	11
Read command setup time	t_{RCS}	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	ns	19
Read command hold time referenced to RAS	t_{RRH}	0	–	0	–	ns	
Write command hold time	t_{WCH}	8	–	10	–	ns	
Write command pulse width	t_{WP}	8	–	10	–	ns	
Write command to RAS lead time	t_{RWL}	13	–	15	–	ns	
Write command to CAS lead time	t_{CWL}	13	–	15	–	ns	
Data setup time	t_{DS}	0	–	0	–	ns	17
Data hold time	t_{DH}	10	–	10	–	ns	17
Refresh period for HYB 3164400J/T	t_{REF}	–	128	–	128	ms	
Refresh period for HYB 3165400J/T	t_{REF}	–	64	–	64	ms	
Write command setup time	t_{WCS}	0	–	0	–	ns	16
CAS to WRITE delay time (RMW)	t_{CWD}	31	–	35	–	ns	16
RAS to WRITE delay time (RMW)	t_{RWD}	68	–	80	–	ns	16
Column address to WRITE delay time (RMW)	t_{AWD}	43	–	50	–	ns	16
CAS setup time (CAS-before-RAS cycle)	t_{CSR}	5	–	5	–	ns	

AC Characteristics (Notes: 7,8,9,10) (cont'd)
T_A = 0 to 70 °C, V_{CC} = 3.3 ± 0.3 V

Parameter	Symbol	Limit Values				Unit	Note
		HYB 3164(5)400 J/T-50		HYB 3164(5)400 J/T-60			
		min.	max.	min.	max.		
CAS hold time (CAS-before-RAS cycle)	t_{CHR}	10	–	10	–	ns	
RAS to CAS precharge time	t_{RPC}	5	–	5	–	ns	
CAS precharge time (CAS-before-RAS counter test cycle)	t_{CPT}	25	–	30	–	ns	
Write command setup time (in test mode entry cycle)	t_{WTS}	10	–	10	–	ns	
Write command hold time (in test mode entry cycle)	t_{WTH}	10	–	10	–	ns	
Write to RAS precharge time (CAS-before-RAS cycle)	t_{WRP}	10	–	10	–	ns	
Write hold time referenced to RAS (CAS-before-RAS cycle)	t_{WRH}	10	–	10	–	ns	
OE command hold time	t_{OEH}	13	–	15	–	ns	
OE access time	t_{OEA}	–	13	–	15	ns	11,18
Output buffer turn-off delay from OE	t_{OEZ}	–	13	–	15	ns	20
CAS delay time from Din	t_{DZC}	0	–	0	–	ns	15
Data to OE low delay	t_{DZO}	0	–	0	–	ns	15
CAS high to data delay	t_{CDD}	13	–	15	–	ns	14
OE high to data delay	t_{ODD}	13	–	15	–	ns	14
RAS pulse width during self refresh cycle	t_{RASS}	100k	–	100k	–	ns	21
RAS precharge time during self refresh	t_{RPS}	90	–	110	–		21
CAS hold time during self refresh	t_{CHS}	50	–	50	–	ns	21

Capacitance

T_A = 0 to 25 °C, V_{CC} = 3.3 V ± 0.3 V, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A11,A12)	C_{I1}	–	5	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	C_{I2}	–	7	pF
I/O capacitance (I/O1-I/O4)	C_{IO}	–	7	pF

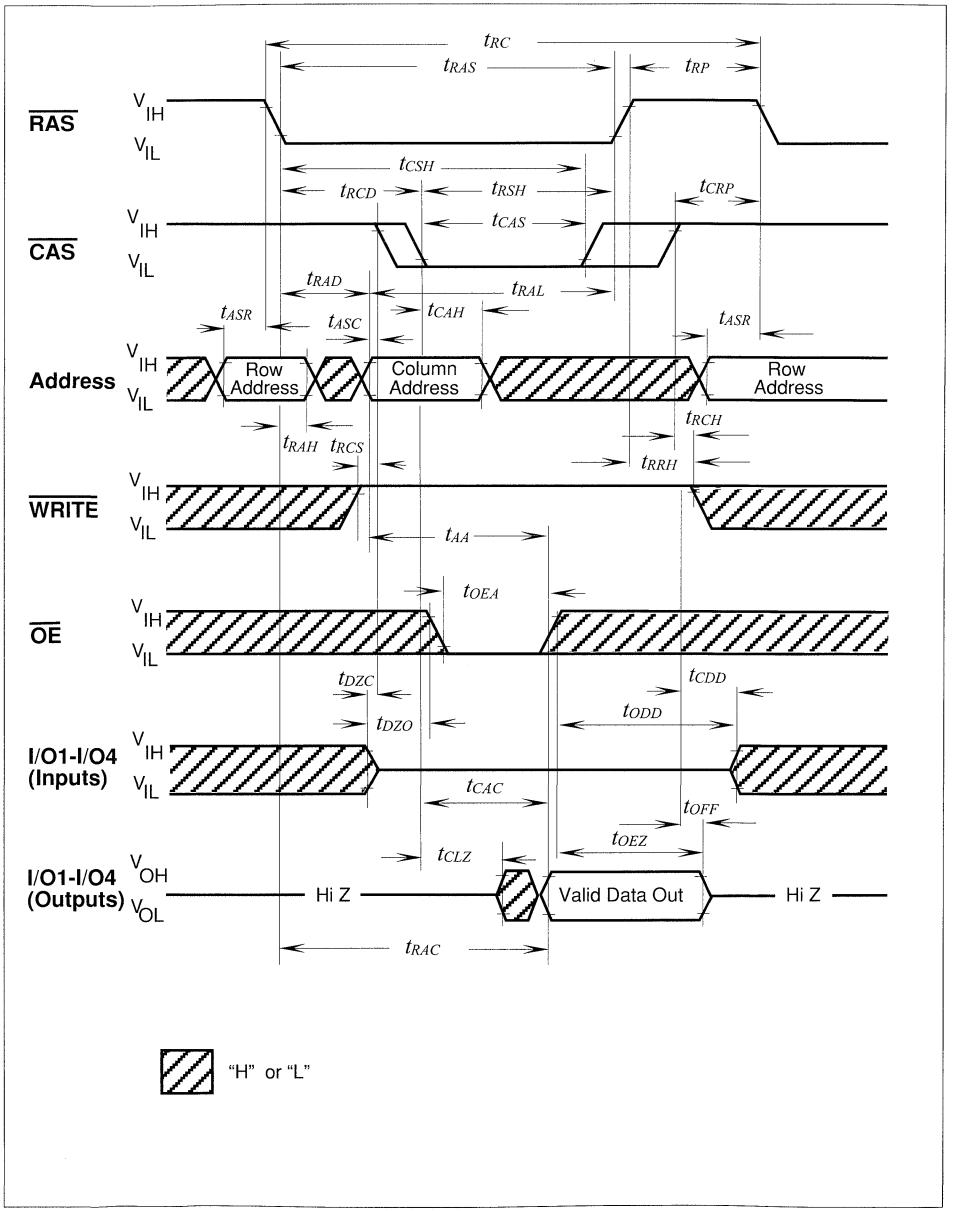
Notes:

1) Stresses greater than listed under „Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ration conditions for extended periods may affect relialibity.
2) All voltages are referenced to V_{SS}.
3) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} and I_{CC7} depend on cycle rate.
4) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.
5) Column address can be changed once or less while RAS = V_{il} and CAS = V_{ih}
6) V_{ol} (LVCMOS) and V_{oh} (LVCMOS) levels are not inteded for use as timing reference levels. LVCMOS levels are the quiescent state of a low impedance output driver, under the specified load conditions.
7) An initial pause of 100 µs is required after power-up followed by 8 $\overline{\text{RAS}}$-only-refresh cycles, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ initialization cycles instead of 8 $\overline{\text{RAS}}$ cycles are required.
8) AC measurements assume tT = 5 ns.
9) $V_{IH\ (min.)}$ and $V_{IL\ (max.)}$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
10) Valid column addresses are only A0 through A10 for HYB 3164400 and A0 through A11 for HYB 316500..
11) In a Test mode Read cylce, the value of t_{RAS}, t_{AA}, t_{CAC} and t_{CPA} are delayed by 5ns, from the specified value. These parameters must be adjusted in Test Mode cycles by adding 5ns to the specified value. Associated timings must also be adjusted by 5ns.
12) Operation within the $t_{RCD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RCD\ (max.)}$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD\ (max.)}$ limit, then access time is controlled by t_{CAC}.
13) Operation within the $t_{RAD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RAD\ (max.)}$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD\ (max.)}$ limit, then access time is controlled by t_{AA}.
15) Either t_{DZC} or t_{DZO} must be satisfied.
16) Either t_{CDD} or t_{ODD} must be satisfied.
16) t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS\ (min.)}$, the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} > t_{RWD\ (min.)}$, $t_{CWD} > t_{CWD\ (min.)}$, $t_{AWD} > t_{AWD\ (min.)}$ and $t_{CPWD} > t_{CPWD\ (min.)}$, the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.
17) These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WRITE}}$ leading edge in Read-Modify-Write cycles.
18) Measured with the specified current load and 100 pF.
19) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
20) $t_{OFF\ (max.)}$ and $t_{OEZ\ (max.)}$ define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.
22) When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:

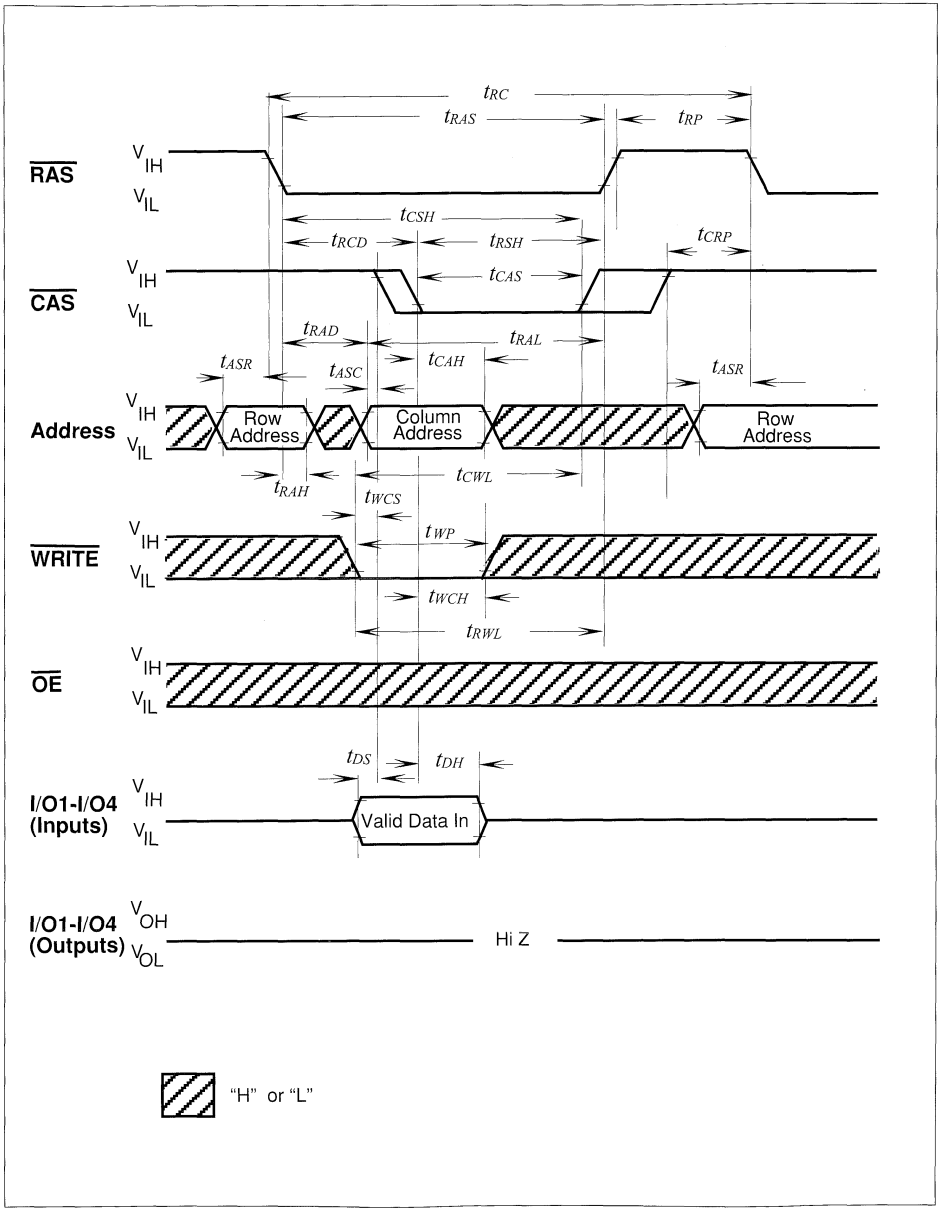
If row addresses are being refresh in an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediatly after exit from Self Refresh.

If row addresses are being refresh in any other manner (ROR - Distributed/Burst or CBR-Burst) over the refresh interval, then a full set of row refreshed must be performed immediately before entry to and immediatey after exit from Self Refresh.

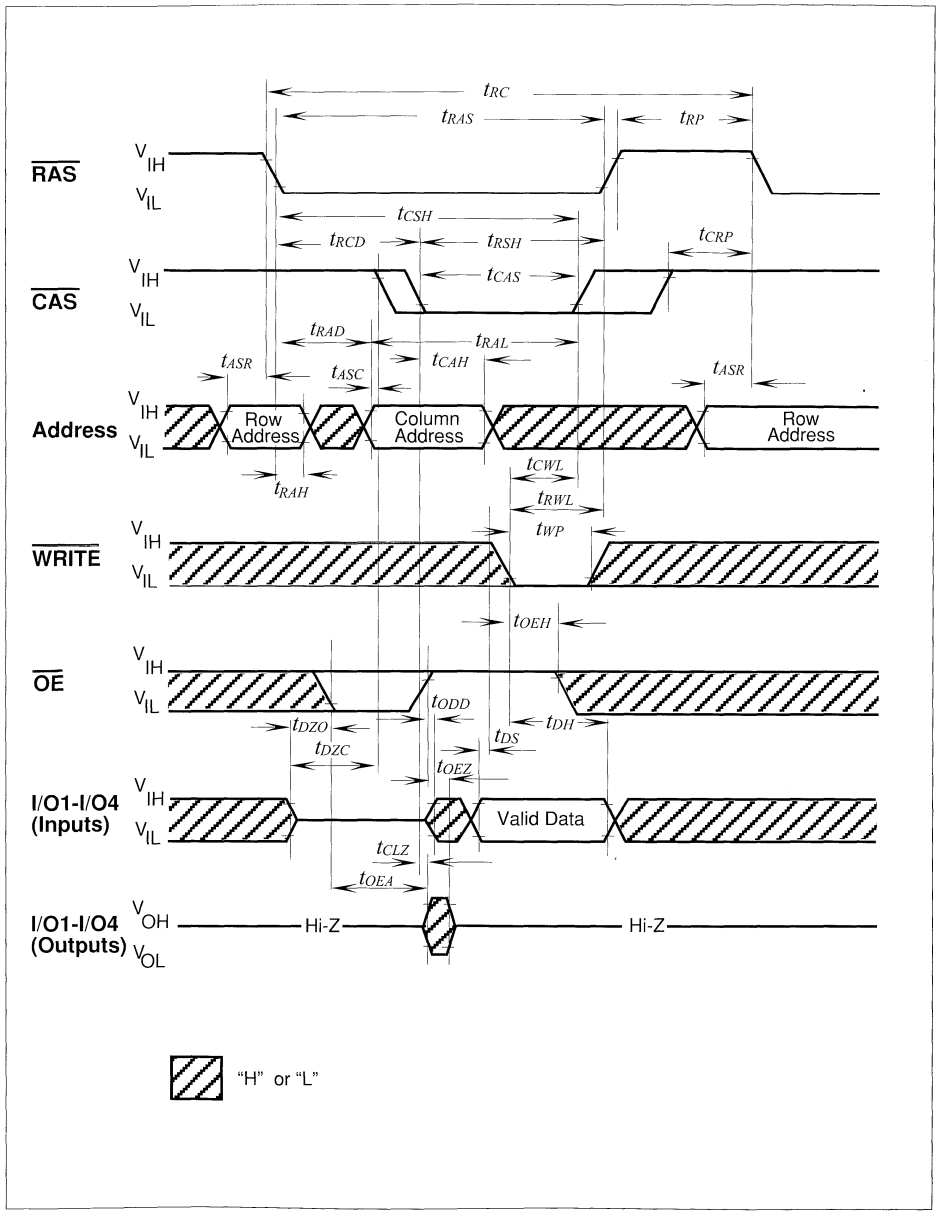
WAVEFORMS



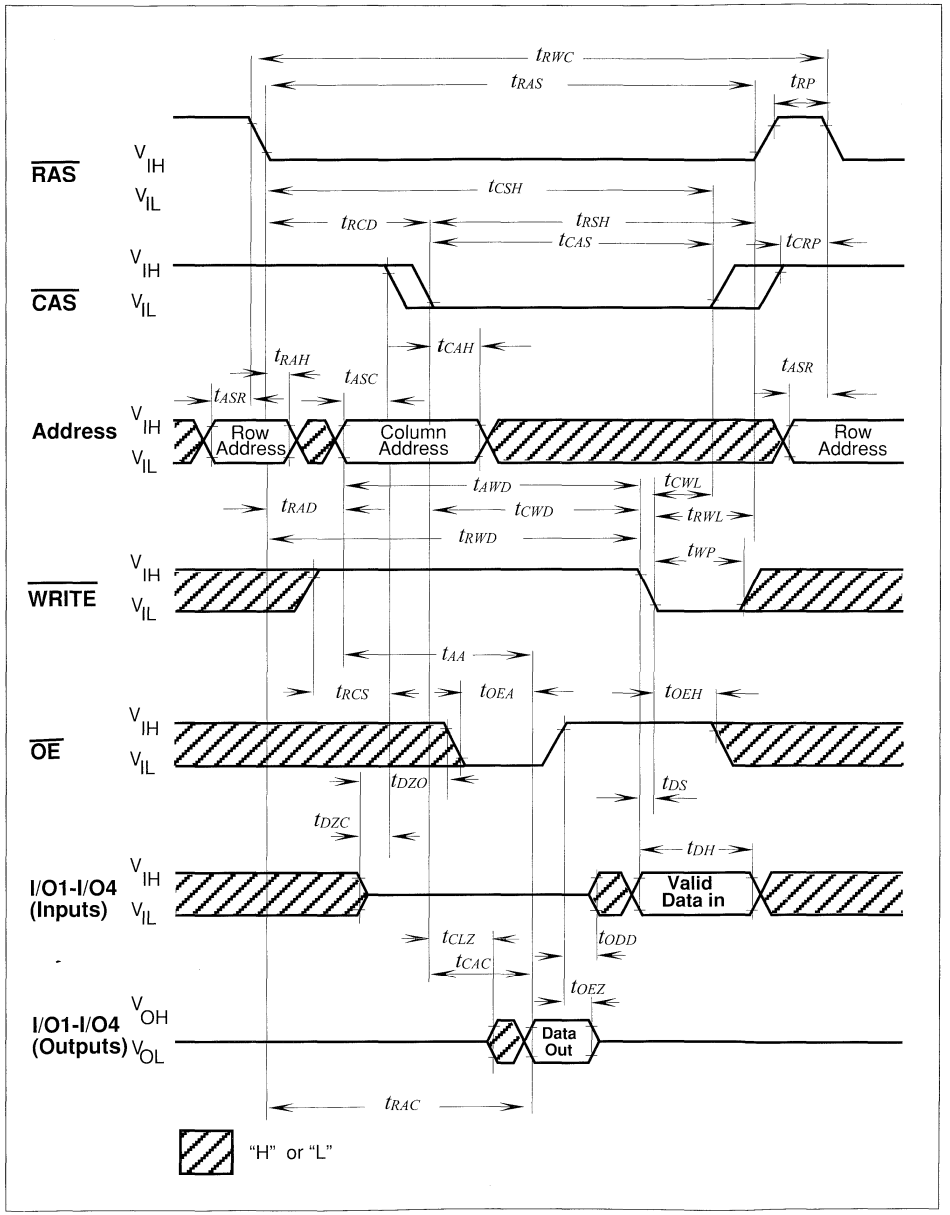
Read Cycle



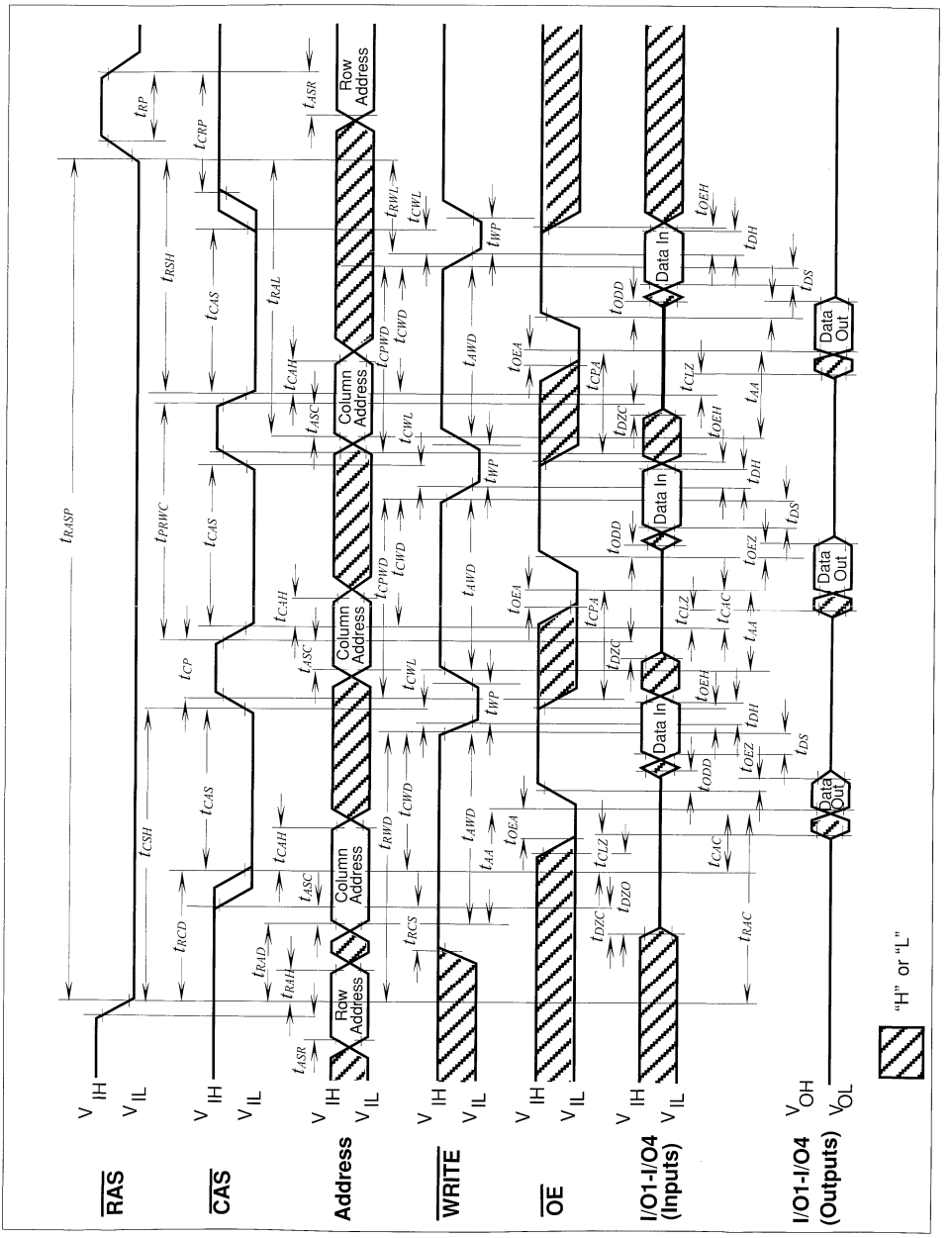
Write Cycle (Early Write)



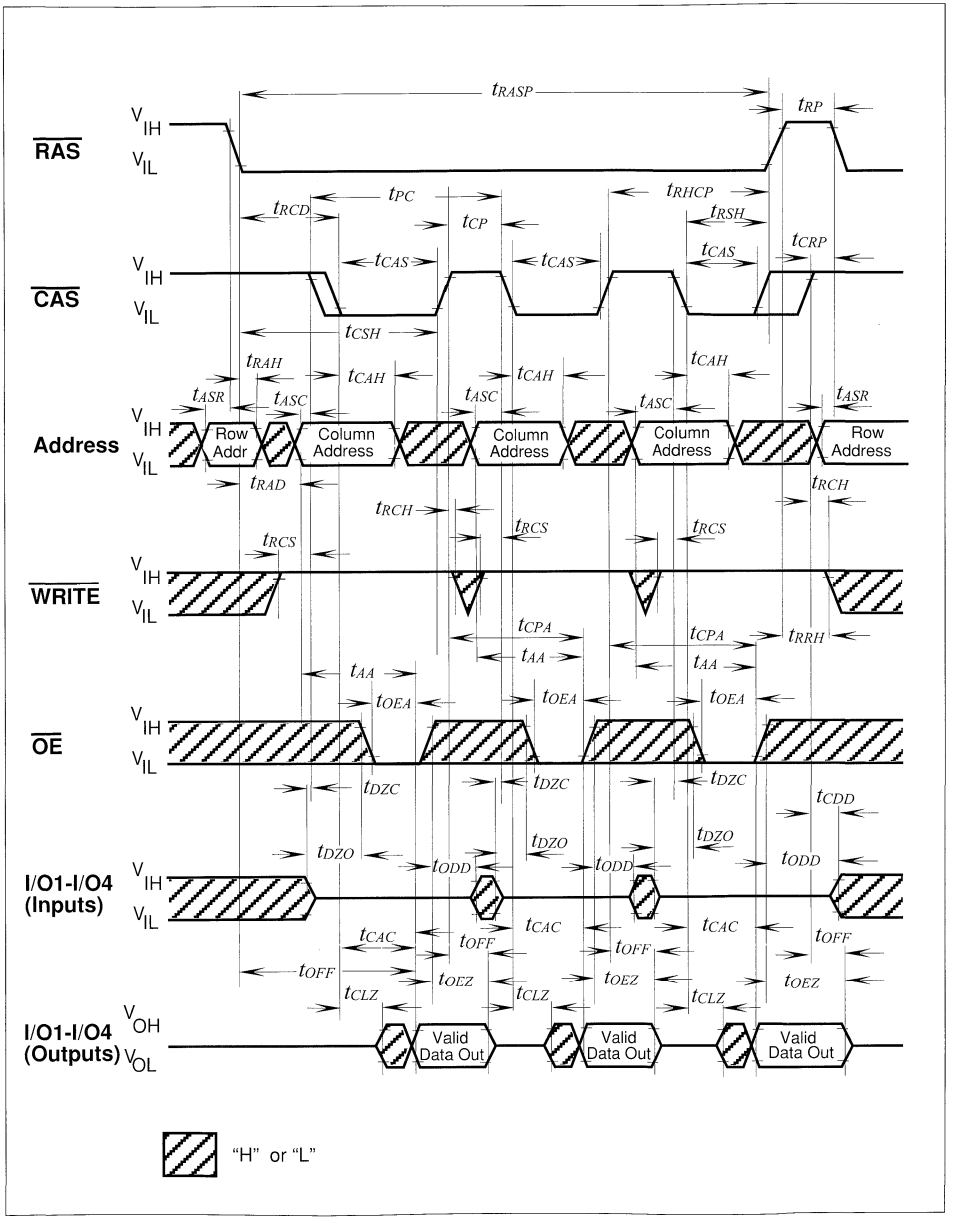
Write Cycle ($\overline{OE}$ Controlled Write)



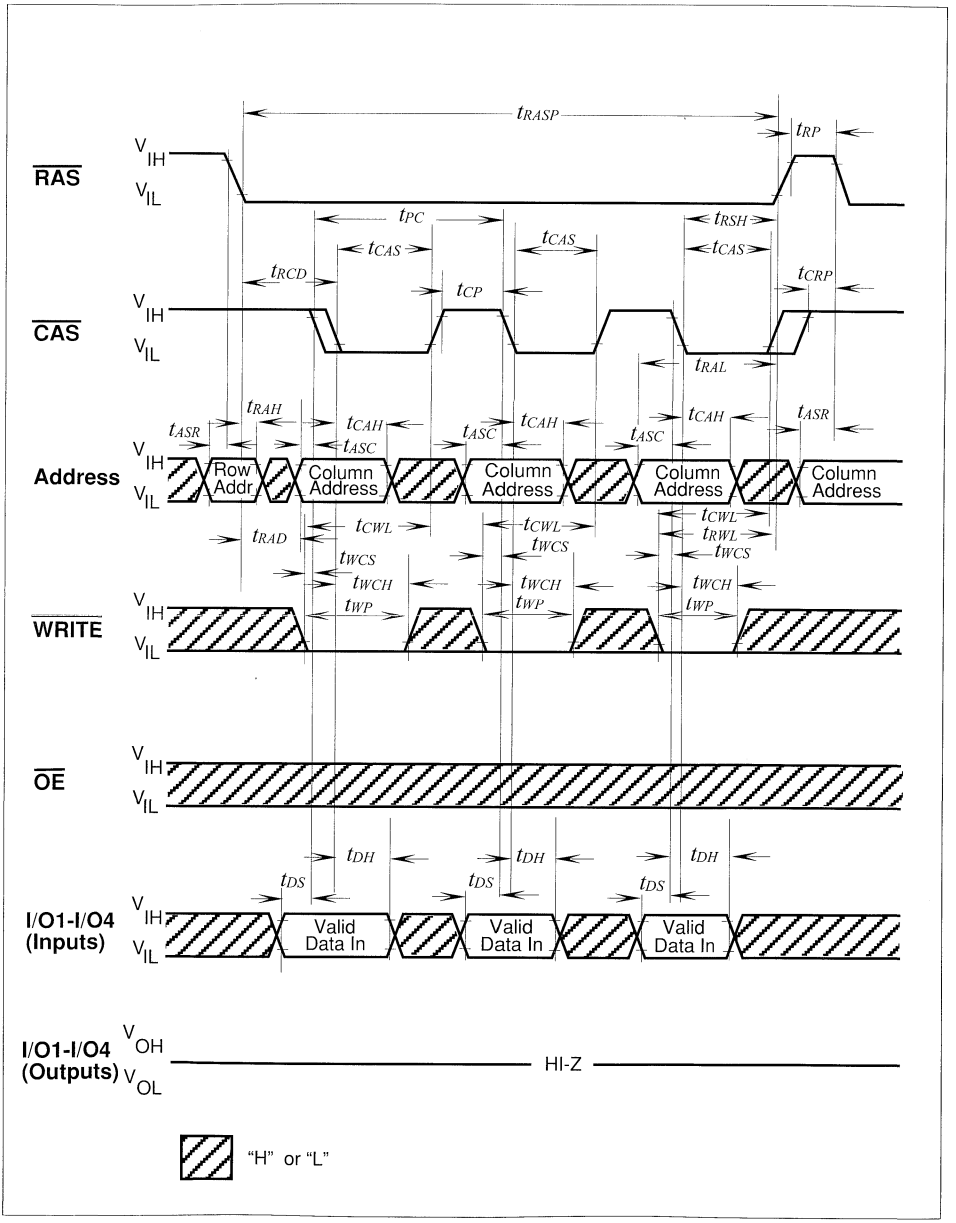
Read-Write (Read-Modify-Write) Cycle



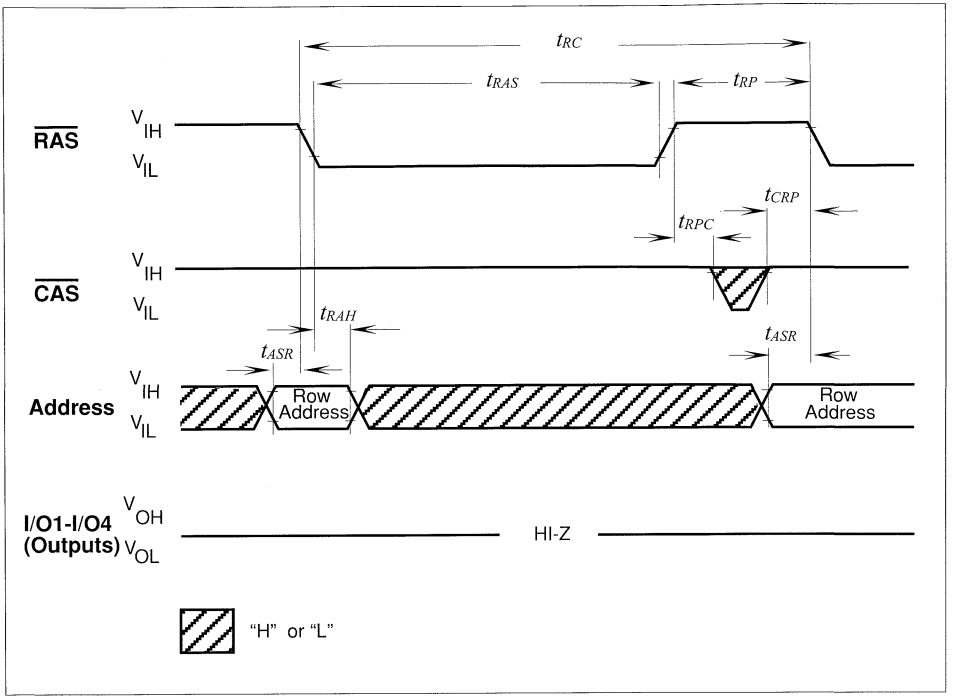
Fast Page Mode Read-Modify-Write Cycle



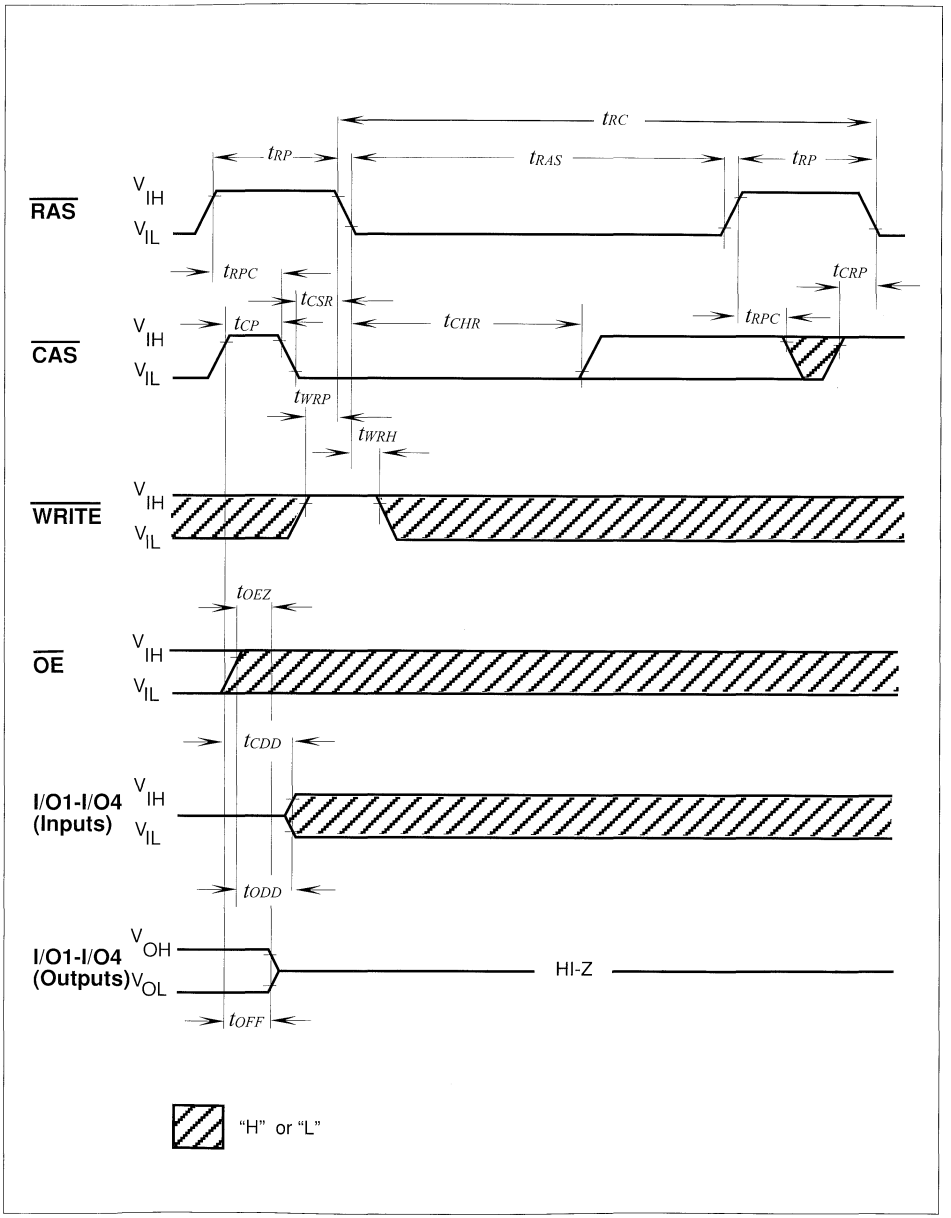
Fast Page Mode Read Cycle



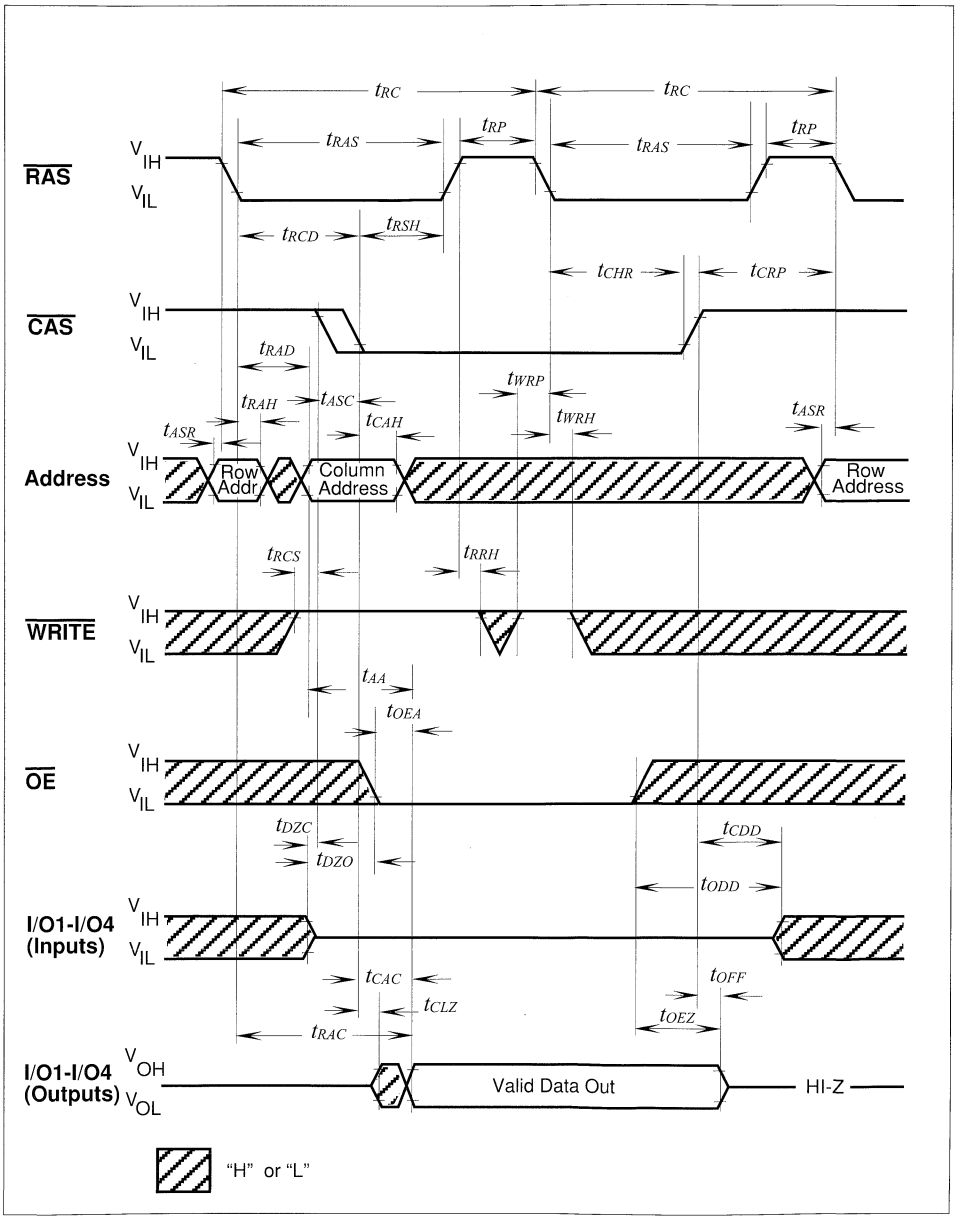
Fast Page Mode Early Write Cycle



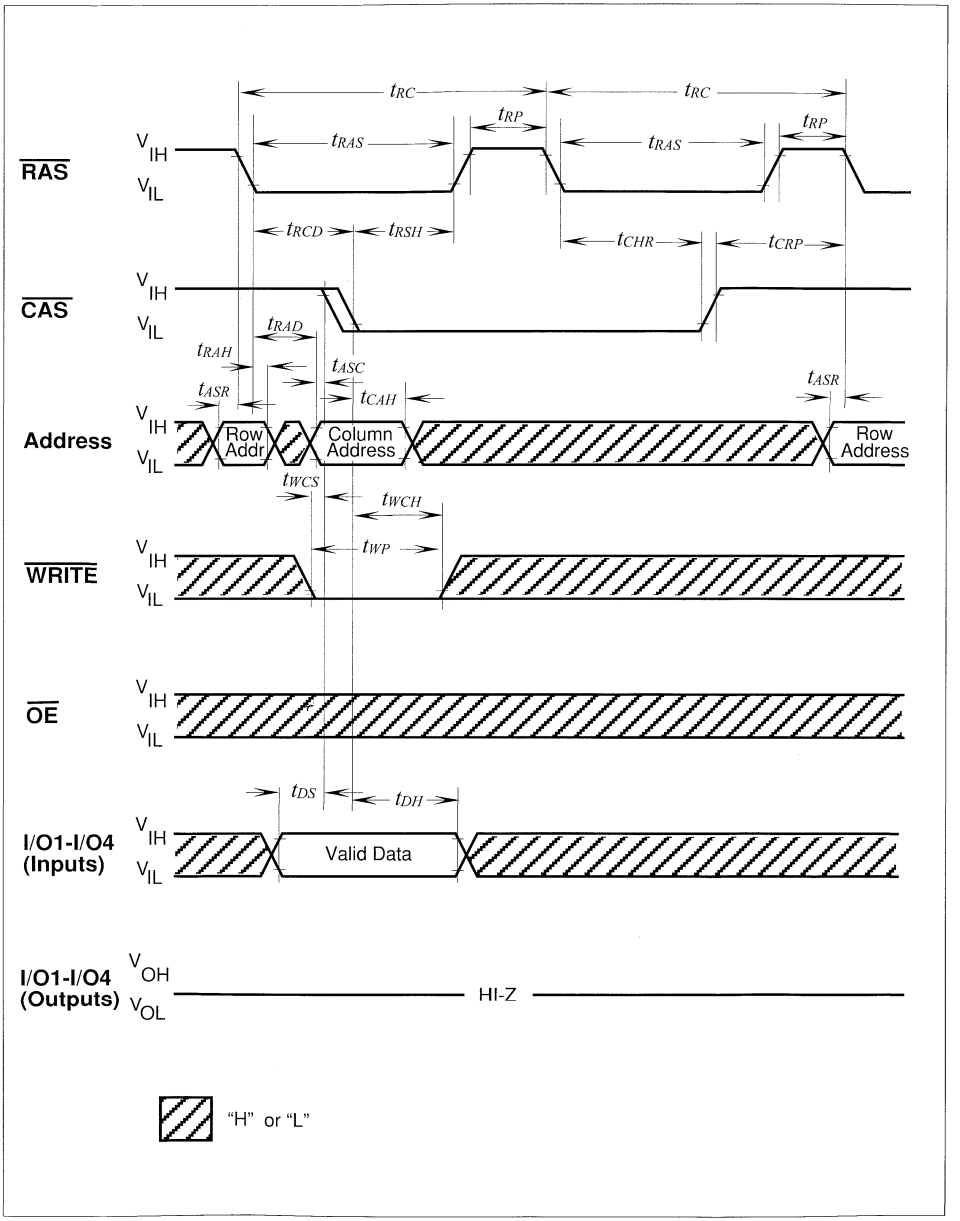
RAS-Only Refresh Cycle



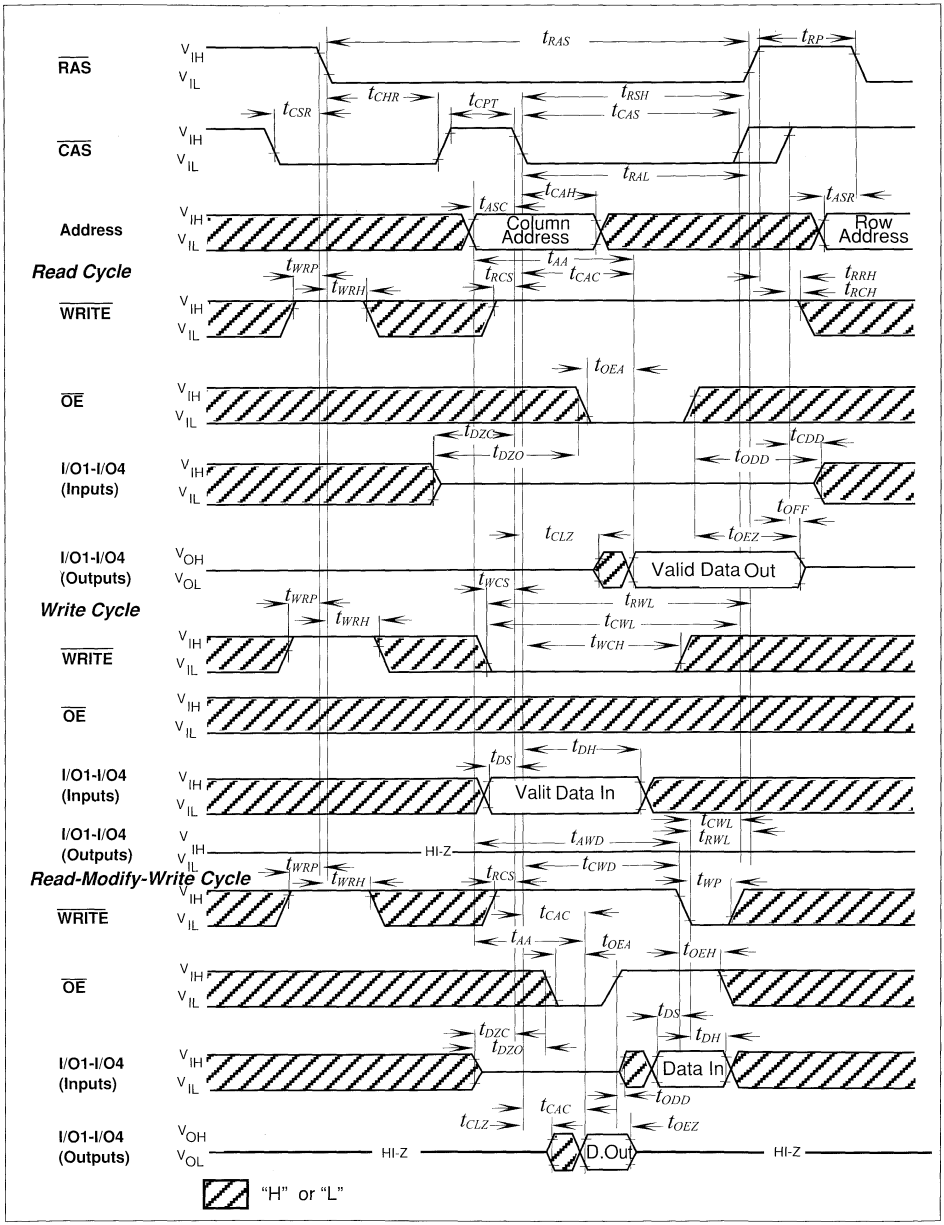
CAS-Before-RAS Refresh Cycle



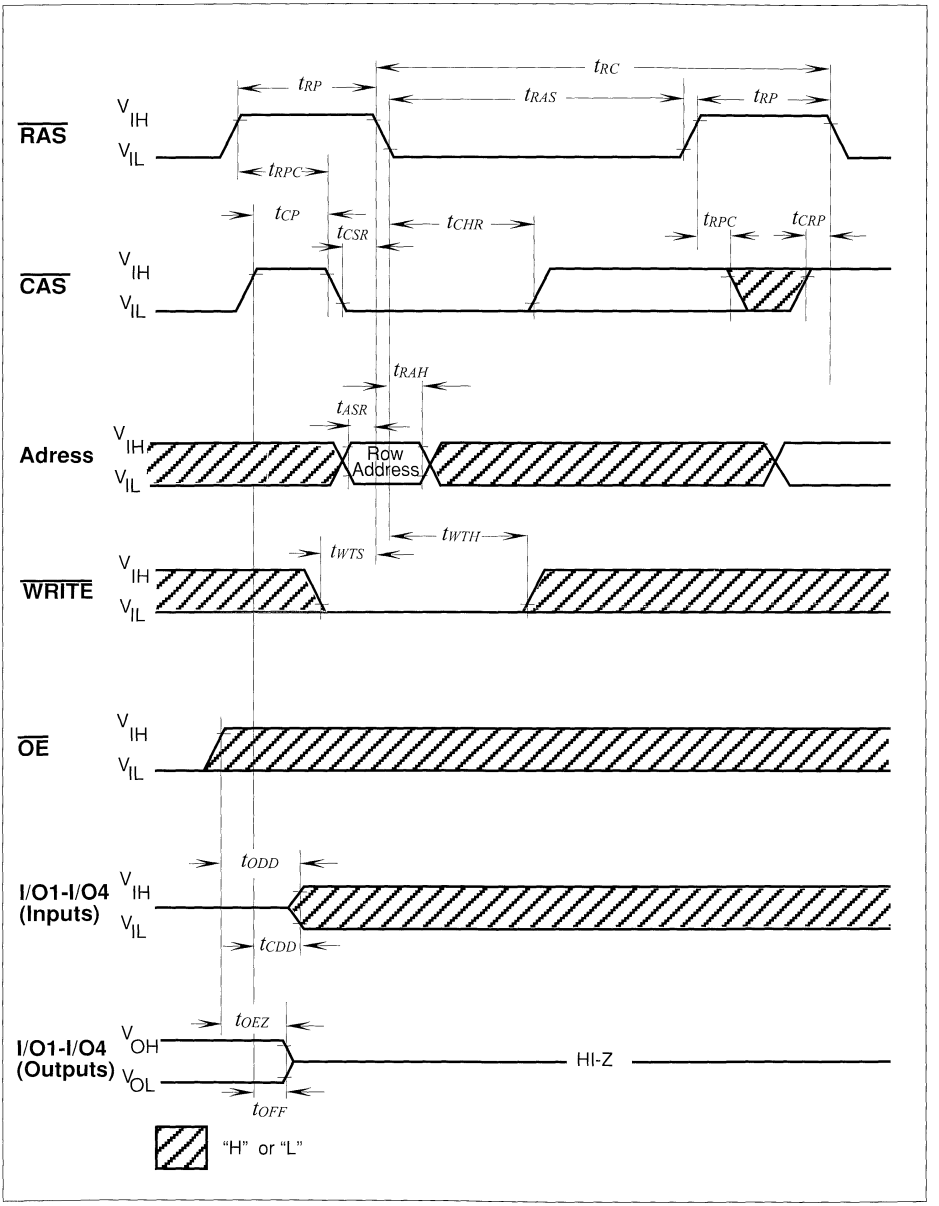
Hidden Refresh Cycle (Read)



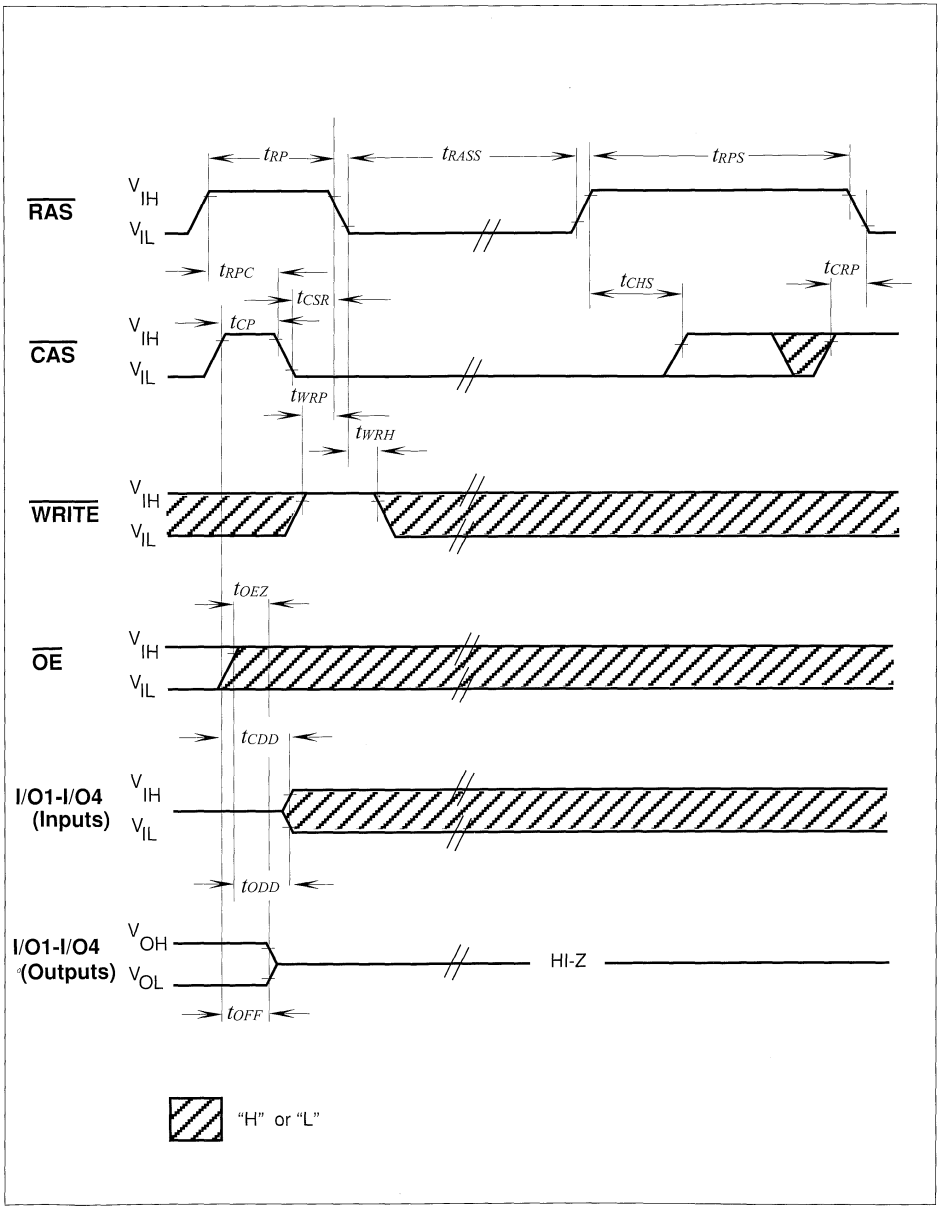
Hidden Refresh Cycle (Early Write)



CAS-Before-RAS Refresh Counter Test Cycle



Test Mode Entry



CAS-before-RAS Self Refresh

8M x 8-Bit Dynamic RAM (4k & 8k Refresh)

HYB 3164800J/T -50/-60
HYB 3165800J/T -50/-60

Preliminary Information

- 8 388 608 words by 8-bit organization
- 0 to 70 °C operating temperature
- Fast access and cycle time
  $\overline{RAS}$ access time:
  50 ns (-50 version)
  60 ns (-60 version)
  Cycle time:
  90 ns (-50 version)
  110 ns (-60 version)
  $\overline{CAS}$ access time:
  13 ns (-50 version)
  15 ns (-60 version)
- Fast page mode cycle time
  35 ns (-50 version)
  40 ns (-60 version)
- Single + 3.3 V (± 0.3 V) power supply
- Low power dissipation
  max. 396 active mW (HYB 3164800J/T-50)
  max. 360 active mW (HYB 3164800J/T-60)
  max. 504 active mW (HYB 3165800J/T-50)
  max. 432 active mW (HYB 3165800J/T-60)
  7.2 mW standby (TTL)
  720 µW standby (MOS)
- Read, write, read-modify-write, $\overline{CAS}$-before-$\overline{RAS}$ refresh (CBR),
  $\overline{RAS}$-only refresh, hidden refresh and self refresh modes
- Fast page mode capability
- 8192 refresh cycles/128 ms , 13 R/ 10C addresses (HYB 3164800J/T)
- 4096 refresh cycles/ 64 ms , 12 R/ 11C addresses (HYB 3165800J/T)
- Plastic Package:
  P-SOJ-34-1 500 mil HYB 3164(5)800J
  P-TSOPII-34-1 500 mil HYB 3164(5)800T

Ordering Information

Type	Ordering Code	Package		Descriptions
HYB 3164800J-50	on request	P-SOJ-34-1	500 mil	DRAM (access time 50 ns)
HYB 3164800J-60	on request	P-SOJ-34-1	500 mil	DRAM (access time 60 ns)
HYB 3164800T-50	on request	P-TSOPII-34-1	500 mil	DRAM (access time 50 ns)
HYB 3164800T-60	on request	P-TSOPII-34-1	500 mil	DRAM (access time 60 ns)
HYB 3165800J-50	on request	P-SOJ-34-1	500 mil	DRAM (access time 50 ns)
HYB 3165800J-60	on request	P-SOJ-34-1	500 mil	DRAM (access time 60 ns)
HYB 3165800T-50	on request	P-TSOPII-34-1	500 mil	DRAM (access time 50 ns)
HYB 3165800T-60	on request	P-TSOPII-34-1	500 mil	DRAM (access time 60 ns)

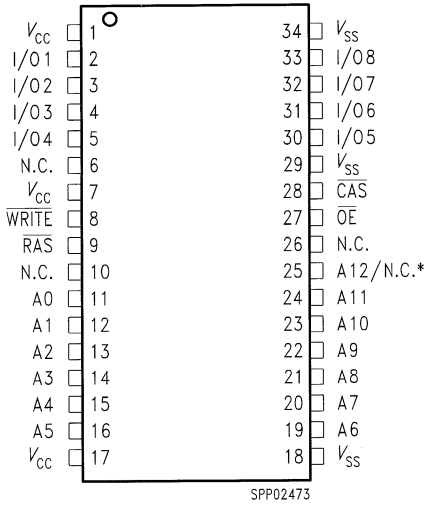
This device is a dynamic RAM organized 8 388 608 by 8 bits. The device is fabricated in SIEMENS/ IBM/TOSHIBAs most advanced second generation 64Mbit CMOS silicon gate process technology. The circuit and process design allow this device to achieve high performance and low power dissipation. This DRAM operates with a single 3.3 ± 0.3 V power supply and interfaces with either LVTTL or LVCMOS levels. Multiplexed address inputs permit the HYB 3164(5)800J/T to be packaged in a 500 mil wide SOJ-34 or TSOP-34 plastic package. These packages provide high system bit densities and are compatible with commonly used automatic testing and insertion equipment.

Pin Definitions and Functions

Pin No.	Function
A0-A12	Address Inputs for HYB 3164800J/T
A0-A11	Address Inputs for HYB 3165800J/T
$\overline{RAS}$	Row Address Strobe
$\overline{OE}$	Output Enable
I/O1-I/O8	Data Input/Output
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{cc}	Power Supply (+ 3.3 V)
V_{ss}	Ground

Pin Configuration
(top view)

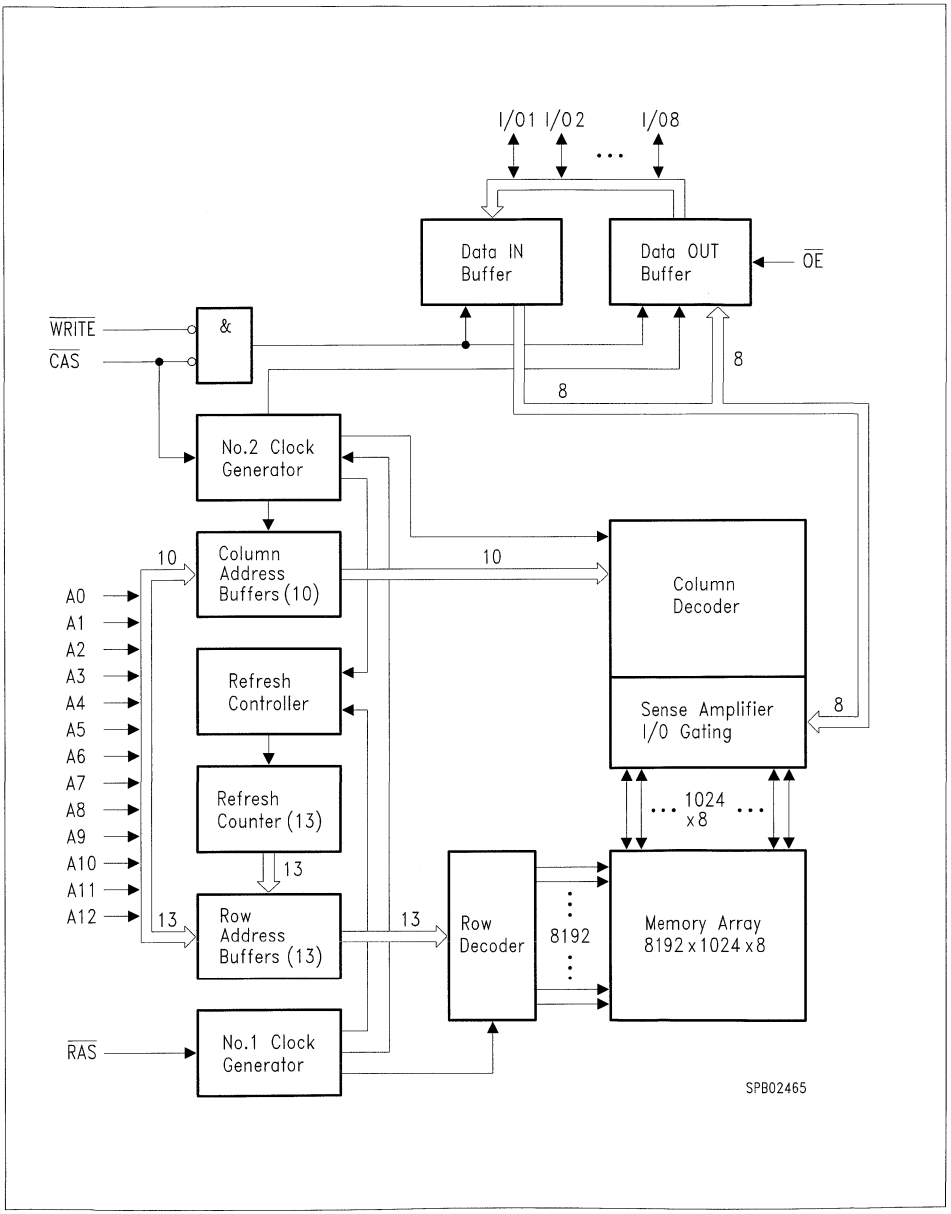
P-SOJ-34-1 (500 mil)
P-TSOPII-34-1 (500 mil)



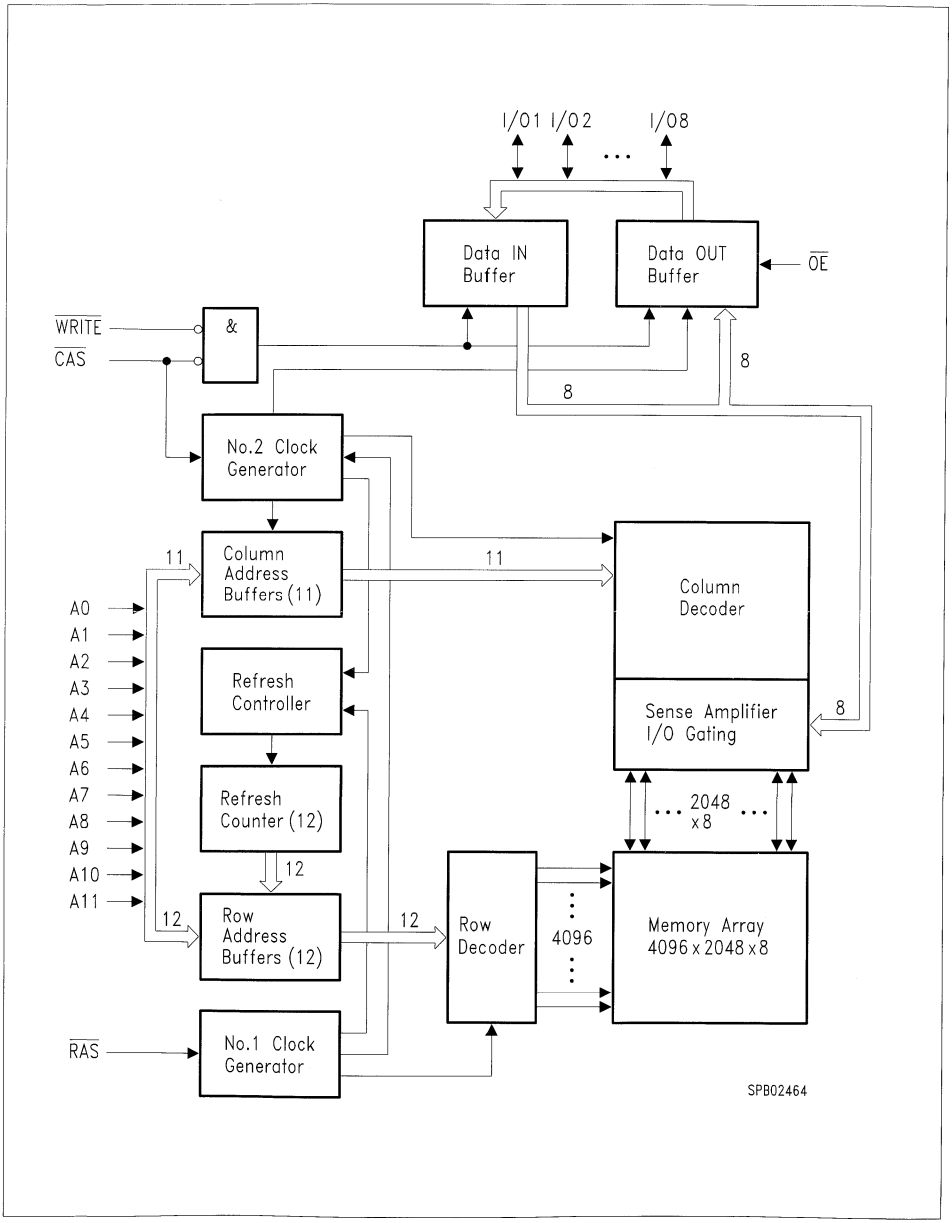
* Pin 25 is A12 for HYB 3164800J/T and N.C. for HYB 3165800J/T

TRUTH TABLE

FUNCTION		RAS	CAS	WRITE	OE	ROW ADDR	COL ADDR	I/O1-I/O8
Standby		H	H - X	X	X	X	X	High Impedance
Read		L	L	H	L	ROW	COL	Data Out
Early-Write		L	L	L	X	ROW	COL	Data In
Delayed-Write		L	L	H - L	H	ROW	COL	Data In
Read-Modify-Write		L	L	H - L	L - H	ROW	COL	Data Out, Data In
Fast Page Mode Read	1st Cycle	L	H - L	H	L	ROW	COL	Data Out
	2nd Cycle	L	H - L	H	L	n/a	COL	Data Out
Fast Page Mode Early Write	1st Cycle	L	H - L	L	X	ROW	COL	Data In
	2nd Cycle	L	H - L	L	X	n/a	COL	Data In
Fast Page Mode RMW	1st Cycle	L	H - L	H - L	L - H	ROW	COL	Data Out, Data In
	2st Cycle	L	H - L	H - L	L - H	n/a	COL	Data Out, Data In
RAS only refresh		L	H	X	X	ROW	n/a	High Impedance
CAS-before-RAS refresh		H - L	L	H	X	X	n/a	High Impedance
Test Mode Entry		H - L	L	L	X	X	n/a	High Impedance
Hidden Refresh	READ	L-H-L	L	H	L	ROW	COL	Data Out
	WRITE	L-H-L	L	L	X	ROW	COL	Data In



Block Diagram for HYB 3164800J/T



Block Diagram for HYB 3165800J/T

Absolute Maximum Ratings [1]

Operating temperature range ..... to 70 °C
Storage temperature range ..... – 55 to 150 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 0.5 to min (V_{CC} + 0.5,4.6) V
Power supply voltage ..... 0.5 V to 4.6 V
Power dissipation ..... .1.0 W
Data out current (short circuit) ..... 50 mA

DC Characteristics

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 3 V ± 0.3 V, (values in brackets for HYB 3165800J/T)

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
Input high voltage	V_{IH}	2.0	V_{CC} + 0.3	V	2)
Input low voltage	V_{IL}	– 0.3	0.8	V	2)
Output high voltage (LVTTL) Output „H" level voltage (Iout = – 2 mA)	V_{OH}	2.4	–	V	
Output low voltage (LVTTL) Output „L"level voltage (Iout = + 2 mA)	V_{OL}	–	0.4	V	
Output high voltage (LVCMOS) Output „H" level voltage (Iout = – 100 uA)	V_{OH}	V_{CC} – 0.2	–	V	6)
Ouput low voltage (LVCMOS) Output „L" level voltage (Iout = +100 uA)	V_{OL}	–	0.2	V	6)
Input leakage current,any input (0 V < V_{in} < V_{CC} , all other pins = 0 V	$I_{I(L)}$	– 2	2	µA	
Output leakage current (DO is disabled, 0 V < V_{out} < V_{CC})	$I_{O(L)}$	– 2	2	µA	
Average V_{cc} supply current: -50 ns version -60 ns version ($\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = t_{RC} min.)	I_{CC1}	 – –	 110 (140) 100 (120)	 mA mA	3) 4) 5)
Standby V_{cc} supply current ($\overline{RAS}$ = $\overline{CAS}$= V_{ih})	I_{CC2}	–	2	mA	–
Average V_{CC} supply current, during RAS-only refresh cycles: -50 ns version -60 ns version (RAS cycling: CAS = V_{IH}: t_{RC} = t_{RC} min.)	I_{CC3}	 – –	 110 (140) 100 (120)	 mA mA	3) 5)

DC Characteristics (cont'd)

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 3 V ± 0.3 V, (values in brackets for HYB 3165800J/T)

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
Average V_{CC} supply current, during fast page mode: -50 ns version -60 ns version ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling: t_{PC} = t_{PC} min.)	I_{CC4}	– –	85 (85) 75 (75)	mA mA	3) 4) 5)
Standby V_{CC} supply current (RAS = CAS = V_{CC} – 0.2 V)	I_{CC5}	–	200	A	–
Average V_{CC} supply current, during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode: -50 ns version -60 ns version ($\overline{RAS}$, $\overline{CAS}$ cycling: t_{RC} = t_{RC} min.)	I_{CC6}	– –	110 (140) 100 (120)	mA mA	3) 4)
Self Refresh Current Average Power Supply Current during Self Refresh. (CBR cycle with tRAS>TRASSmin, $\overline{CAS}$ held low, $\overline{WE}$ = V_{CC} – 0.2V, Address and Din = V_{CC} – 0.2 V or 0.2 V)	I_{CC7}	–	200	A	

AC Characteristics (Notes: 7,8,9,10)
T_A = 0 to 70 °C, V_{CC} = 3.3 ± 0.3 V

Parameter	Symbol	Limit Values				Unit	Note
		HYB 3164(5)800 J/T-50		HYB 3164(5)800 J/T-60			
		min.	max.	min.	max.		
Random read or write cycle time	t_{RC}	90	–	110	–	ns	11
Read-write cycle time	t_{RWC}	126	–	150	–	ns	
Fast page mode cycle time	t_{PC}	35	–	40	–	ns	11
Fast page mode read-write cycle time	t_{PRWC}	71	–	80	–	ns	11
Access time from RAS	t_{RAC}	–	50	–	60	ns	11,12 13,18
Access time from CAS	t_{CAC}	–	13	–	15	ns	11,12 18
Access time from column address	t_{AA}	–	25	–	30	ns	11,12 18
Access time from CAS precharge	t_{CPA}	–	30	–	35	ns	11 18
CAS to output in low-Z	t_{CLZ}	0	–	0	–	ns	18
Output buffer turn-off delay	t_{OFF}	–	13	–	15	ns	20
Transition time (rise and fall)	t_T	3	30	3	30	ns	8
RAS precharge time	t_{RP}	30	–	40	–	ns	
RAS pulse width	t_{RAS}	50	100k	60	100k	ns	11
RAS pulse width (fast page mode)	t_{RASP}	50	200k	60	200k	ns	11
$\overline{CAS}$ precharge to $\overline{RAS}$ Delay (fast page mode)	t_{RHCP}	30	–	35	–	ns	
$\overline{CAS}$ precharge to $\overline{WE}$ (FPM RMW)	t_{CPW}	48	–	55	–	ns	16
RAS hold time	t_{RSH}	13	–	15	–	ns	
CAS hold time	t_{CSH}	50	–	60	–	ns	
CAS pulse width	t_{CAS}	13	100k	15	100k	ns	11
RAS to CAS delay time	t_{RCD}	18	37	20	45		12
RAS to column address delay time	t_{RAD}	13	25	15	30	ns	13
CAS to RAS precharge time	t_{CRP}	5	–	5	–	ns	11

AC Characteristics (Notes: 7,8,9,10)
T_A = 0 to 70 °C, V_{CC} = 3.3 ± 0.3 V

Parameter	Symbol	Limit Values				Unit	Note
		HYB 3164(5)800 J/T-50		HYB 3164(5)800 J/T-60			
		min.	max.	min.	max.		
CAS precharge time	t_{CP}	10	–	10	–	ns	
Row address setup time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	8	–	10	–	ns	
Column address setup time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	10	–	10	–	ns	
Column address to RAS lead time	t_{RAL}	25	–	30	–	ns	11
Read command setup time	t_{RCS}	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	ns	19
Read command hold time referenced to RAS	t_{RRH}	0	–	0	–	ns	
Write command hold time	t_{WCH}	8	–	10	–	ns	
Write command pulse width	t_{WP}	8	–	10	–	ns	
Write command to RAS lead time	t_{RWL}	13	–	15	–	ns	
Write command to CAS lead time	t_{CWL}	13	–	15	–	ns	
Data setup time	t_{DS}	0	–	0	–	ns	17
Data hold time	t_{DH}	10	–	10	–	ns	17
Refresh period for HYB 3164800J/T	t_{REF}	–	128	–	128	ms	
Refresh period for HYB 3165800J/T	t_{REF}	–	64	–	64	ms	
Write command setup time	t_{WCS}	0	–	0	–	ns	16
CAS to WRITE delay time (RMW)	t_{CWD}	31	–	35	–	ns	16
RAS to WRITE delay time (RMW)	t_{RWD}	68	–	80	–	ns	16
Column address to WRITE delay time (RMW)	t_{AWD}	43	–	50	–	ns	16
CAS setup time (CAS-before-RAS cycle)	t_{CSR}	5	–	5	–	ns	
CAS hold time (CAS-before-RAS cycle)	t_{CHR}	10	–	10	–	ns	

AC Characteristics (Notes: 7,8,9,10)
T_A = 0 to 70 °C, V_{CC} = 3.3 ± 0.3 V

Parameter	Symbol	Limit Values				Unit	Note
		HYB 3164(5)800 J/T-50		HYB 3164(5)800 J/T-60			
		min.	max.	min.	max.		
RAS to CAS precharge time	t_{RPC}	5	–	5	–	ns	
CAS precharge time (CAS-before-RAS counter test cycle)	t_{CPT}	25	–	30	–	ns	
Write command setup time (in test mode entry cycle)	t_{WTS}	10	–	10	–	ns	
Write command hold time (in test mode entry cycle)	t_{WTH}	10	–	10	–	ns	
Write to RAS precharge time (CAS-before-RAS cycle)	t_{WRP}	10	–	10	–	ns	
Write hold time referenced to RAS (CAS-before-RAS cycle)	t_{WRH}	10	–	10	–	ns	
OE command hold time	t_{OEH}	13	–	15	–	ns	
OE access time	t_{OEA}	–	13	–	15	ns	11,18
Output buffer turn-off delay from OE	t_{OEZ}	–	13	–	15	ns	20
CAS delay time from Din	t_{DZC}	0	–	0	–	ns	15
Data to OE low delay	t_{DZO}	0	–	0	–	ns	15
CAS high to data delay	t_{CDD}	13	–	15	–	ns	14
OE high to data delay	t_{ODD}	13	–	15	–	ns	14
RAS pulse width during self refresh cycle	t_{RASS}	100k	–	100k	–	ns	21
RAS precharge time during self refresh	t_{RPS}	90	–	110	–		21
CAS hold time during self refresh	t_{CHS}	50	–	50	–	ns	21

Capacitance

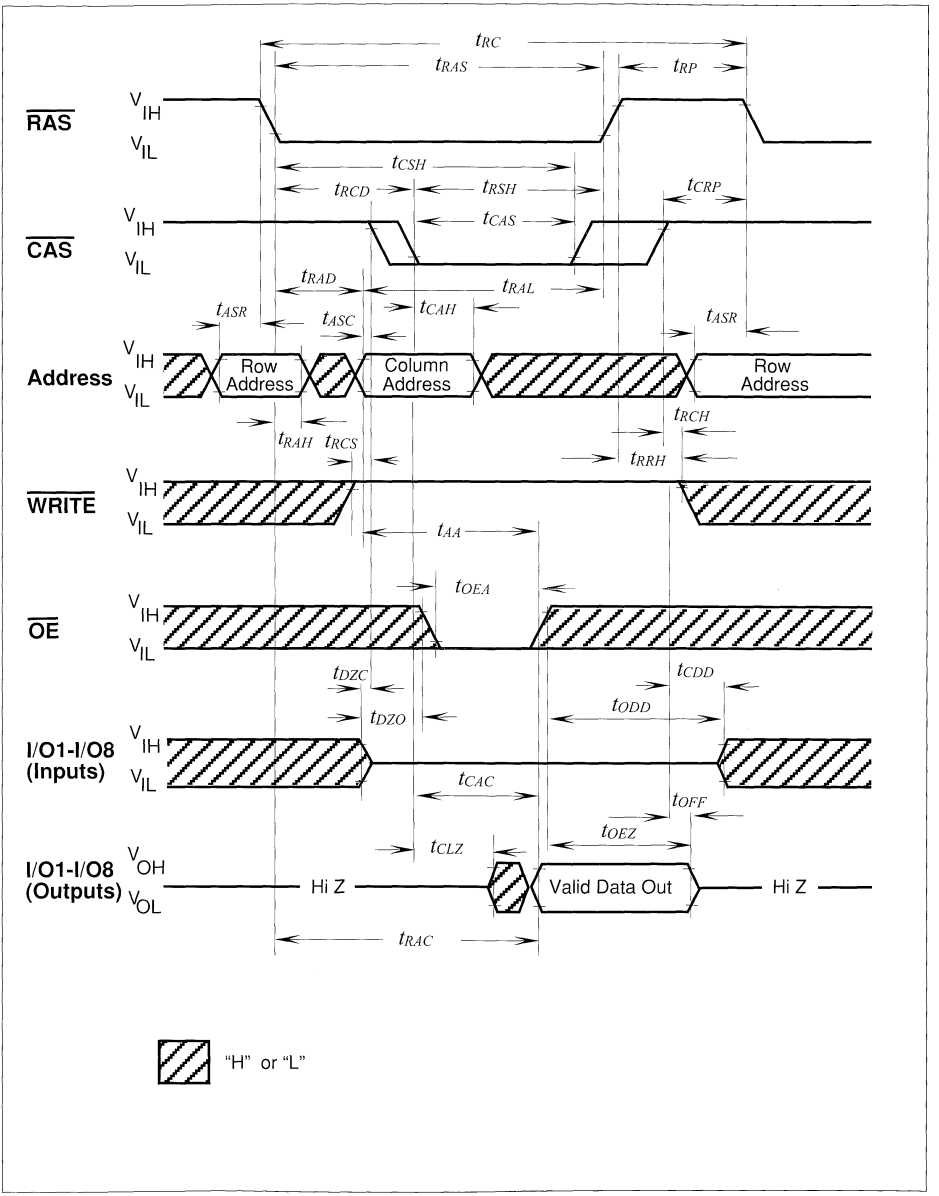
T_A = 0 to 25 °C, V_{CC} = 3.3 V ± 0.3 V, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A11,A12)	C_{I1}	–	5	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	C_{I2}	–	7	pF
I/O capacitance (I/O1-I/O8)	C_{IO}	–	7	pF

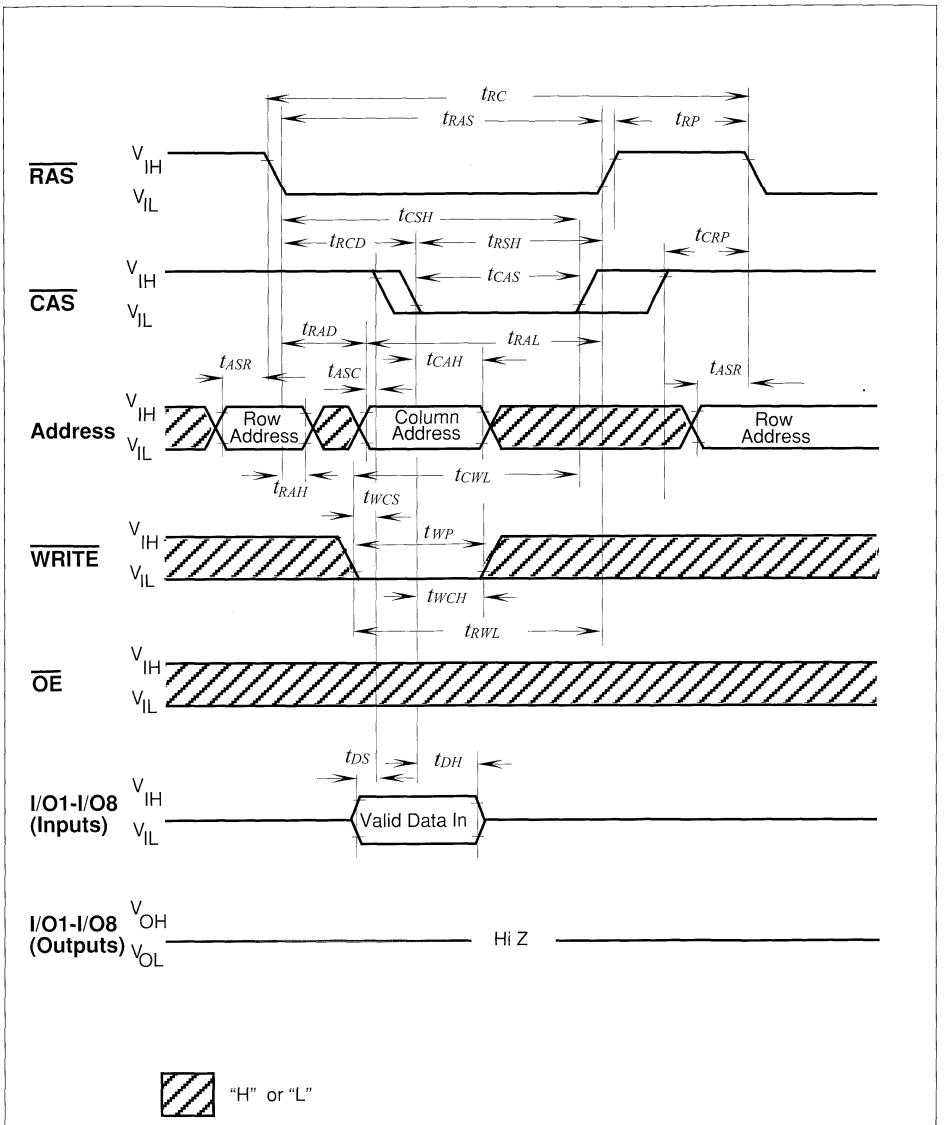
Notes:

1) Stresses greater than listed under „Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ration conditions for extended periods may affect relialibity.
2) All voltages are referenced to V_{SS}.
3) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} and I_{CC7} depend on cycle rate.
4) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.
5) Column address can be changed once or less while RAS = V_{il} and CAS = V_{ih}
6) V_{ol} (LVCMOS) and V_{oh} (LVCMOS) levels are not inteded for use as timing reference levels. LVCMOS levels are the quiescent state of a low impedance output driver, under the specified load conditions.
7) An initial pause of 100 µs is required after power-up followed by 8 $\overline{\text{RAS}}$-only refresh cycles, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ initialization cycles instead of 8 $\overline{\text{RAS}}$ cycles are required.
8) AC measurements assume tT = 5 ns.
9) $V_{IH\ (min.)}$ and $V_{IL\ (max.)}$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
10) Valid column addresses are only A0 through A9 for HYB 3164800 and A0 through A10 for HYB 3165800..
11) In a Test mode Read cylce, the value of t_{RAS}, t_{AA}, t_{CAC} and tCPA are delayed by 5ns, from the specified value. These parameters must be adjusted in Test Mode cycles by adding 5ns to the specified value. Associated timings must also be adjusted by 5ns.
12) Operation within the $t_{RCD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RCD\ (max.)}$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD\ (max.)}$ limit, then access time is controlled by t_{CAC}.
13) Operation within the $t_{RAD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RAD\ (max.)}$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD\ (max.)}$ limit, then access time is controlled by t_{AA}.
15) Either t_{DZC} or t_{DZO} must be satisfied.
16) Either t_{CDD} or t_{ODD} must be satisfied.
16) t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS\ (min.)}$, the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} > t_{RWD\ (min.)}$, $t_{CWD} > t_{CWD\ (min.)}$, $t_{AWD} > t_{AWD\ (min.)}$ and $t_{CPWD} > t_{CPWD\ (min.)}$, the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.
17) These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WRITE}}$ leading edge in Read-Modify-Write cycles.
18) Measured with the specified current load and 100 pF.
19) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
20) $t_{OFF\ (max.)}$ and $t_{OEZ\ (max.)}$ define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.
22) When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:
    If row addresses are being refresh in an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediatly after exit from Self Refresh.
    If row addresses are being refresh in any other manner (ROR - Distributed/Burst or CBR-Burst) over the refresh interval, then a full set of row refreshed must be performed immediately before entry to and immediatey after exit from Self Refresh.

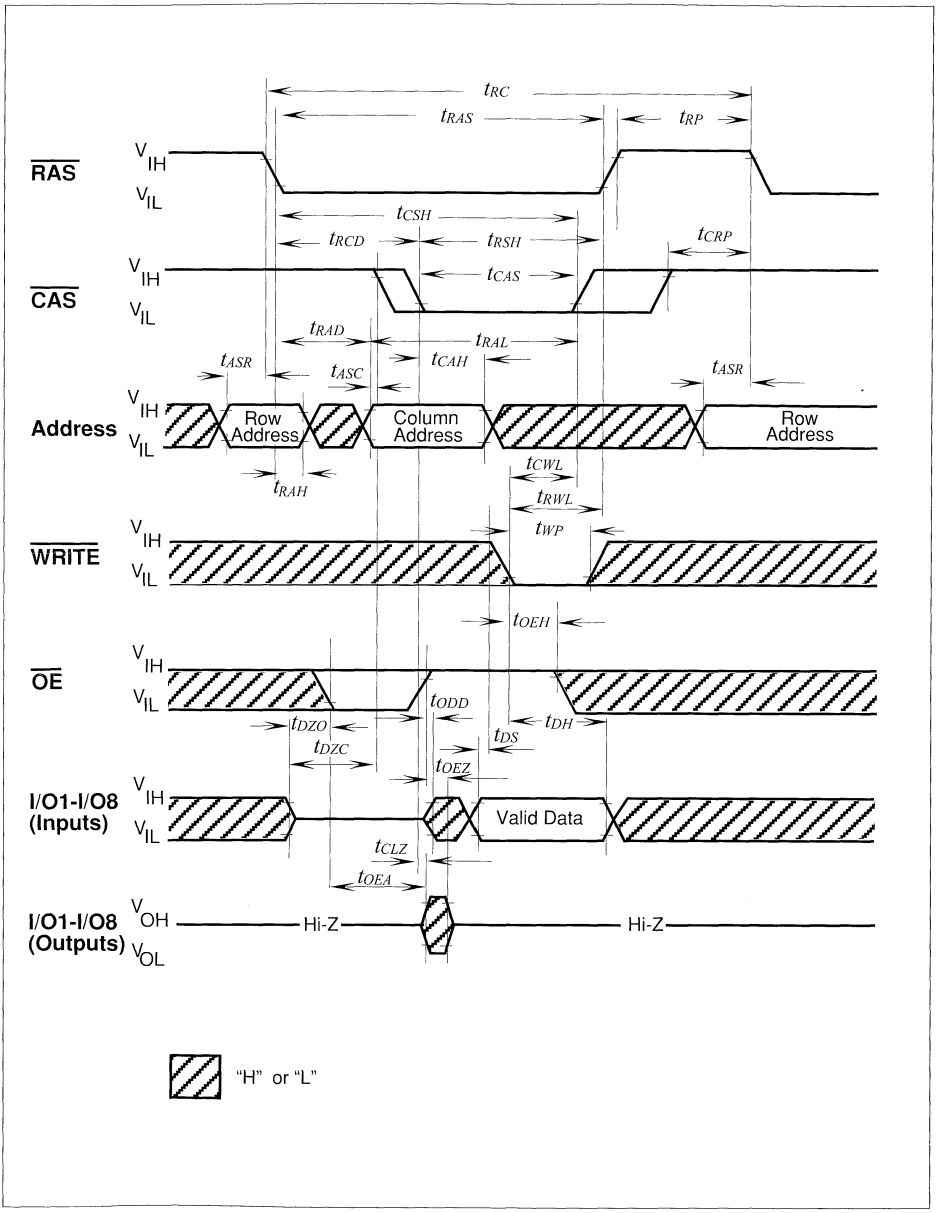
WAVEFORMS



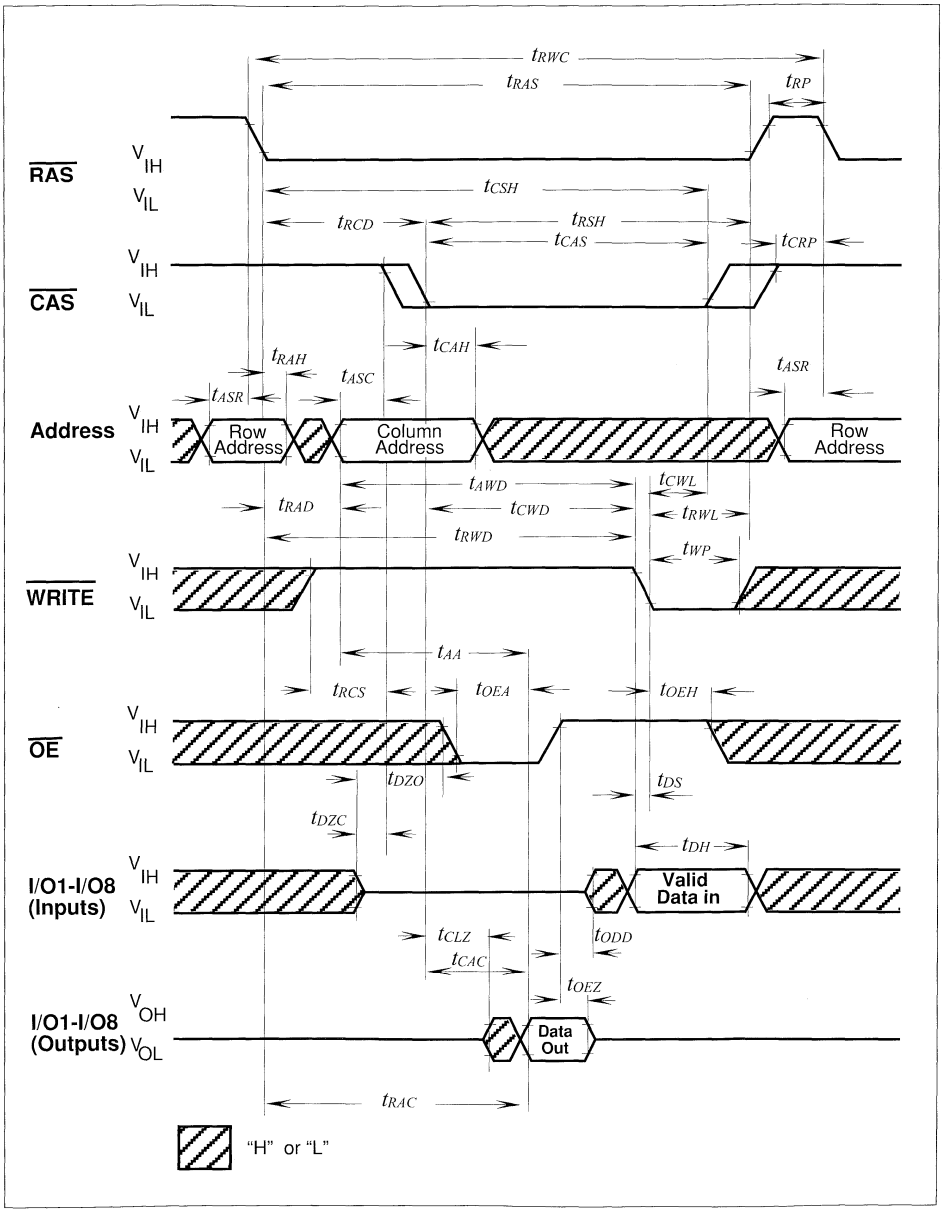
Read Cycle



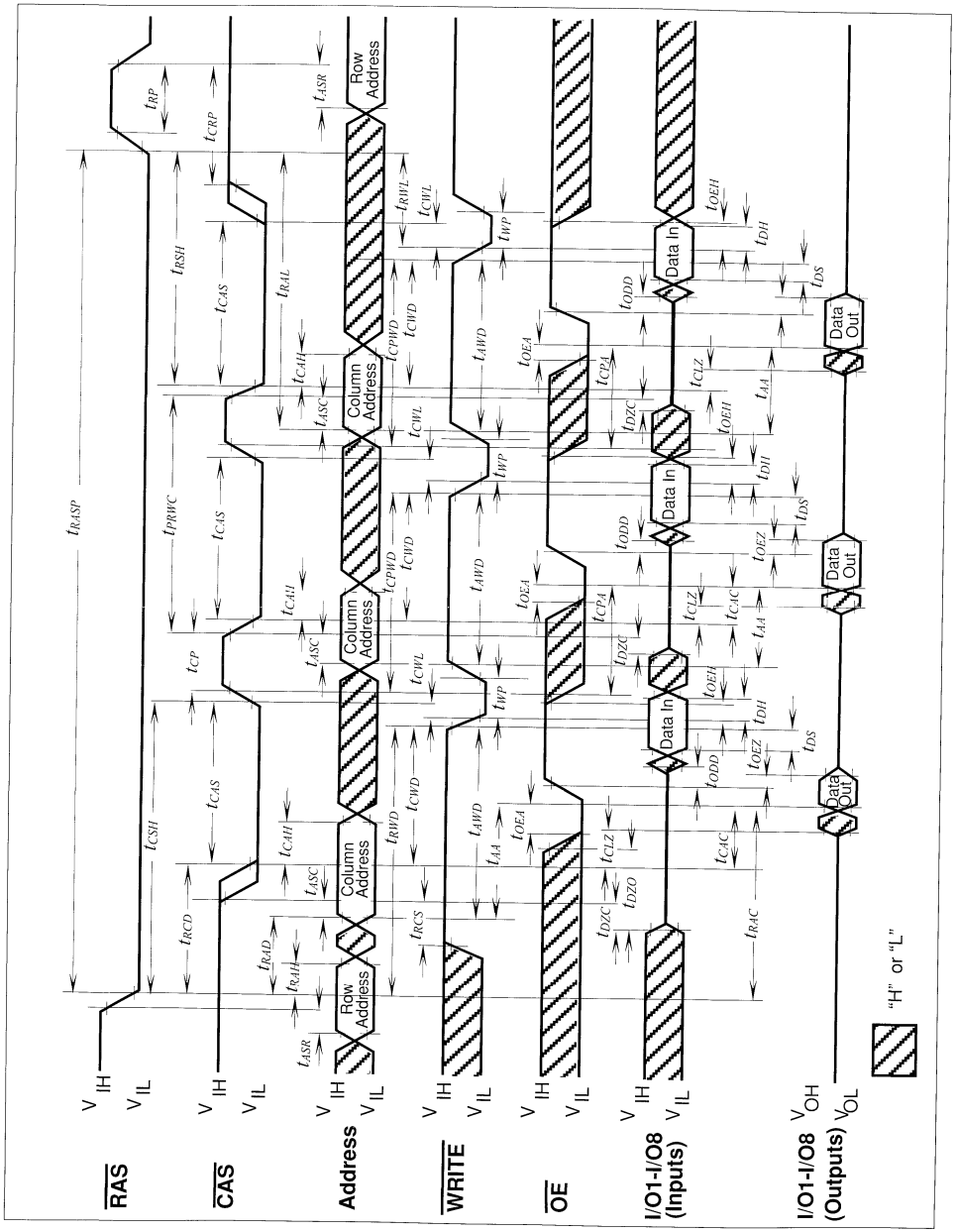
Write Cycle (Early Write)



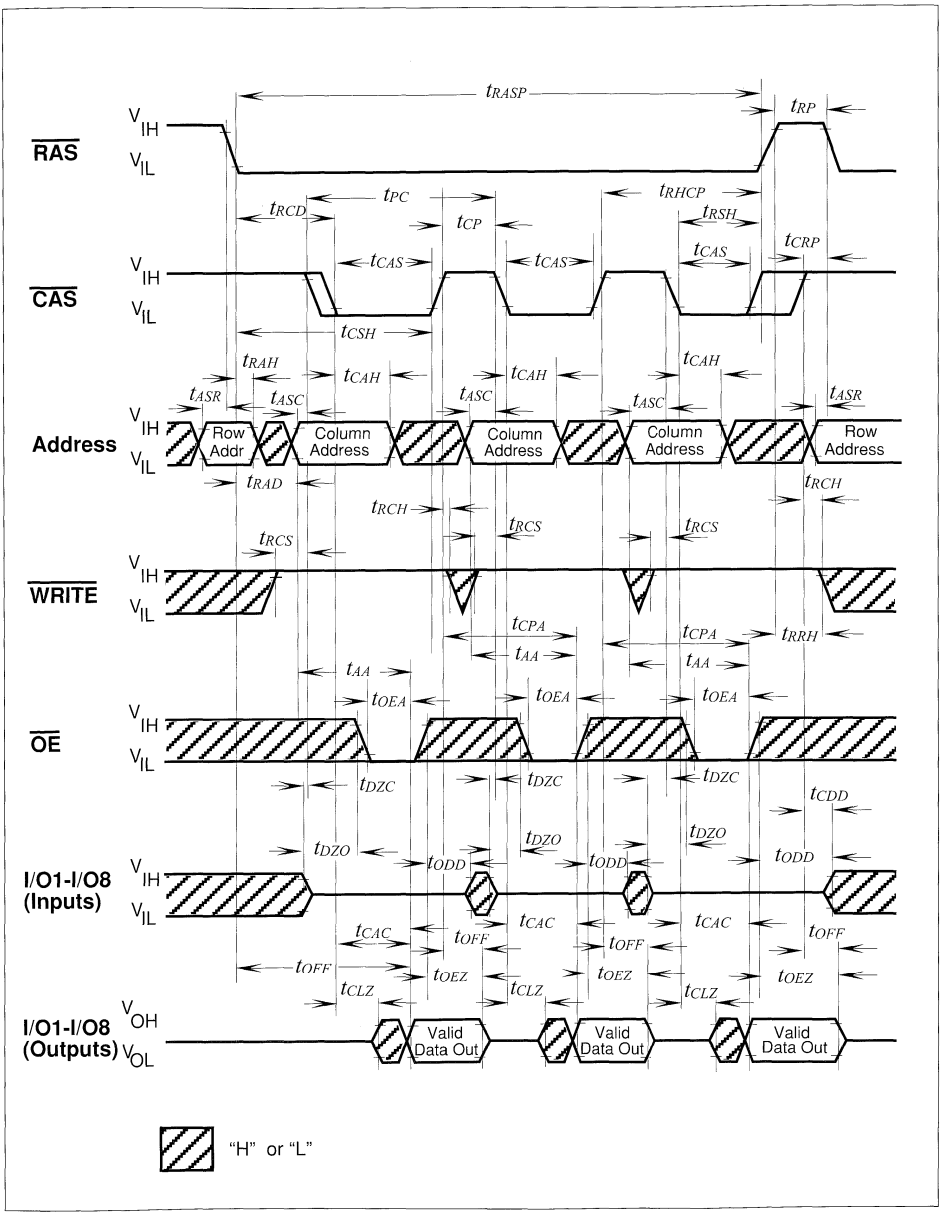
Write Cycle ($\overline{OE}$ Controlled Write)



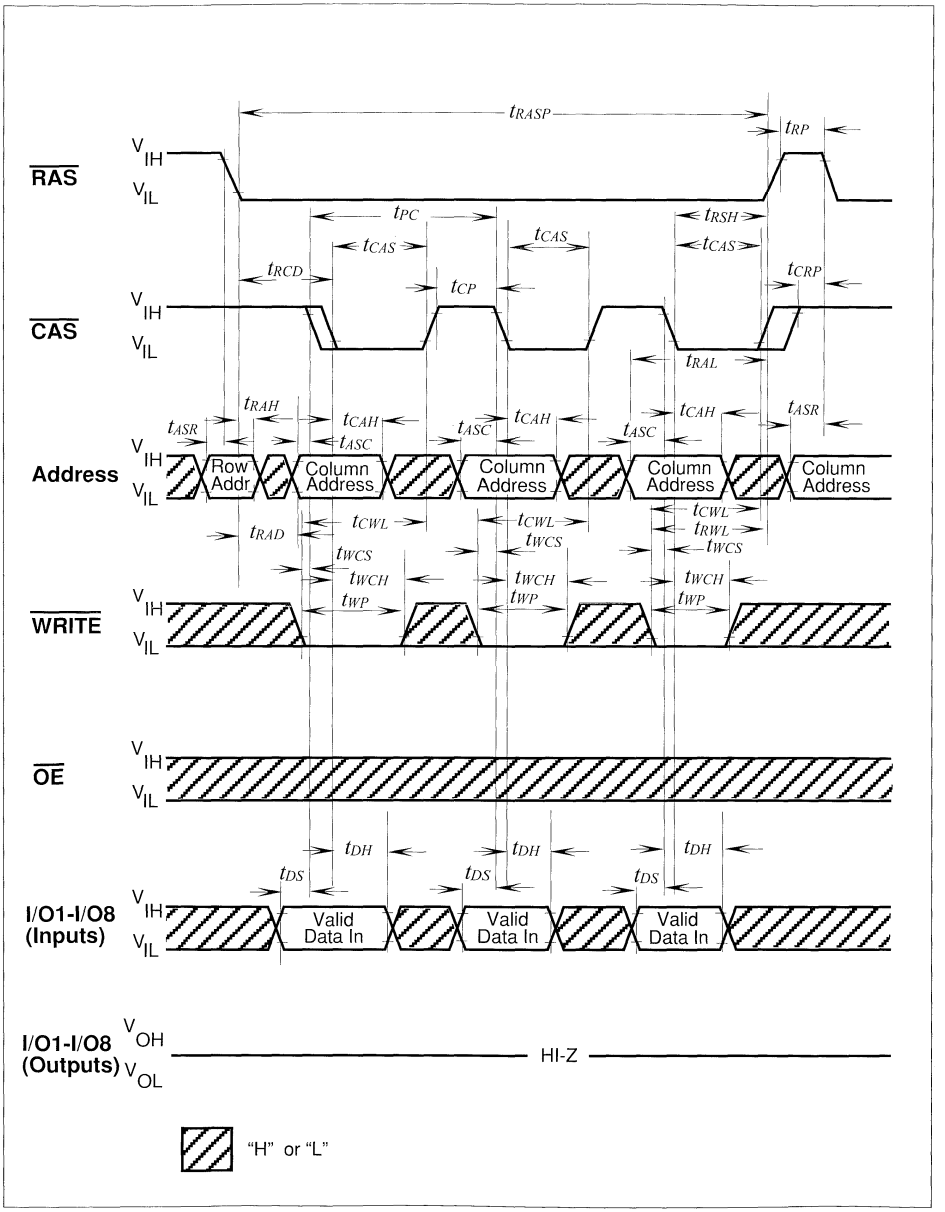
Read-Write (Read-Modify-Write) Cycle



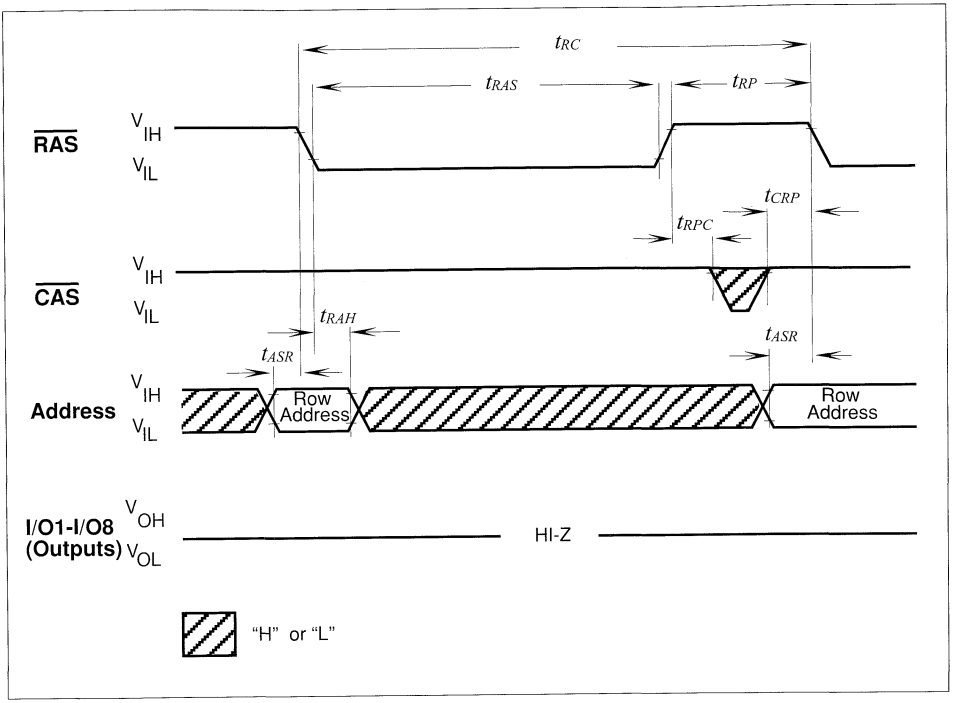
Fast Page Mode Read-Modify-Write Cycle



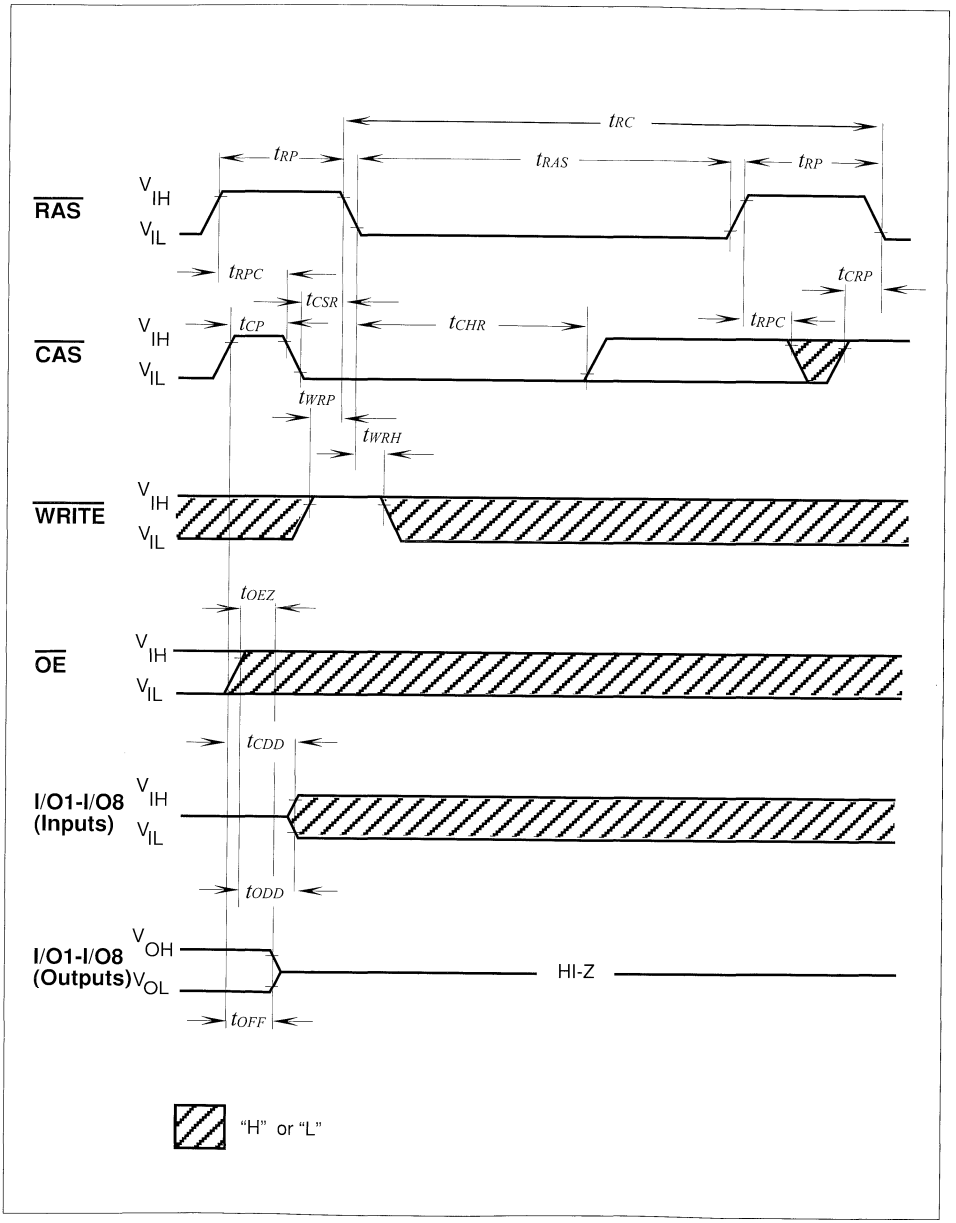
Fast Page Mode Read Cycle



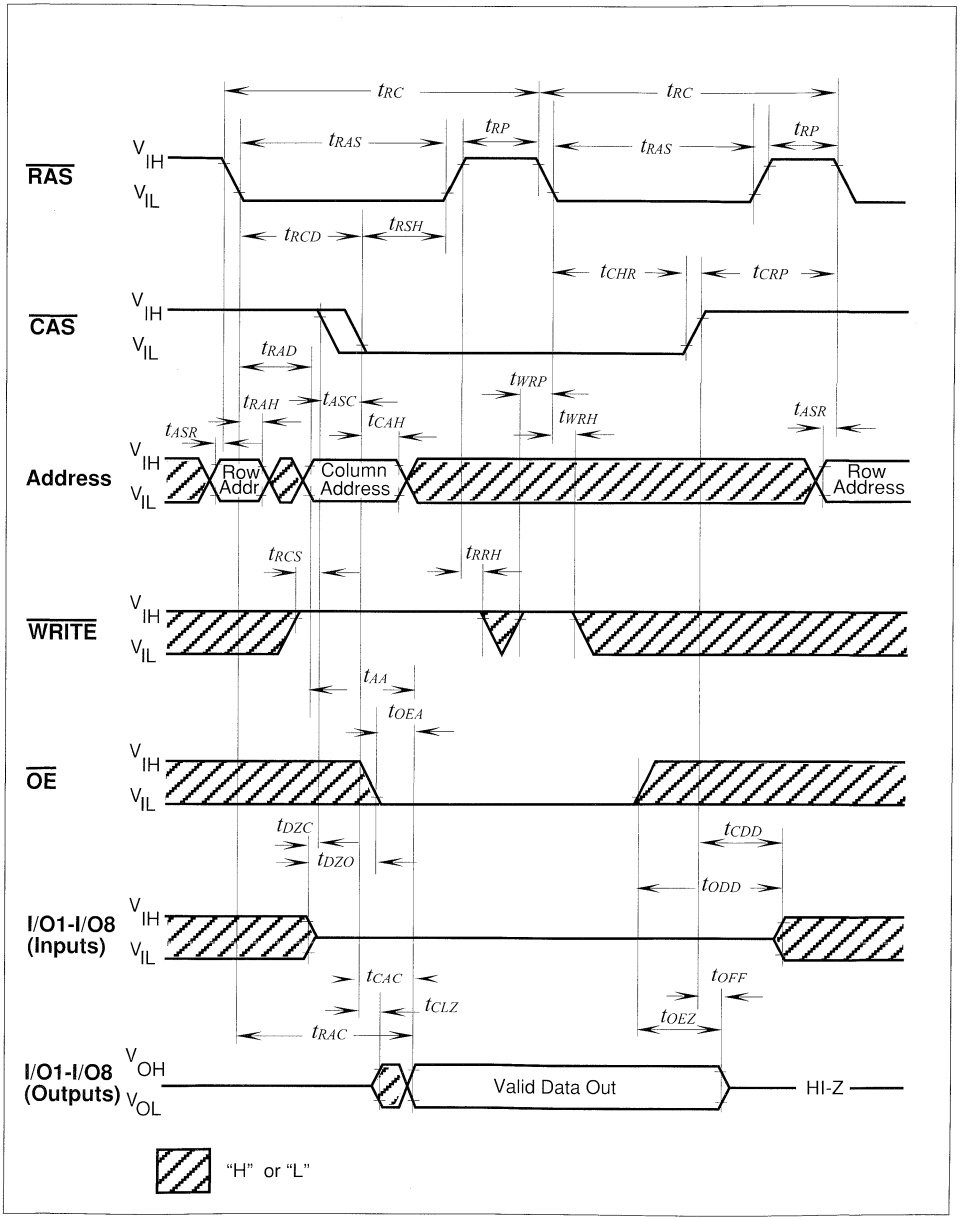
Fast Page Mode Early Write Cycle



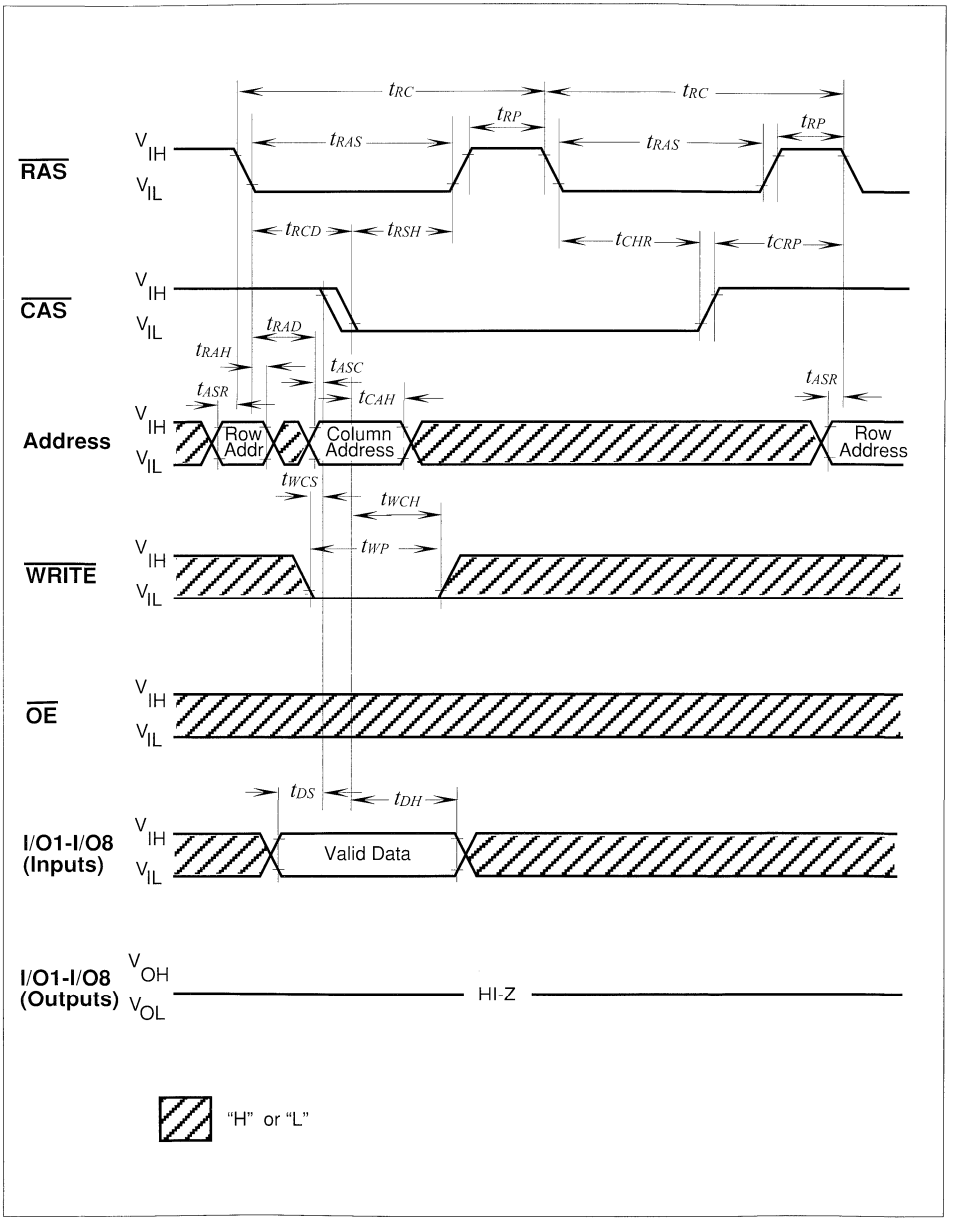
$\overline{RAS}$-Only Refresh Cycle



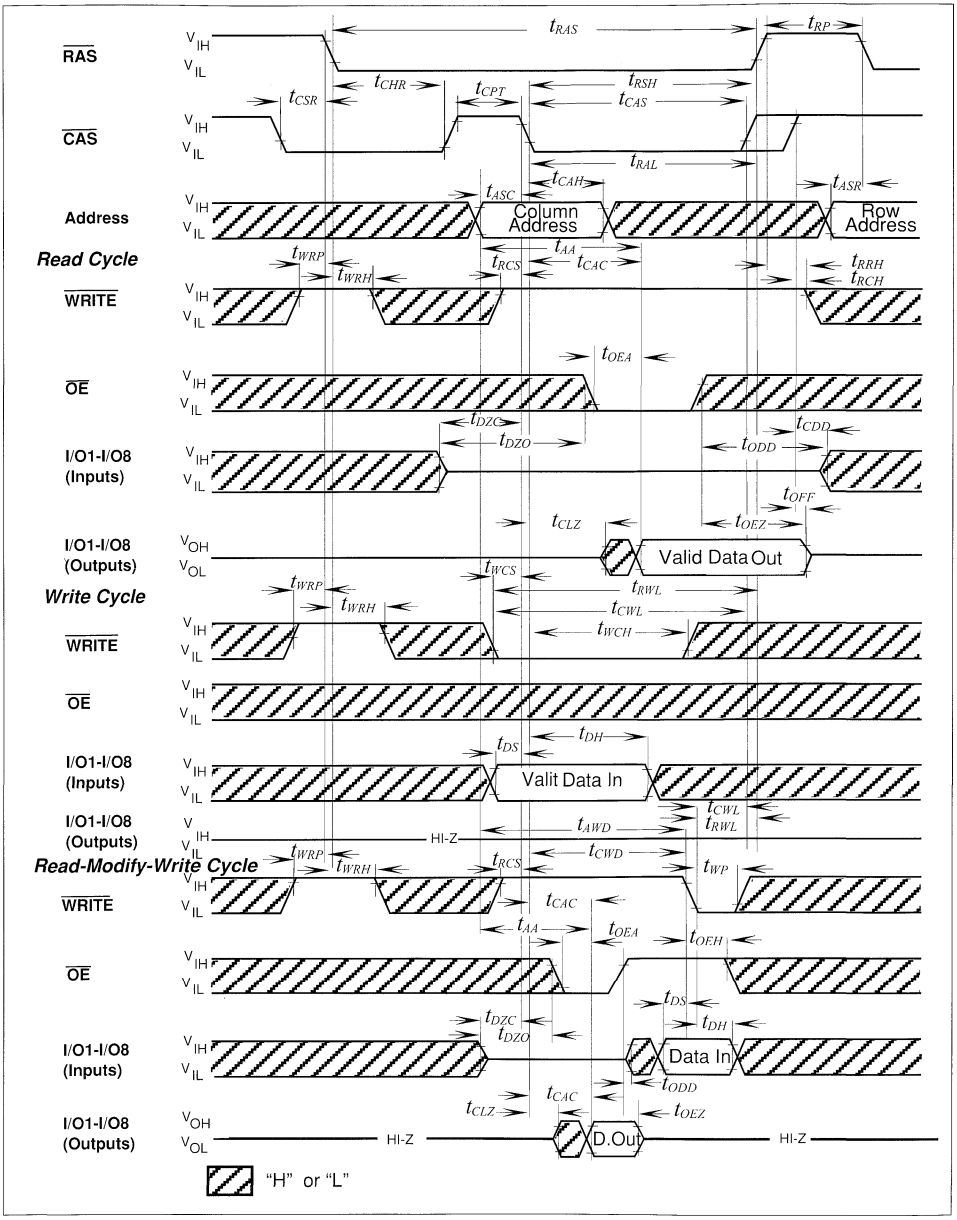
CAS-Before-RAS Refresh Cycle



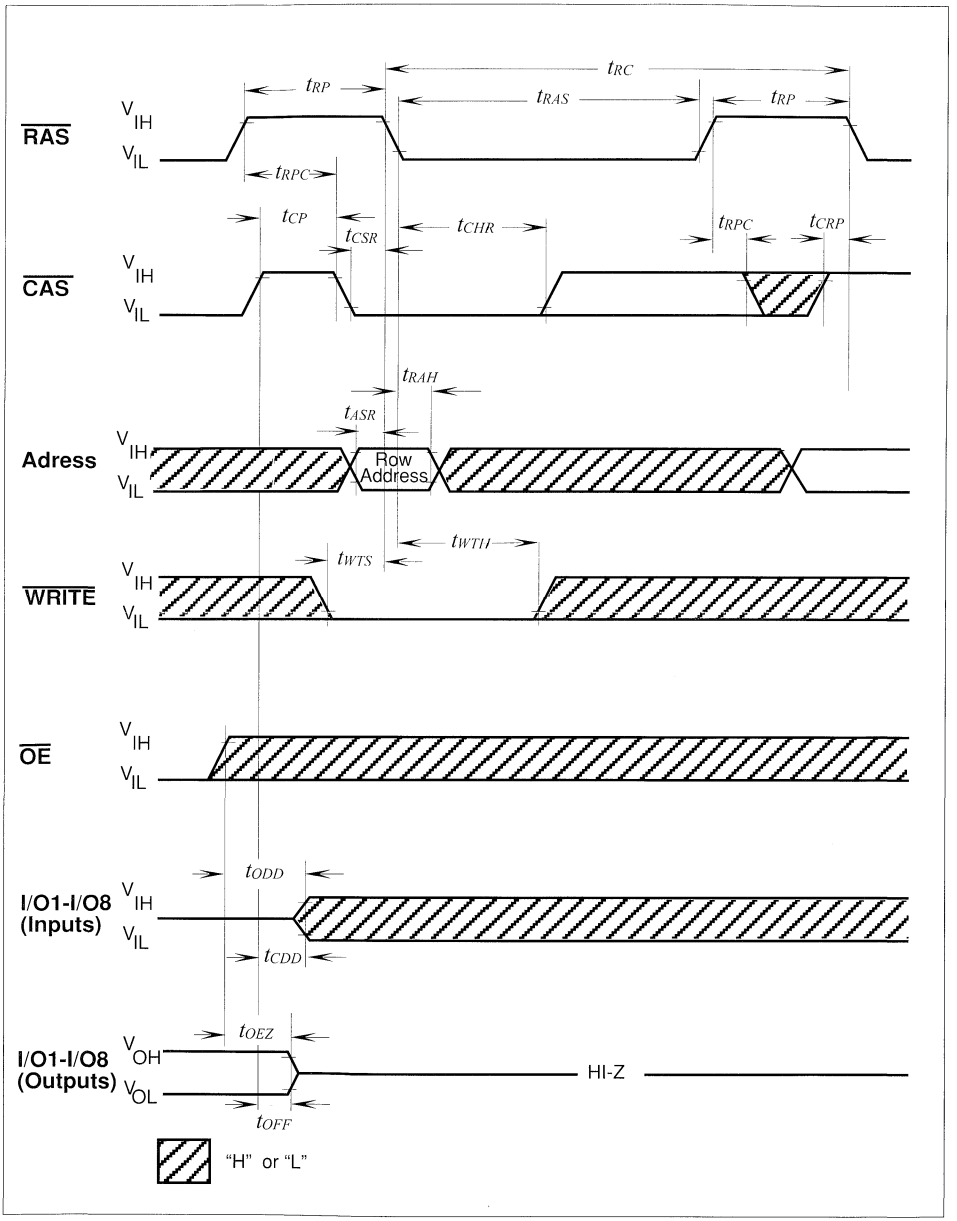
Hidden Refresh Cycle (Read)



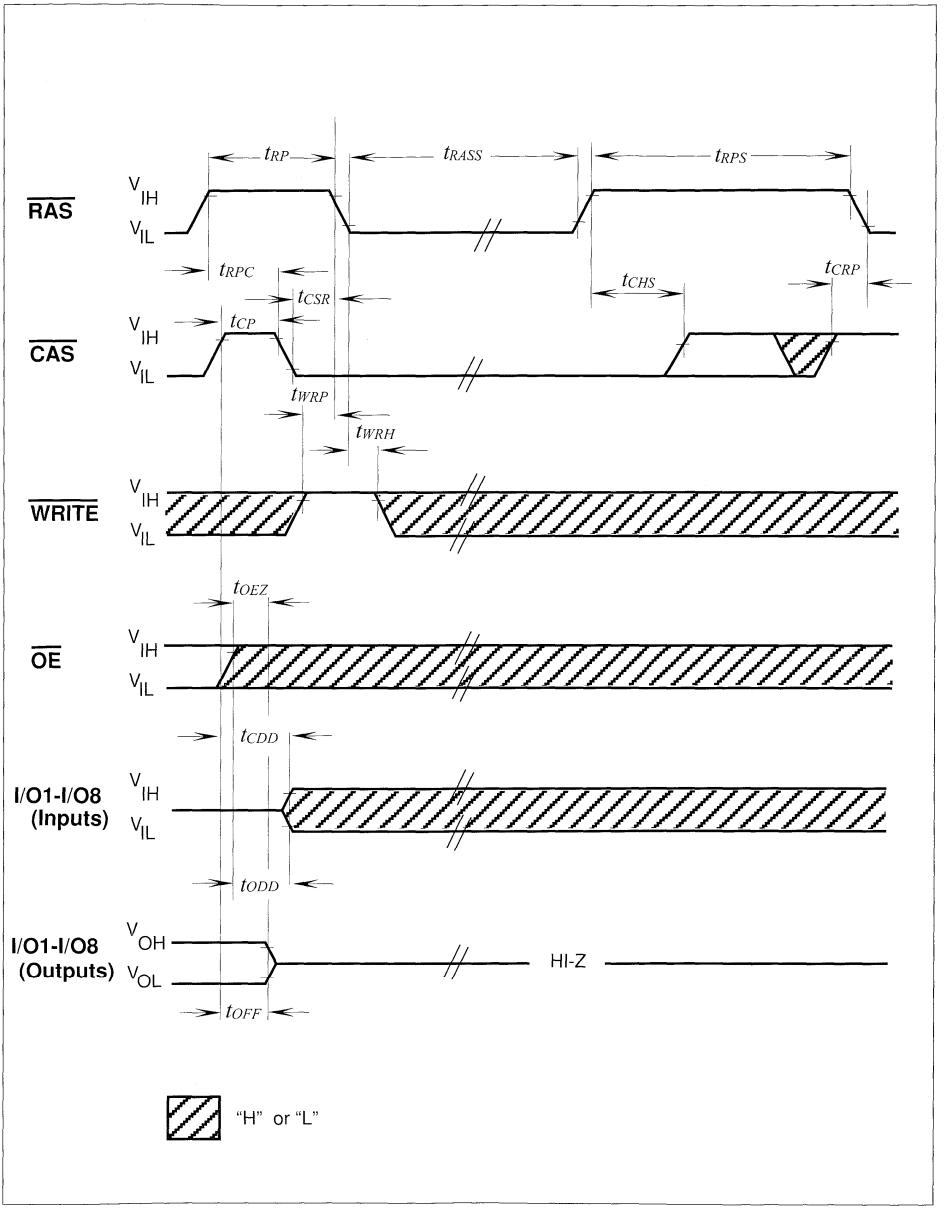
Hidden Refresh Cycle (Early Write)



CAS-Before-RAS Refresh Counter Test Cycle



Test Mode Entry



CAS-before-RAS Self Refresh

4M x 16-Bit Dynamic RAM (4k & 8k Refresh)

HYB 3164160T -50/-60
HYB 3165160T -50/-60

Preliminary Information

- 4 194 304 words by 16-bit organization
- 0 to 70 °C operating temperature
- Fast access and cycle time
  $\overline{RAS}$ access time:
  50 ns (-50 version)
  60 ns (-60 version)
  Cycle time:
  90 ns (-50 version)
  110 ns (-60 version)
  $\overline{CAS}$ access time:
  13 ns (-50 version)
  15 ns (-60 version)
- Fast page mode cycle time
  35 ns (-50 version)
  40 ns (-60 version)
- Single + 3.3 V (± 0.3 V) power supply
- Low power dissipation
  max. 396 active mW (HYB 3164160T-50)
  max. 360 active mW (HYB 3164160T-60)
  max. 504 active mW (HYB 3165160T-50)
  max. 432 active mW (HYB 3165160T-60)
  7.2 mW standby (TTL)
  720 µW standby (MOS)
- Read, write, read-modify-write, $\overline{CAS}$-before-$\overline{RAS}$ refresh (CBR), $\overline{RAS}$-only refresh, hidden refresh and self refresh modes
- Fast page mode capability
- 2 $\overline{CAS}$ / 1 $\overline{WRITE}$ byte control
- 8192 refresh cycles/128 ms ,
  13 R/ 9C addresses (HYB 3164160T)
- 4096 refresh cycles/ 64 ms ,
  12 R/ 10C addresses (HYB 3165160T)
- Plastic Package: P-TSOPII-54-1 500 mil

Ordering Information

Type	Ordering Code	Package		Descriptions
HYB 3164160T-50	on request	P-TSOPII-54-1	500 mil	DRAM (access time 50 ns)
HYB 3164160T-60	on request	P-TSOPII-54-1	500 mil	DRAM (access time 60 ns)
HYB 3165160T-50	on request	P-TSOPII-54-1	500 mil	DRAM (access time 50 ns)
HYB 3165160T-60	on request	P-TSOPII-54-1	500 mil	DRAM (access time 60 ns)

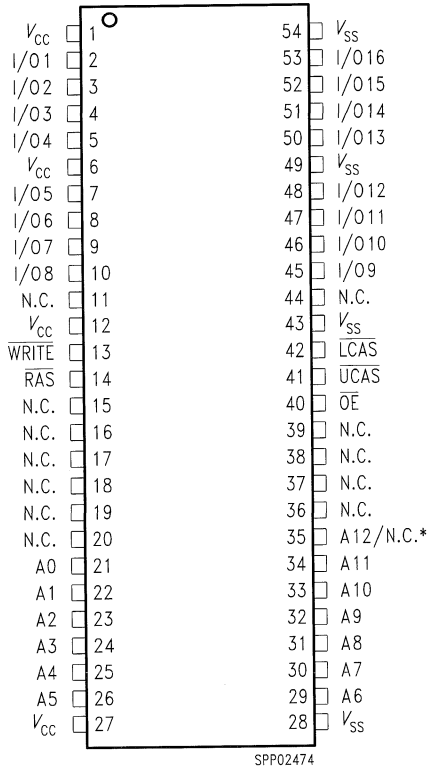
This device is a dynamic RAM organized 4 194 304 by 16 bits. The device is fabricated in SIEMENS/IBM most advanced first generation 64Mbit CMOS silicon gate process technology. The circuit and process design allow this device to achieve high performance and low power dissipation. This DRAM operates with a single 3.3 ± 0.3 V power supply and interfaces with either LVTTL or LVCMOS levels. Multiplexed address inputs permit the HYB 3164(5)160T to be packaged in a 500 mil wide TSOP-54 plastic package. These packages provide high system bit densities and are compatible with commonly used automatic testing and insertion equipment.

Pin Definitions and Functions

Pin No.	Function
A0-A12	Address Inputs for HYB 3164160T
A0-A11	Address Inputs for HYB 3165160T
$\overline{RAS}$	Row Address Strobe
$\overline{OE}$	Output Enable
I/O1-I/O16	Data Input/Output
$\overline{UCAS}$,$\overline{LCAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
Vcc	Power Supply (+ 3.3V)
Vss	Ground

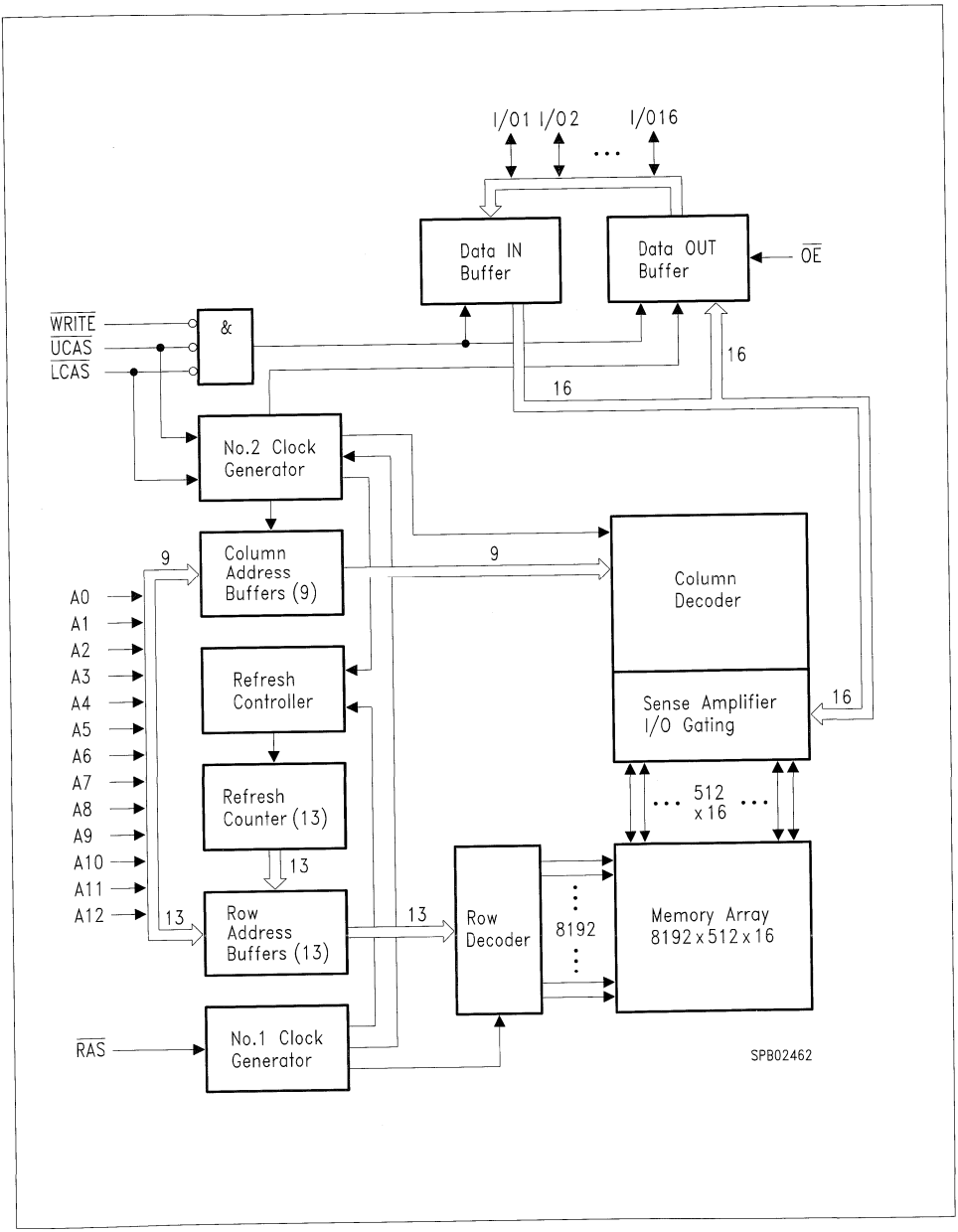
Pin Configuration
(top view)

P-SOJ-54-1 (500 mil)
P-TSOPII-54-1 (500 mil)

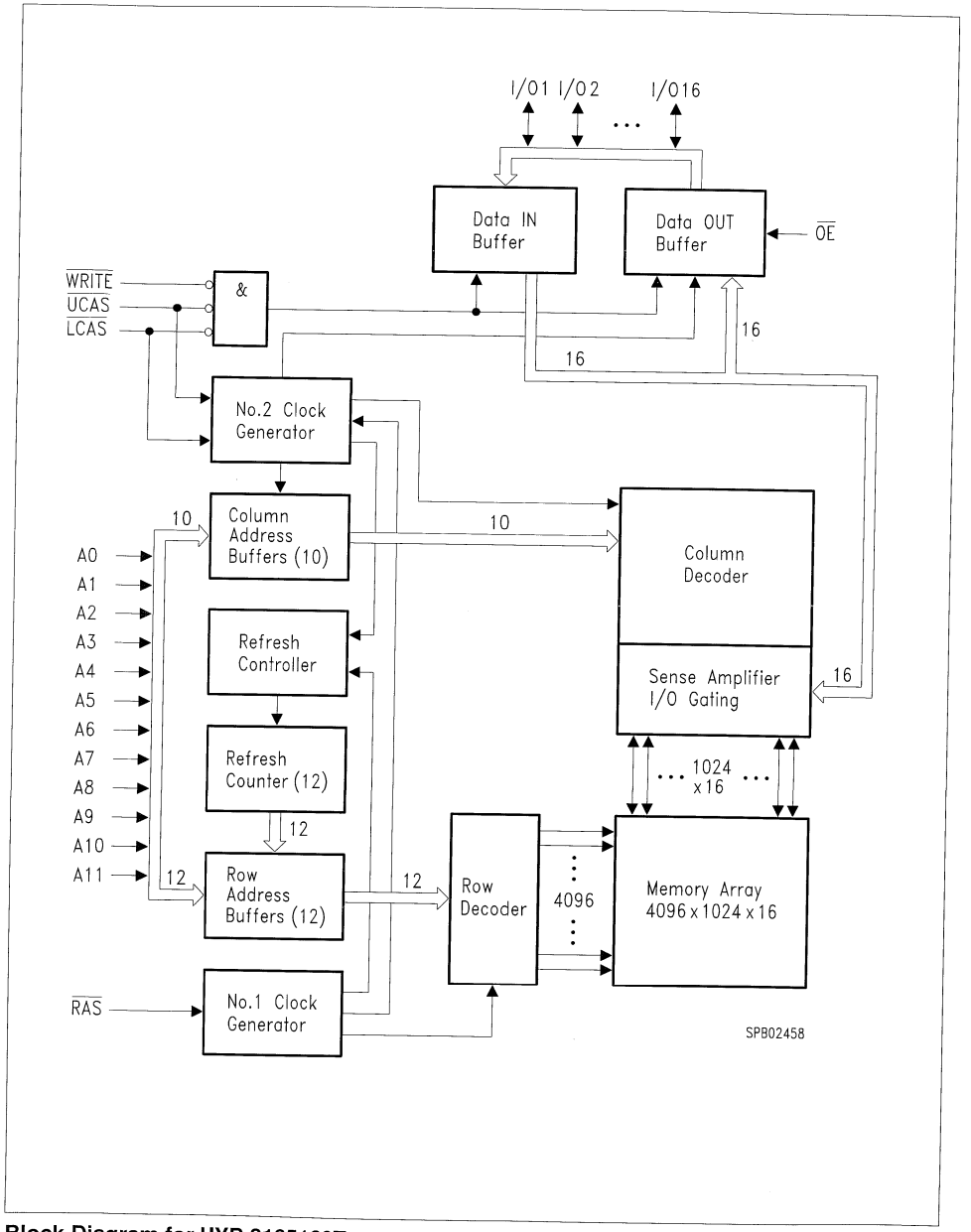


TRUTH TABLE

FUNCTION		RAS	LCAS	UCAS	WRITE	OE	ROW ADD	COL ADD	I/O1-I/O16
Standby		H	H - X	H - X	X	X	X	X	High Impedance
Read:Word		L	L	H	H	L	ROW	COL	Data Out
Read:Lower Byte		L	L	H	H	L	ROW	COL	Lower Byte:Data Out Upper-Byte:High-Z
Read:Upper Byte		L	H	L	H	L	ROW	COL	Lower Byte:High-Z Upper Byte:Data Out
Write:Word (Early-Write)		L	L	L	L	X	ROW	COL	Data In
Write:Lower Byte (Early-Write)		L	L	H	L	X	ROW	COL	Lower Byte:Data Out Upper-Byte:High-Z
Write:Upper Byte (Early Write)		L	H	L	L	X	ROW	COL	Lower Byte:High-Z Upper Byte:Data Out
Read-Modify-Write		L	L	L	H - L	L - H	ROW	COL	Data Out, Data In
Fast Page Mode Read (Word)	1st Cycle	L	H - L	H - L	H	L	ROW	COL	Data Out
Fast Page Mode Read (Word)	2nd Cycle	L	H - L	H - L	H	L	n/a	COL	Data Out
Fast Page Mode Early Write(Word)	1st Cycle	L	H - L	H - L	L	X	ROW	COL	Data In
Fast Page Mode Early Write(Word)	2nd Cycle	L	H - L	H - L	L	X	n/a	COL	Data In
Fast Page Mode RMW	1st Cycle	L	H - L	H - L	H - L	L - H	ROW	COL	Data Out, Data In
Fast Page Mode RMW	2st Cycle	L	H - L	H - L	H - L	L - H	n/a	COL	Data Out, Data In
RAS only refresh		L	H	H	X	X	ROW	n/a	High Impedance
CAS-before-RAS refrosh		H - L	L	L	H	X	X	n/a	High Impedance
Test Mode Entry		H - L	L	L	L	X	X	n/a	High Impedance
Hidden Refresh (Read)		L-H-L	L	L	H	L	ROW	COL	Data Out
Hidden Refresh (Write)		L-H-L	L	L	L	X	ROW	COL	Data In



Block Diagram for HYB 3164160T



Block Diagram for HYB 3165160T

Absolute Maximum Ratings [1)]

Operating temperature range ..... 0 to 70 °C
Storage temperature range ..... – 55 to 150 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 0.5 to min (V_{CC} + 0.5, 4.6) V
Power supply voltage ..... – 0.5 V to 4.6 V
Power dissipation ..... 1.0 W
Data out current (short circuit) ..... 50 mA

DC Characteristics

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 3 V ± 0.3 V, (values in brackets for HYB 3165160T)

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
Input high voltage	V_{IH}	2.0	V_{CC} + 0.3	V	2)
Input low voltage	V_{IL}	– 0.3	0.8	V	2)
Output high voltage (LVTTL) Output „H" level voltage (I_{out} = – 2mA)	V_{OH}	2.4	–	V	
Output low voltage (LVTTL) Output „L"level voltage (I_{out} = + 2mA)	V_{OL}	–	0.4	V	
Output high voltage (LVCMOS) Output „H" level voltage (I_{out} = –100uA)	V_{OH}	V_{CC} – 0.2	–	V	6)
Ouput low voltage (LVCMOS) Output „L" level voltage (I_{out} = +100uA)	V_{OL}	–	0.2	V	6)
Input leakage current,any input (0 V < V_{in} < V_{CC} , all other pins = 0 V	$I_{I(L)}$	– 2	2	µA	
Output leakage current (DO is disabled, 0 V < V_{out} < V_{CC})	$I_{O(L)}$	– 2	2	µA	
Average V_{CC} supply current: -50 ns version -60 ns version ($\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = t_{RC} min.)	I_{CC1}	 – –	 110 (140) 100 (120)	 mA mA	3) 4) 5)
Standby Vcc supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{ih})	I_{CC2}	–	2	mA	–
Average V_{CC} supply current, during RAS-only refresh cycles: -50 ns version -60 ns version (RAS cycling: CAS = V_{IH}: t_{RC} = t_{RC} min.)	I_{CC3}	 – –	 110 (140) 100 (120)	 mA mA	3) 5)

DC Characteristics (cont'd)

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 3 V ± 0.3 V, (values in brackets for HYB 3165160T)

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
Average V_{cc} supply current, during fast page mode: -50 ns version -60 ns version ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling: t_{PC}=t_{PC} min.)	I_{CC4}	– –	85 (85) 75 (75)	mA mA	3) 4) 5)
Standby Vcc supply current ($\overline{RAS}$=$\overline{CAS}$= $V_{cc-0.2V}$)	I_{CC5}	–	200	A	–
Average Vcc supply current, during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode: -50 ns version -60 ns version ($\overline{RAS}$, $\overline{CAS}$ cycling: t_{RC} = t_{RC} min.)	I_{CC6}	– –	110 (140) 100 (120)	mA mA	3) 4)
Self Refresh Current Average Power Supply Current during Self Refresh. ($\overline{CBR}$ cycle with tRAS>TRASSmin, $\overline{CAS}$ held low, $\overline{WE}$ = Vcc-0.2V, Address and Din=Vcc-0.2V or 0.2V)	I_{CC7}	–	200	A	

AC Characteristics (note: 7,8,9,10)
T_A = 0 to 70 °C, V_{CC} = 3.3 ± 0.3 V

Parameter	Symbol	Limit Values				Unit	Note
		HYB 3164(5)160 J/T-50		HYB 3164(5)160 J/T-60			
		min.	max.	min.	max.		
Random read or write cycle time	t_{RC}	90	–	110	–	ns	11
Read-write cycle time	t_{RWC}	126	–	150	–	ns	
Fast page mode cycle time	t_{PC}	35	–	40	–	ns	11
Fast page mode read-write cycle time	t_{PRWC}	71	–	80	–	ns	11
Access time from RAS	t_{RAC}	–	50	–	60	ns	11,12 13,18
Access time from CAS	t_{CAC}	–	13	–	15	ns	11,12 18
Access time from column address	t_{AA}	–	25	–	30	ns	11,12 18
Access time from CAS precharge	t_{CPA}	–	30	–	35	ns	11 18
CAS to output in low-Z	t_{CLZ}	0	–	0	–	ns	18
Output buffer turn-off delay	t_{OFF}	–	13	–	15	ns	20
Transition time (rise and fall)	t_T	3	30	3	30	ns	8
RAS precharge time	t_{RP}	30	–	40	–	ns	
RAS pulse width	t_{RAS}	50	100k	60	100k	ns	11
RAS pulse width (fast page mode)	t_{RASP}	50	200k	60	200k	ns	11
$\overline{CAS}$ precharge to $\overline{RAS}$ Delay (fast page mode)	t_{RHCP}	30	–	35	–	ns	
$\overline{CAS}$ precharge to $\overline{WE}$ (FPM RMW)	t_{CPW}	48	–	55	–	ns	16
RAS hold time	t_{RSH}	13	–	15	–	ns	
CAS hold time	t_{CSH}	50	–	60	–	ns	
CAS pulse width	t_{CAS}	13	100k	15	100k	ns	11
RAS to CAS delay time	t_{RCD}	18	37	20	45		12
RAS to column address delay time	t_{RAD}	13	25	15	30	ns	13
CAS to RAS precharge time	t_{CRP}	5	–	5	–	ns	11

AC Characteristics(cont'd)(note: 7,8,9,10)
T_A = 0 to 70 °C, V_{CC} = 3.3 ± 0.3 V

Parameter	Symbol	Limit Values				Unit	Note
		HYB 3164(5)160 J/T-50		HYB 3164(5)160 J/T-60			
		min.	max.	min.	max.		
CAS precharge time	t_{CP}	10	–	10	–	ns	
Row address setup time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	8	–	10	–	ns	
Column address setup time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	10	–	10	–	ns	
Column address to RAS lead time	t_{RAL}	25	–	30	–	ns	11
Read command setup time	t_{RCS}	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	ns	19
Read command hold time referenced to RAS	t_{RRH}	0	–	0	–	ns	
Write command hold time	t_{WCH}	8	–	10	–	ns	
Write command pulse width	t_{WP}	8	–	10	–	ns	
Write command to RAS lead time	t_{RWL}	13	–	15	–	ns	
Write command to CAS lead time	t_{CWL}	13	–	15	–	ns	
Data setup time	t_{DS}	0	–	0	–	ns	17
Data hold time	t_{DH}	10	–	10	–	ns	17
Refresh period for HYB 3164160T	t_{REF}	–	128	–	128	ms	
Refresh period for HYB 3165160T	t_{REF}	–	64	–	64	ms	
Write command setup time	t_{WCS}	0	–	0	–	ns	16
CAS to WRITE delay time (RMW)	t_{CWD}	31	–	35	–	ns	16
RAS to WRITE delay time (RMW)	t_{RWD}	68	–	80	–	ns	16
Column address to WRITE delay time (RMW)	t_{AWD}	43	–	50	–	ns	16
CAS setup time (CAS-before-RAS cycle)	t_{CSR}	5	–	5	–	ns	

AC Characteristics(cont'd)(note: 7,8,9,10)
T_A = 0 to 70 °C, V_{CC} = 3.3 ± 0.3 V

Parameter	Symbol	Limit Values				Unit	Note
		HYB 3164(5)160 J/T-50		HYB 3164(5)160 J/T-60			
		min.	max.	min.	max.		
CAS hold time (CAS-before-RAS cycle)	t_{CHR}	10	–	10	–	ns	
RAS to CAS precharge time	t_{RPC}	5	–	5	–	ns	
CAS precharge time (CAS-before-RAS counter test cycle)	t_{CPT}	25	–	30	–	ns	
Write command setup time (in test mode entry cycle)	t_{WTS}	10	–	10	–	ns	
Write command hold time (in test mode entry cycle)	t_{WTH}	10	–	10	–	ns	
Write to RAS precharge time (CAS-before-RAS cycle)	t_{WRP}	10	–	10	–	ns	
Write hold time referenced to RAS (CAS-before-RAS cycle)	t_{WRH}	10	–	10	–	ns	
OE command hold time	t_{OEH}	13	–	15	–	ns	
OE access time	t_{OEA}	–	13	–	15	ns	11,18
Output buffer turn-off delay from OE	t_{OEZ}	–	13	–	15	ns	20
CAS delay time from Din	t_{DZC}	0	–	0	–	ns	15
Data to OE low delay	t_{DZO}	0	–	0	–	ns	15
CAS high to data delay	t_{CDD}	13	–	15	–	ns	14
OE high to data delay	t_{ODD}	13	–	15	–	ns	14
RAS pulse width during self refresh cycle	t_{RASS}	100k	–	100k	–	ns	21
RAS precharge time during self refresh	t_{RPS}	90	–	110	–		21
CAS hold time during self refresh	t_{CHS}	50	–	50	–	ns	21

Capacitance

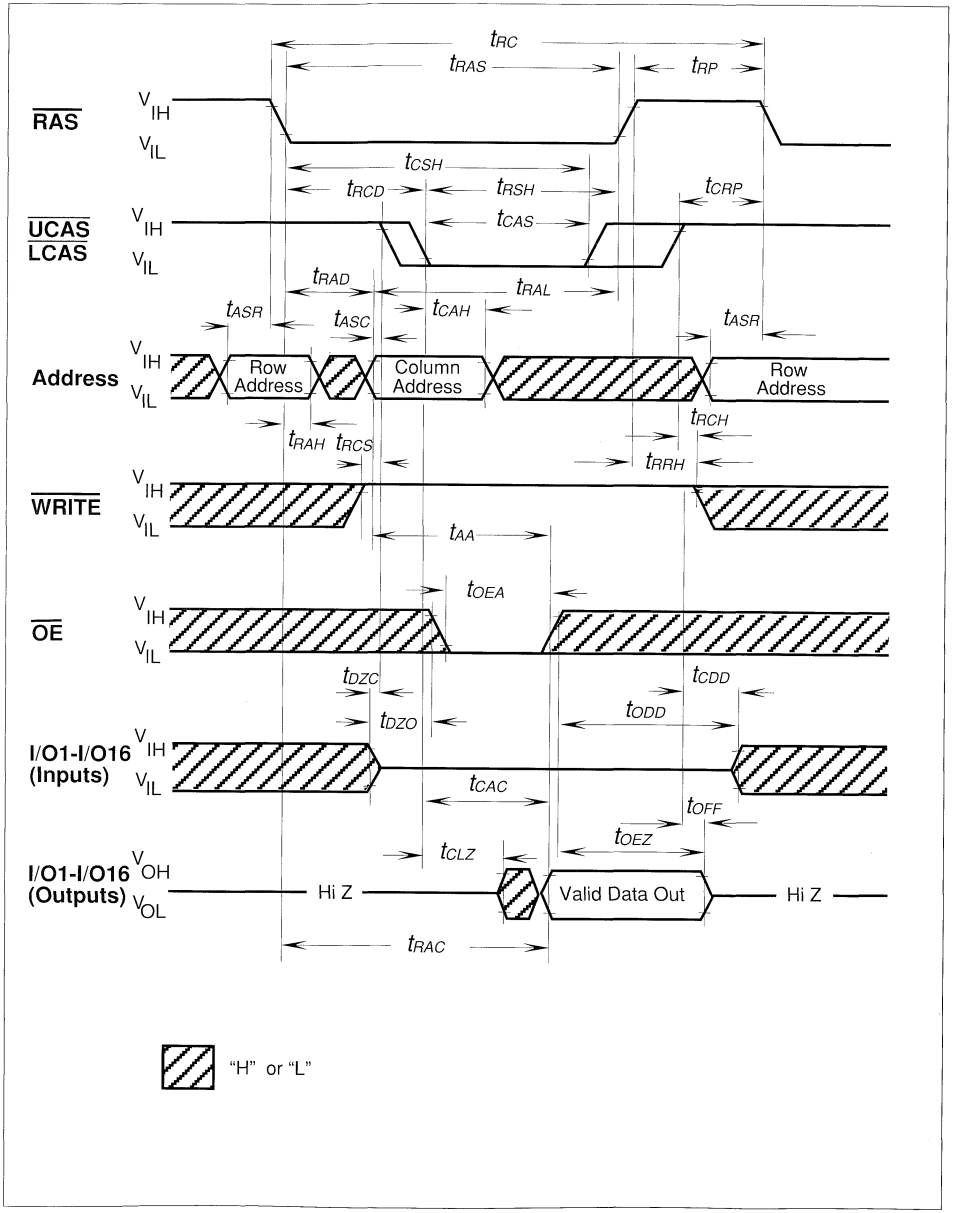
T_A = 0 to 25 °C, V_{CC} = 3.3 V ± 0.3 V, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A11,A12)	C_{I1}	–	5	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	C_{I2}	–	7	pF
I/O capacitance (I/O1-I/O16)	C_{IO}	–	7	pF

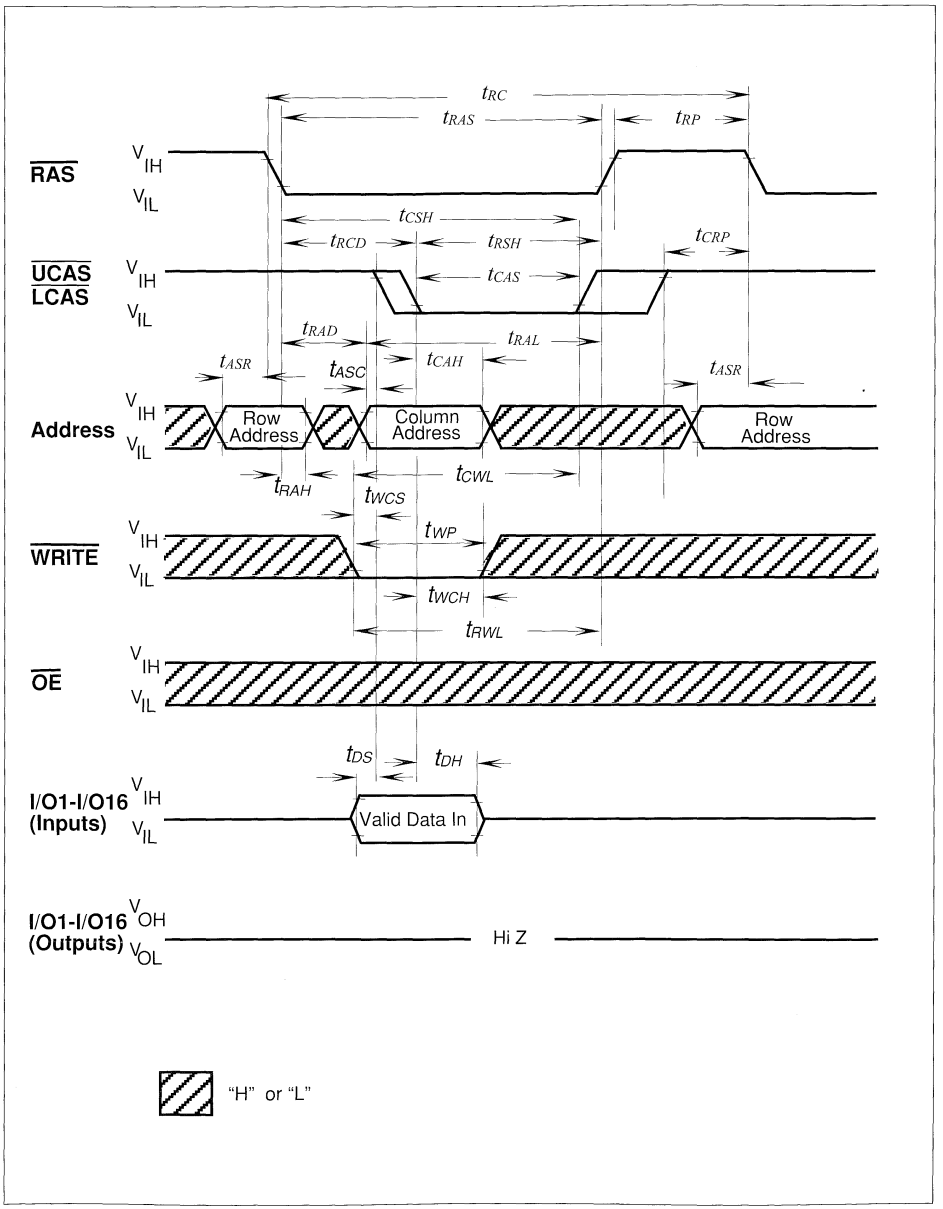
Notes:

1) Stresses greater than listed under „Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ration conditions for extended periods may affect relialibity.
2) All voltages are referenced to V_{SS}.
3) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} and I_{CC7} depend on cycle rate.
4) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.
5) Column address can be changed once or less while RAS = V_{il} and CAS = V_{ih}
6) V_{ol} (LVCMOS) and V_{oh} (LVCMOS) levels are not inteded for use as timing reference levels. LVCMOS levels are the quiescent state of a low impedance output driver, under the specified load conditions.
7) An initial pause of 100 µs is required after power-up followed by 8 $\overline{\text{RAS}}$-only refresh cycles , before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ initialization cycles instead of 8 $\overline{\text{RAS}}$ cycles are required.
8) AC measurements assume t_T = 5 ns.
9) $V_{IH\ (min.)}$ and $V_{IL\ (max.)}$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
10) Valid column addresses are only A0 through A8 for HYB 3164160 and A0 through A9 for HYB 3165160.
11) In a Test mode Read cylce, the value of t_{RAS}, t_{AA}, t_{CAC} and t_{CPA} are delayed by 5 ns, from the specified value. These parameters must be adjusted in Test Mode cycles by adding 5ns to the specified value. Associated timings must also be adjusted by 5 ns.
12) Operation within the $t_{RCD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RCD\ (max.)}$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD\ (max.)}$ limit, then access time is controlled by t_{CAC}.
13) Operation within the $t_{RAD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RAD\ (max.)}$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD\ (max.)}$ limit, then access time is controlled by t_{AA}.
15) Either t_{DZC} or t_{DZO} must be satisfied.
16) Either t_{CDD} or t_{ODD} must be satisfied.
16) t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS\ (min.)}$, the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} > t_{RWD\ (min.)}$, $t_{CWD} > t_{CWD\ (min.)}$, $t_{AWD} > t_{AWD\ (min.)}$ and $t_{CPWD} > t_{CPWD\ (min.)}$, the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.
17) These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WRITE}}$ leading edge in Read-Modify-Write cycles.
18) Measured with the specified current load and 100 pF.
19) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
20) $t_{OFF\ (max.)}$ and $t_{OEZ\ (max.)}$ define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.
22) When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:
    If row addresses are being refresh in an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediatly after exit from Self Refresh.
    If row addresses are being refresh in any other manner (ROR - Distributed/Burst or CBR-Burst) over the refresh interval, then a full set of row refreshed must be performed immediately before entry to and immediatey after exit from Self Refresh.

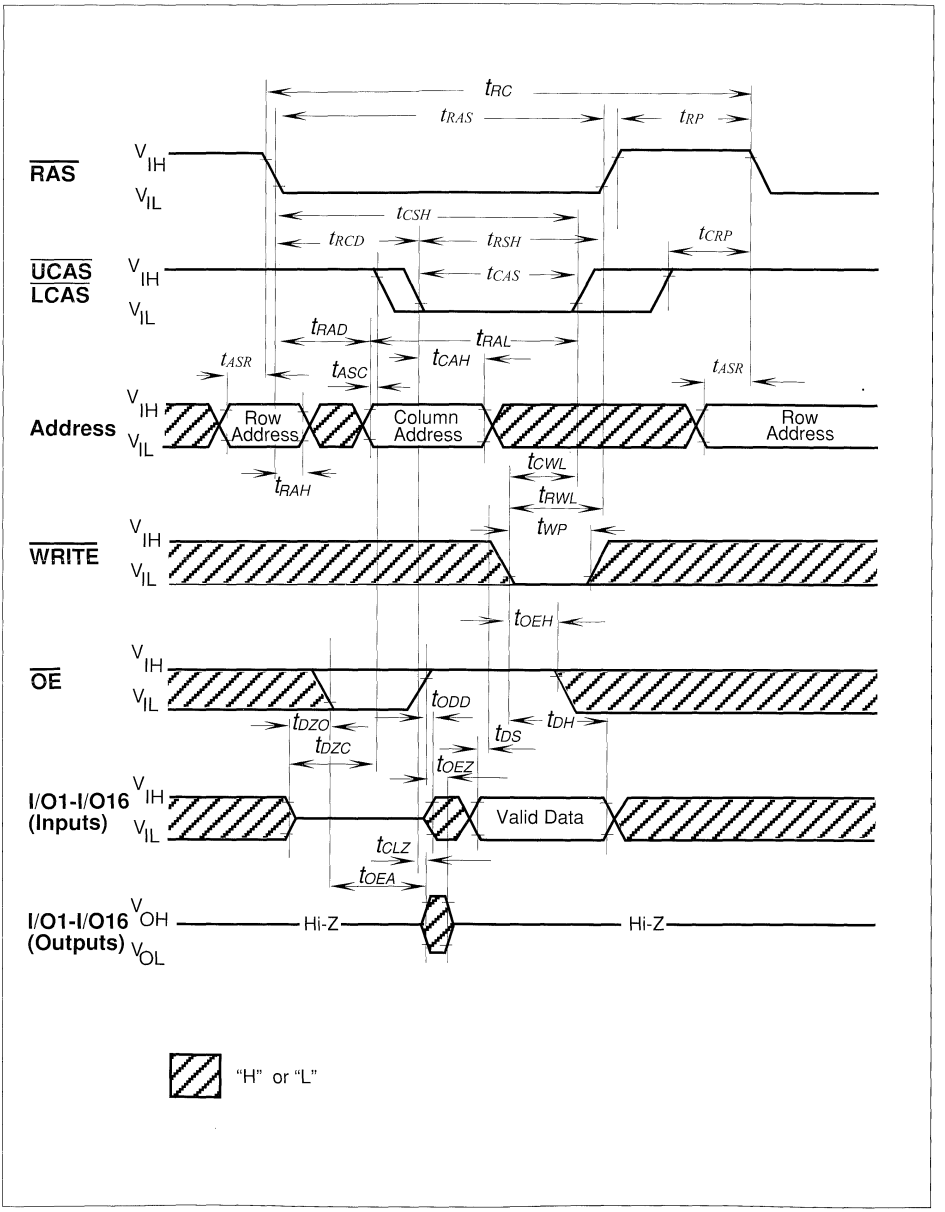
WAVEFORMS



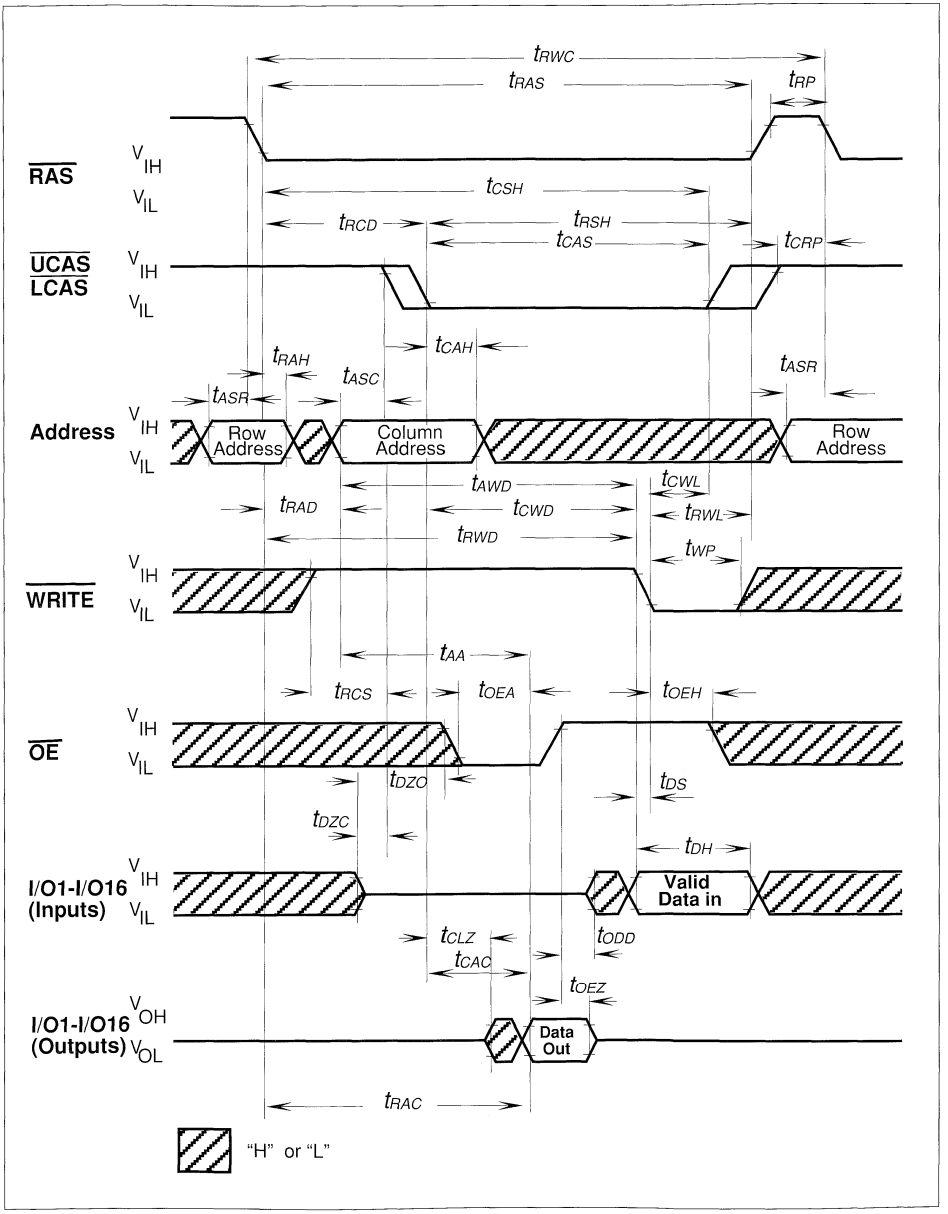
Read Cycle



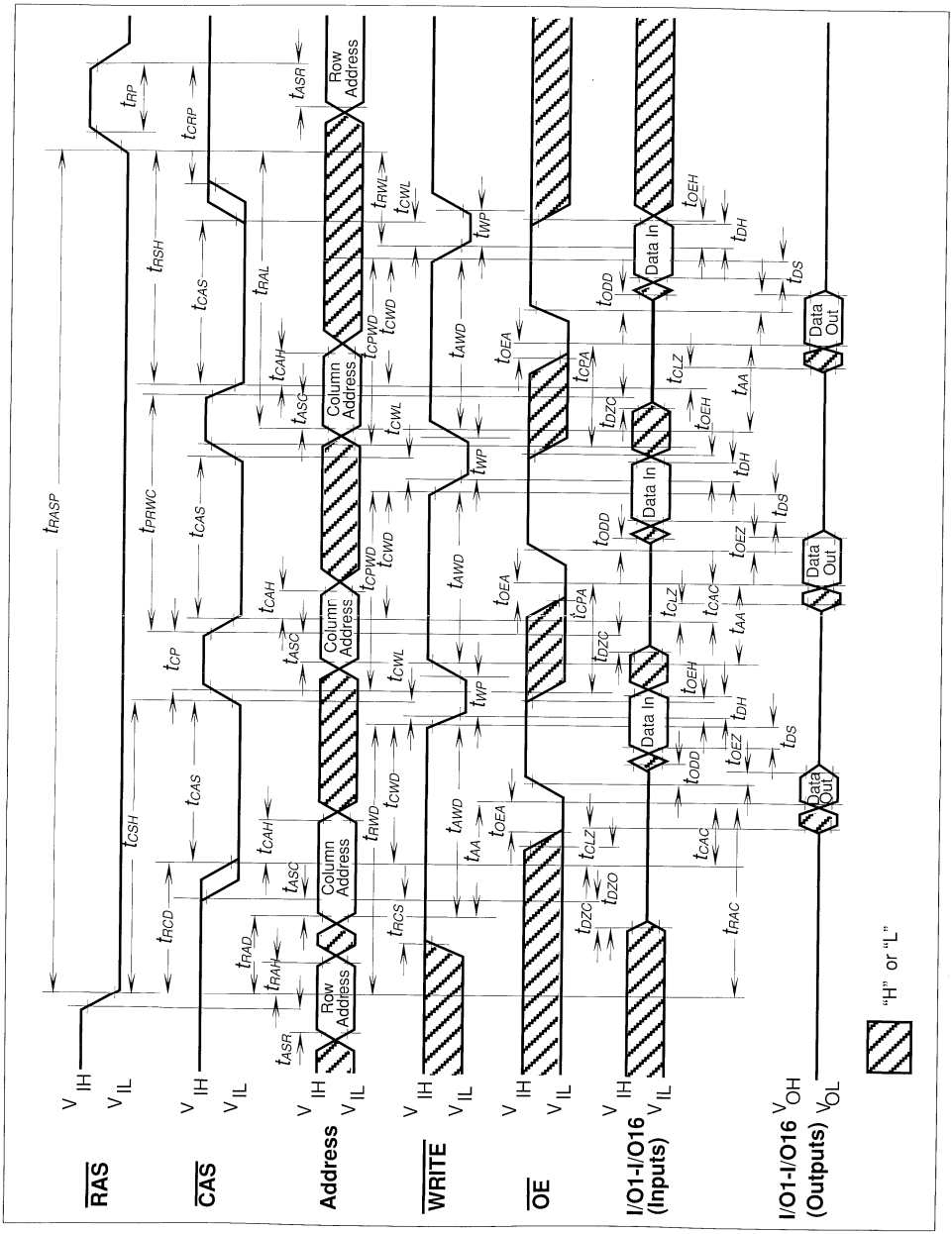
Write Cycle (Early Write)



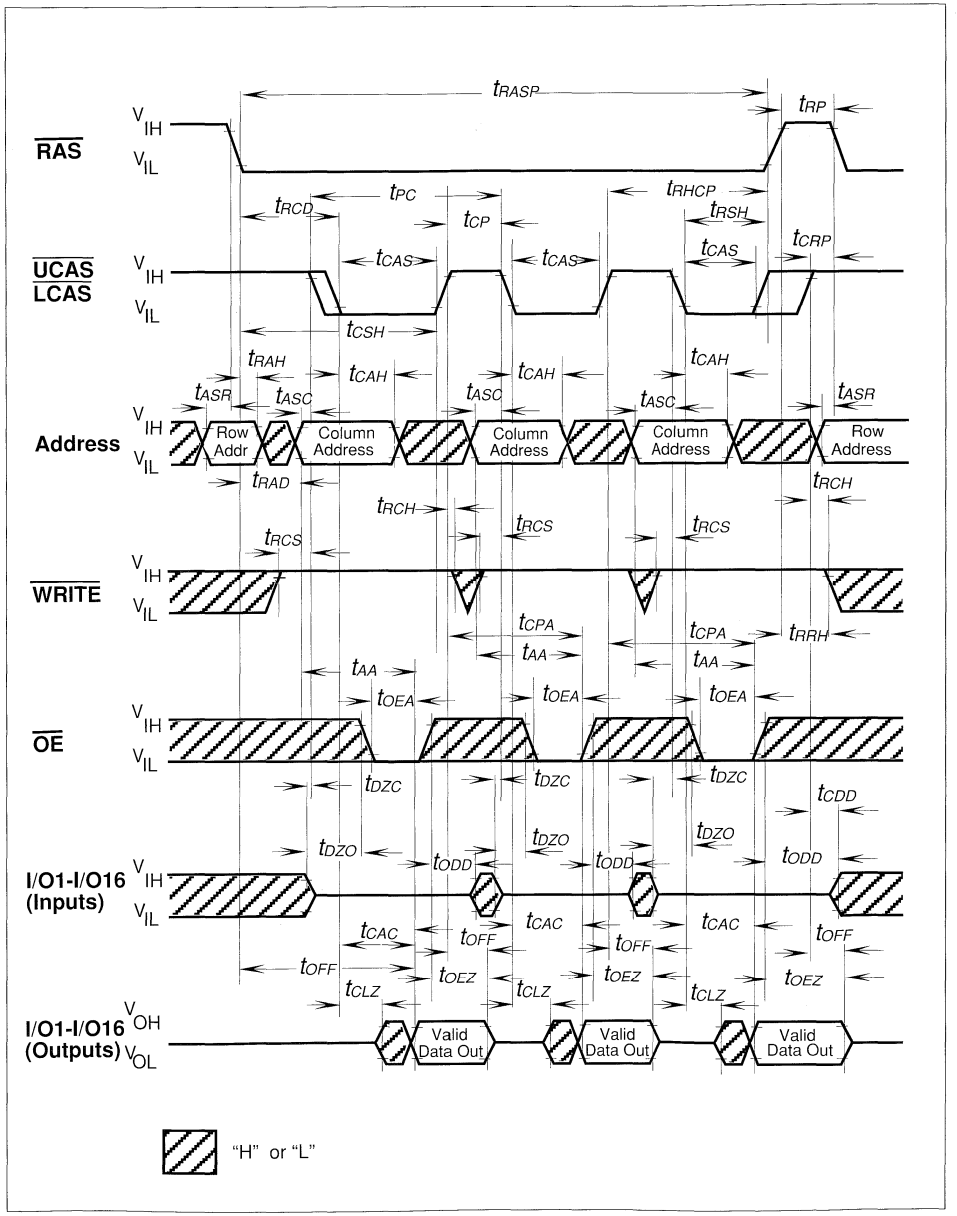
Write Cycle ($\overline{OE}$ Controlled Write)



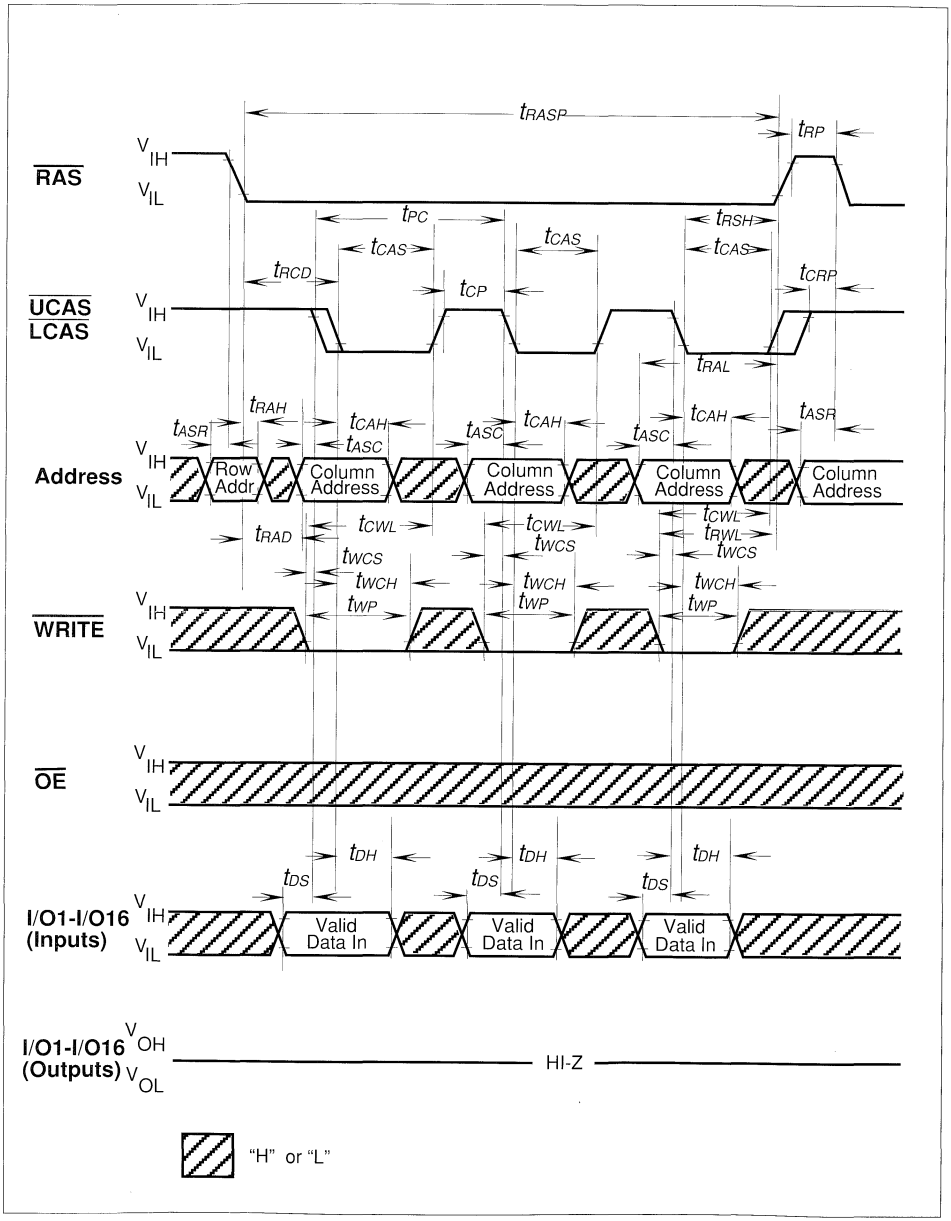
Read-Write (Read-Modify-Write) Cycle



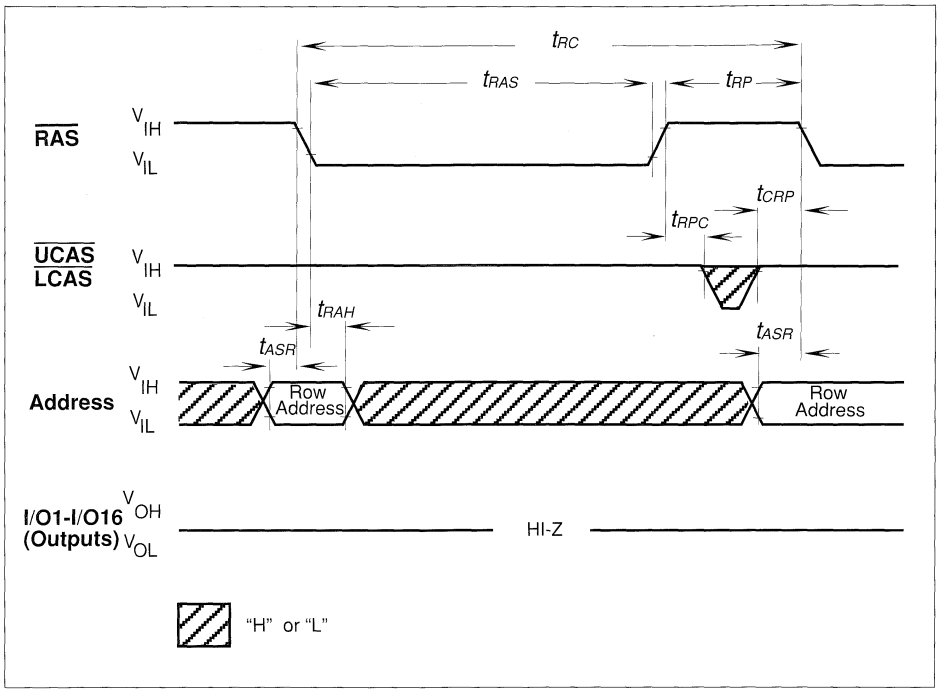
Fast Page Mode Read-Modify-Write Cycle



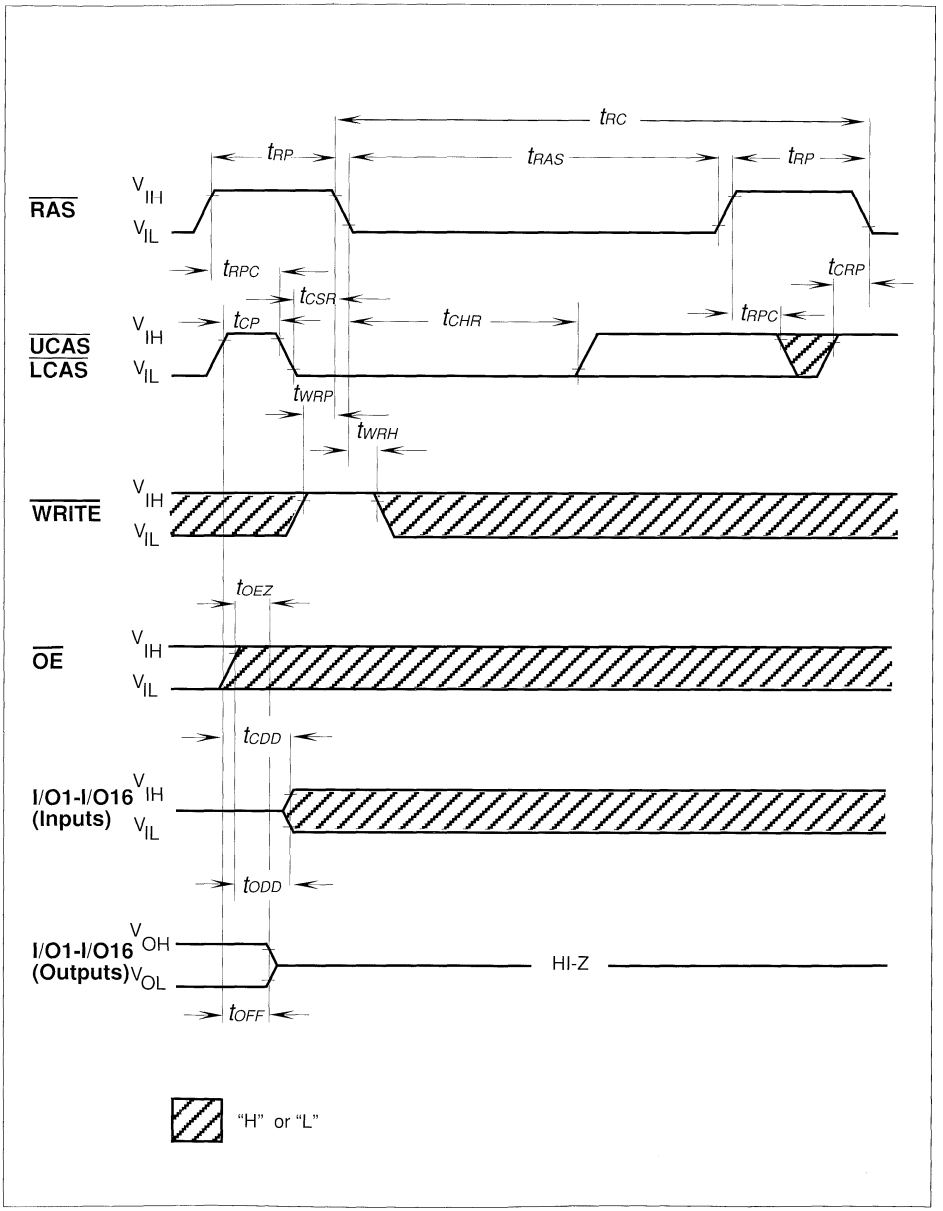
Fast Page Mode Read Cycle



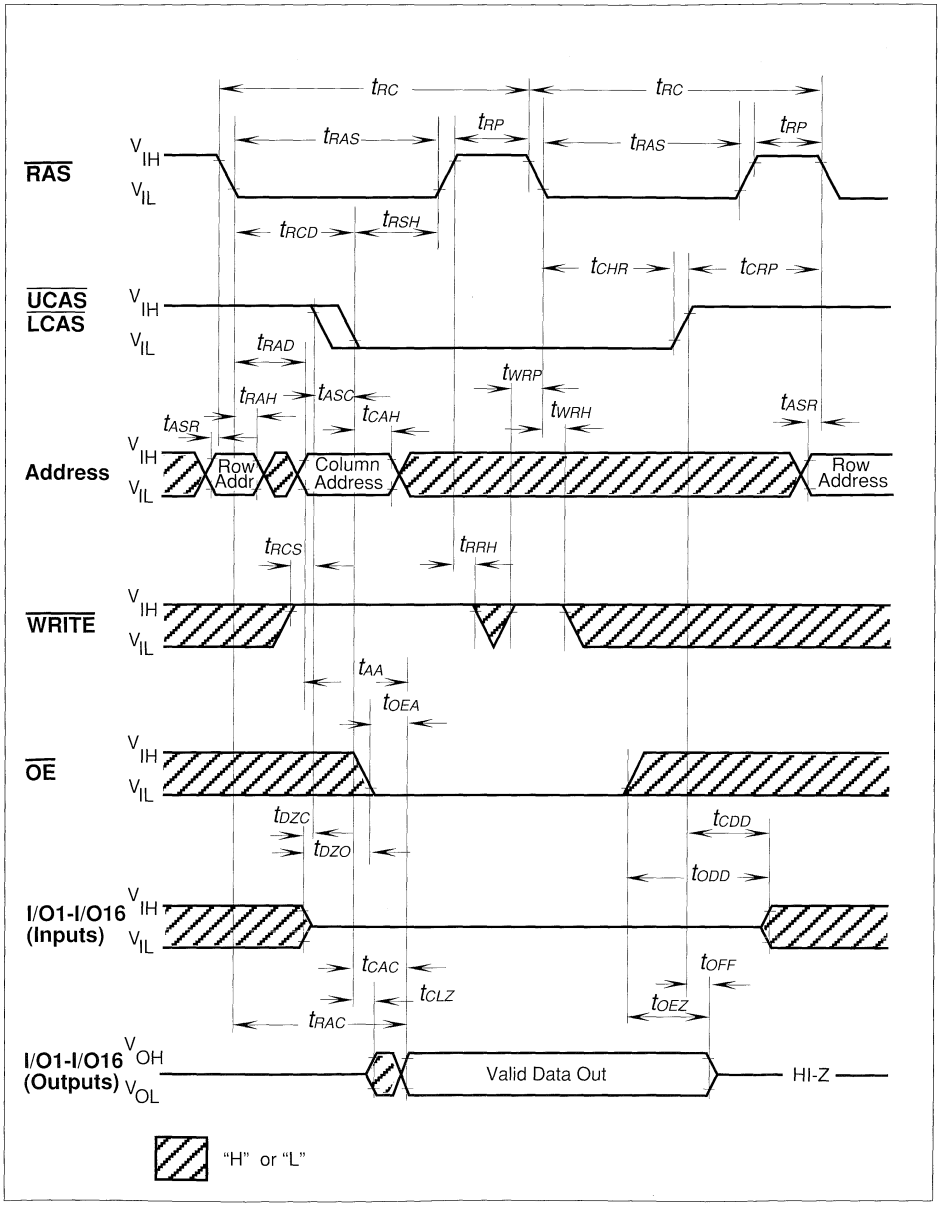
Fast Page Mode Early Write Cycle



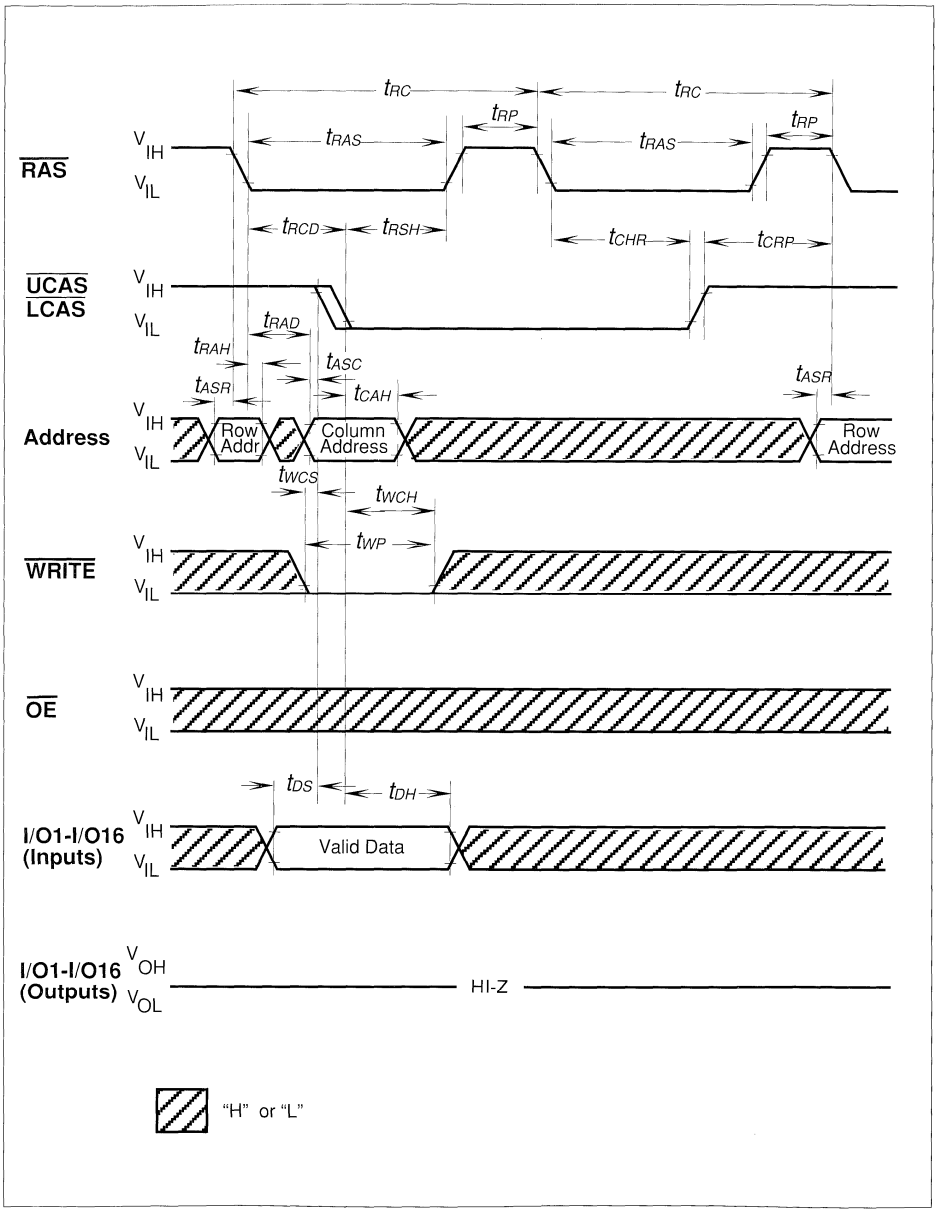
RAS-Only Refresh Cycle



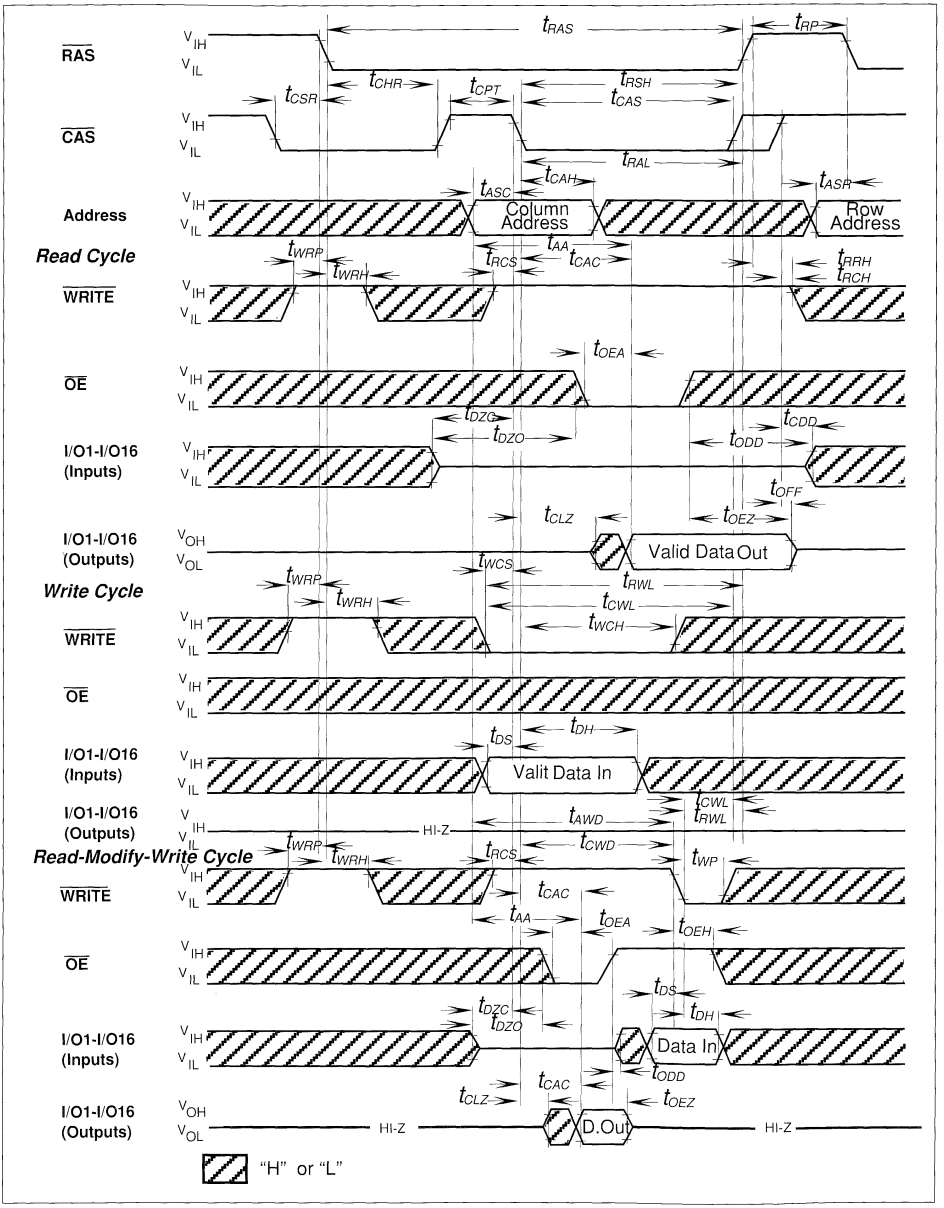
CAS-Before-RAS Refresh Cycle



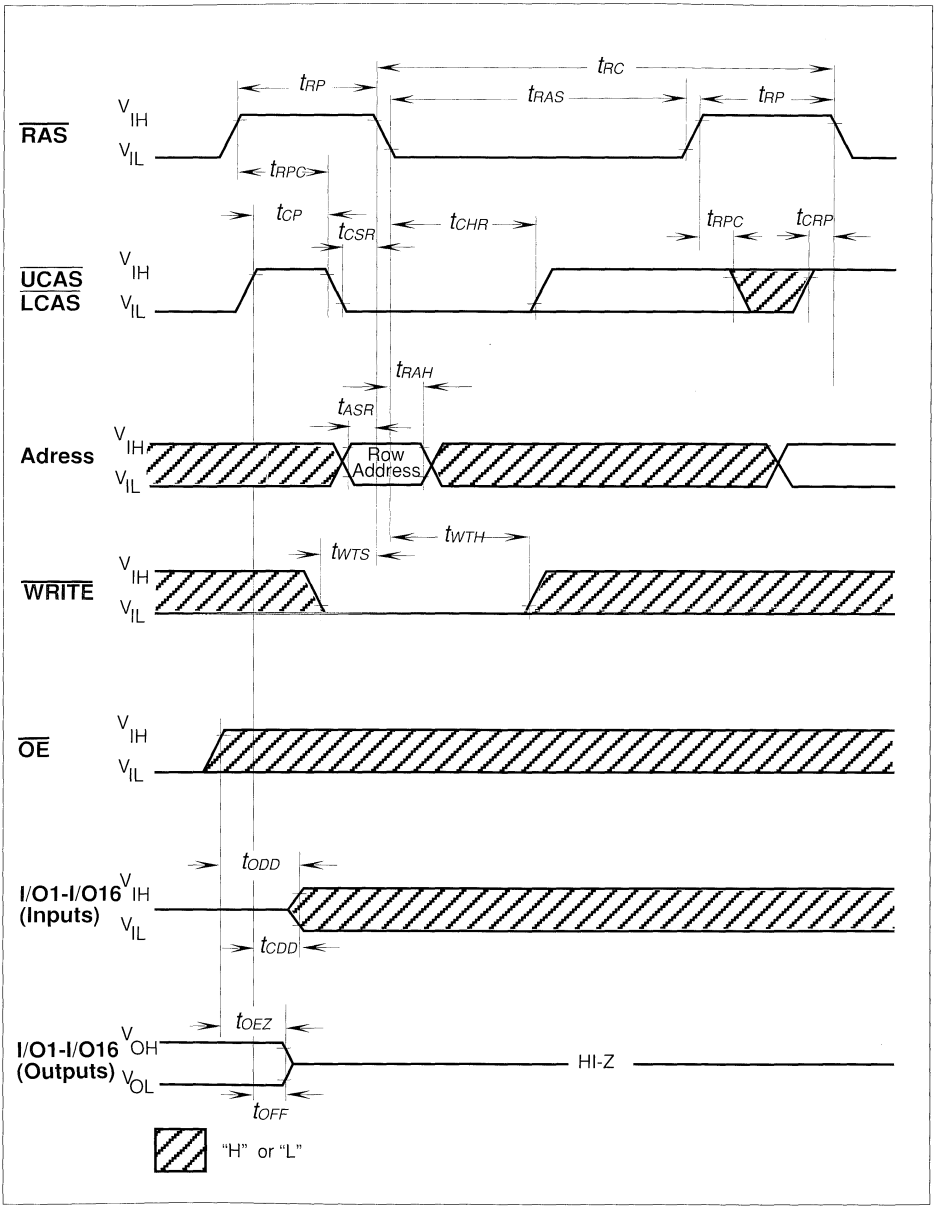
Hidden Refresh Cycle (Read)



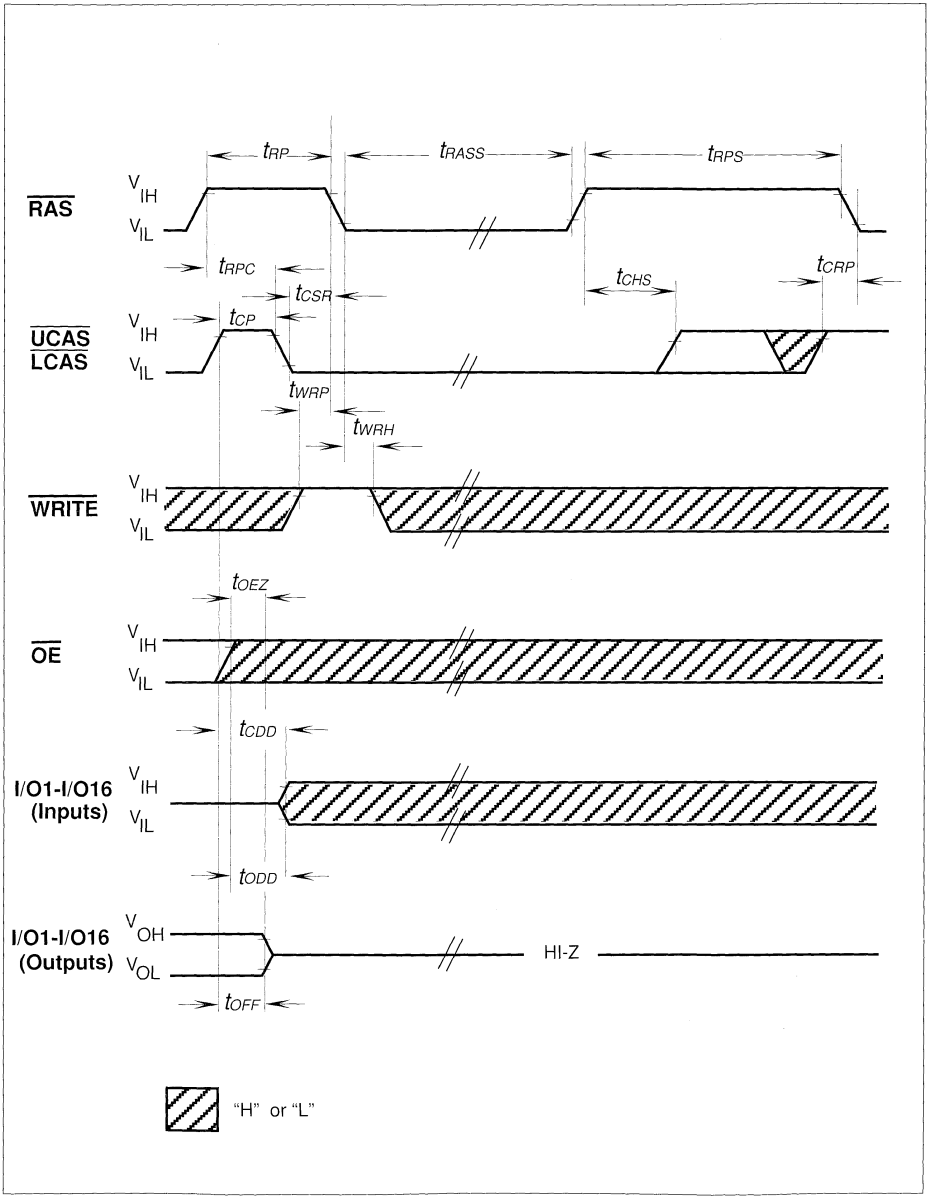
Hidden Refresh Cycle (Early Write)



CAS-Before-RAS Refresh Counter Test Cycle



Test Mode Entry



CAS-before-RAS Self Refresh

Memory Modules
Waveform for Modules

1M x 32-Bit Dynamic RAM Module (2M x 16-Bit Dynamic RAM Module)

HYM 321160S/GS-60/-70

Advanced Information

- 1 048 576 words by 32-bit organization (alternative 2 097 152 words by 16-bit)
- Fast access and cycle time
  60 ns access time
  110 ns cycle time (-60 version)
  70 ns access time
  130 ns cycle time (-70 version)
- Fast page mode capability with
  40 ns cycle time (-60 version)
  45 ns cycle time (-70 version)
- Single + 5 V (± 10 %) supply
- Low power dissipation
  max. 4840 mW active (-60 version)
  max. 4400 mW active (-70 version)
  CMOS – 44 mW standby
  TTL – 88 mW standby
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$-only-refresh, Hidden refresh
- 8 decoupling capacitors mounted on substrate
- All inputs, outputs and clock fully TTL compatible
- 72 pin Single in-Line Memory Module
- Utilizes eight 1M × 4-DRAMs in 300 mil SOJ packages
- 1024 refresh cycles /16 ms
- Tin-Lead contact pads (S - version)
- Gold contact pads (GS - version)
- single sided module with 25.4 mm (1000 mil) height

Ordering Information

Type	Ordering Code	Package	Descriptions
HYM 321160S-60	Q67100-Q2010	L-SIM-72-11	DRAM module (access time 60 ns)
HYM 321160S-70	on request	L-SIM-72-11	DRAM module (access time 70 ns)
HYM 321160GS-60	Q67100-Q2009	L-SIM-72-11	DRAM module (access time 60 ns)
HYM 321160GS-70	on request	L-SIM-72-11	DRAM module (access time 70 ns)

The HYM 321160S/GS-60/-70 is a 4 M Byte DRAM module organized as 1 048 576 words by 32-bit in a 72-pin single-in-line package comprising eight HYB 514400BJ 1M × 4 DRAMs in 300 mil wide SOJ-packages mounted together with eight 0.2 µF ceramic decoupling capacitors on a PC board.

The HYM 321160S/GS-60/-70 can also be used as a 2 097 152 words by 16-bits dynamic RAM module by means of connecting DQ0 and DQ16, DQ1 and DQ17, DQ2 and DQ18, ..., DQ15 and DQ31, respectively.

Each HYB 514400BJ is described in the data sheet and is fully electrically tested and processed according to Siemens standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

The speed of the module can be detected by the use of four presence detect pins.

The common I/O feature on the HYM 321160S/GS-60/-70 dictates the use of early write cycles.

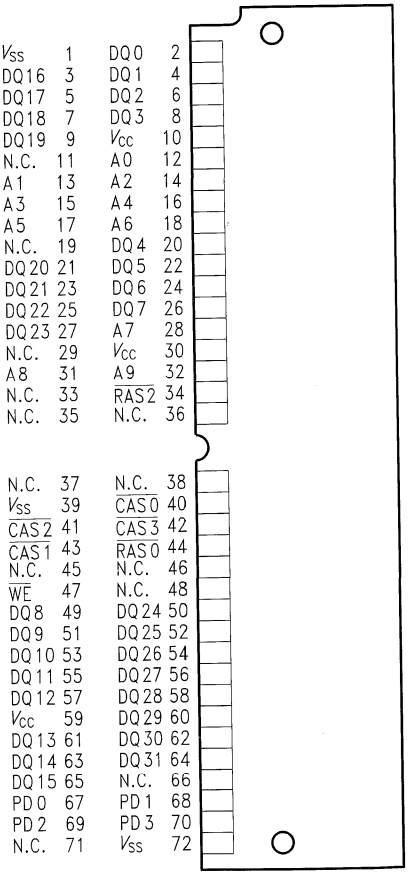
Pin Definitions and Functions

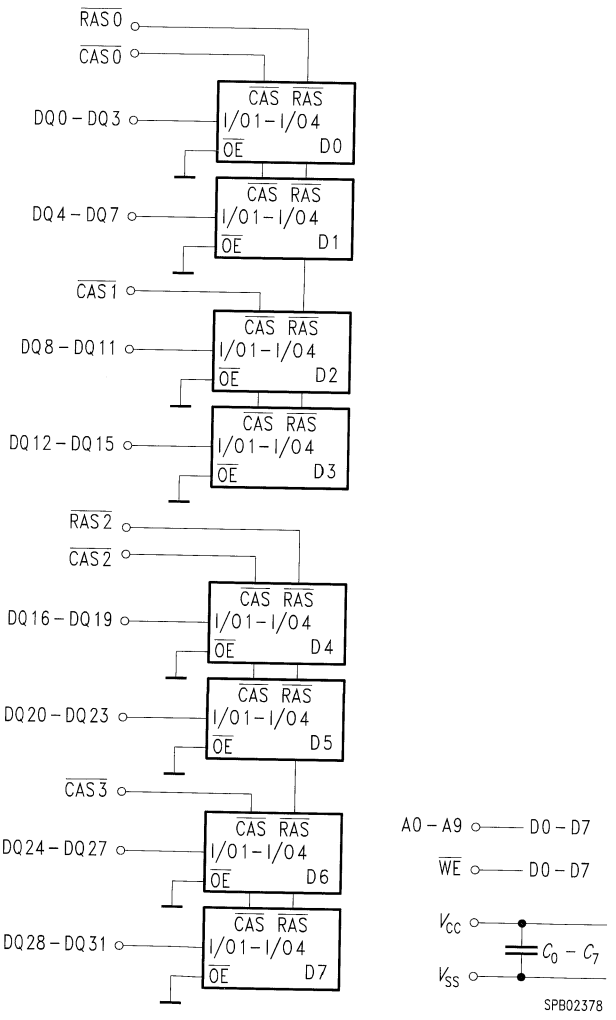
Pin No.	Function
A0-A9	Address Inputs
DQ0-DQ31	Data Input/Output
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
PD	Presence Detect Pin
N.C.	No Connection

Presence Detect Pins

	-60	-70
PD0	V_{SS}	V_{SS}
PD1	V_{SS}	V_{SS}
PD2	N.C.	V_{SS}
PD3	N.C.	N.C.

Pin Configuration
(top view)





Block Diagram

Absolute Maximum Ratings

Operating temperature range ..... 0 to + 70 °C
Storage temperature range ..... – 55 to + 125 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 1 to + 7 V
Power supply voltage ..... – 1 to + 7 V
Power dissipation ..... 6.16 W
Data out current (short circuit) ..... 50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics [1]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	5.5	V	–
Input low voltage	V_{IL}	– 1.0	0.8	V	–
Output high voltage (I_{OUT} = – 5 mA)	V_{OH}	2.4	–	V	–
Output low voltage (I_{OUT} = 4.2 mA)	V_{OL}	–	0.4	V	–
Input leakage current (0 V < V_{IN} < 6.5 V, all other pins = 0 V)	$I_{I(L)}$	– 20	20	µA	–
Output leakage current (DO is disabled, 0 V < V_{OUT} < 5.5 V)	$I_{O(L)}$	– 10	10	µA	–
Average V_{CC} supply current:	I_{CC1}				
-60 version		–	880	mA	2), 3)
-70 version		–	800	mA	
($\overline{RAS}$, $\overline{CAS}$, address cycling, t_{RC} = t_{RC} min.)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	16	mA	–
Average V_{CC} supply current during $\overline{RAS}$ only refresh cycles:	I_{CC3}				2)
-60 version		–	880	mA	
-70 version		–	800	mA	
($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)					

DC Characteristics (cont'd) [1]

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current during fast page mode:	I_{CC4}				[2], [3]
-60 version		–	560	mA	
-70 version		–	560	mA	
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling t_{PC} = t_{PC} min.)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	–	8	mA	–
Average V_{CC} supply current during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode:	I_{CC6}				[1]
-60 version		–	880	mA	
-70 version		–	800	mA	
($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min.)					

Capacitance
T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A9)	C_{I1}	–	70	pF
Input capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	C_{I2}	–	35	pF
Input capacitance ($\overline{CAS0}$-$\overline{CAS3}$)	C_{I3}	–	35	pF
Input capacitance ($\overline{WE}$)	C_{I4}	–	45	pF
I/O capacitance (DQ0-DQ31)	C_{IO1}	–	20	pF

AC Characteristics [4) 5)]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values				Unit
		HYM 321160S/GS-60		HYM 321160S/GS-70		
		min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	110	–	130	–	ns
Fast page mode cycle time	t_{PC}	40	–	45	–	ns
Access time from $\overline{RAS}$ [6) 11) 12)]	t_{RAC}	–	60	–	70	ns
Access time from $\overline{CAS}$ [6) 11)]	t_{CAC}	–	15	–	20	ns
Access time from column address [6) 12)]	t_{AA}	–	30	–	35	ns
Access time from $\overline{CAS}$ precharge [6)]	t_{CPA}	–	35	–	40	ns
$\overline{CAS}$ to output in low-Z [6)]	t_{CLZ}	0	–	0	–	ns
Output buffer turn-off delay [7)]	t_{OFF}	0	20	0	20	ns
Transition time (rise and fall) [5)]	t_T	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	40	–	50	–	ns
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	ns
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	60	200000	70	200000	ns
$\overline{CAS}$ precharge to $\overline{RAS}$ delay	t_{RHCP}	35	–	40	–	ns
$\overline{RAS}$ hold time	t_{RSH}	15	–	20	–	ns
$\overline{CAS}$ hold time	t_{CSH}	60	–	70	–	ns
$\overline{CAS}$ pulse width	t_{CAS}	15	10000	20	10000	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time [11)]	t_{RCD}	20	45	20	50	ns
$\overline{RAS}$ to column address delay time [12)]	t_{RAD}	15	30	15	35	ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	ns
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	ns
Row address hold time	t_{RAH}	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	ns
Column address hold time	t_{CAH}	15	–	15	–	ns

AC Characteristics (cont'd) [4) 5)]
T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values				Unit
		HYM 321160S/GS-60		HYM 321160S/GS-70		
		min.	max.	min.	max.	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	–	35	–	ns
Read command setup time	t_{RCS}	0	–	0	–	ns
Read command hold time [8)]	t_{RCH}	0	–	0	–	ns
Read command hold time ref. to $\overline{RAS}$ [8)]	t_{RRH}	0	–	0	–	ns
Write command hold time	t_{WCH}	10	–	15	–	ns
Write command pulse width	t_{WP}	10	–	15	–	ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	–	20	–	ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	–	20	–	ns
Data setup time [9)]	t_{DS}	0	–	0	–	ns
Data hold time [9)]	t_{DH}	15	–	15	–	ns
Refresh period	t_{REF}	–	16	–	16	ms
Write command setup time [10)]	t_{WCS}	0	–	0	–	ns
$\overline{CAS}$ setup time [13)]	t_{CSR}	5	–	5	–	ns
$\overline{CAS}$ hold time [13)]	t_{CHR}	15	–	15	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	0	–	0	–	ns
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	ns
Write to $\overline{RAS}$ precharge time [13)]	t_{WRP}	10	–	10	–	ns
Write to time ref. to $\overline{RAS}$ [13)]	t_{WRH}	10	–	10	–	ns

Notes

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.

4) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles out of which at least one cycle has to be a refresh cycle before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

5) V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.

6) Measured with a load equivalant of 2 TTL loads and 100 pF.

7) t_{OFF} (max.) defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.

8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9) These parameters are referenced to the $\overline{CAS}$ leading edge.

10) t_{WCS} is not a restrictive operating parameter. This is included in the data sheet as electrical characteristic only. If $t_{WCS} > t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance).

11) Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

12) Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

13) For $\overline{CAS}$-before-$\overline{RAS}$ cycles only.

SIEMENS

2M x 32-Bit Dynamic RAM Module

HYM 322160S/GS-60/-70

Advanced Information

- 2 097 152 words by 32-Bit organization (alternative 4 194 304 words by 16-Bit)
- Fast access and cycle time
  60 ns access time
  110 ns cycle time (-60 version)
  70 ns access time
  130 ns cycle time (-70 version)
- Fast page mode capability with
  40 ns cycle time (-60 version)
  45 ns cycle time (-70 version)
- Single + 5 V (± 10 %) supply
- Low power dissipation
  max. 4840 mW active (-60 version)
  max. 4400 mW active (-70 version)
  CMOS – 88 mW standby
  TTL – 176 mW standby
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  $\overline{\text{RAS}}$-only-refresh
  Hidden-refresh
- 8 decoupling capacitors mounted on substrate
- All inputs, outputs and clocks fully TTL compatible
- 72 pin double-sided Single in-Line Memory Module with 25.4 mm (1000 mil) height
- Utilizes sixteen 1M × 4 DRAMs in 300 mil SOJ packages
- 1024 refresh cycles / 16 ms
- Tin-Lead contact pads (S - version)
- Gold contact pads (GS - version)

Ordering Information

Type	Ordering Code	Package	Description
HYM 322160S-60	Q67100-Q2014	L-SIM-72-11	DRAM Module (access time 60 ns)
HYM 322160S-70	Q67100-Q2015	L-SIM-72-11	DRAM Module (access time 70 ns)
HYM 322160GS-60	Q67100-Q2016	L-SIM-72-11	DRAM Module (access time 60 ns)
HYM 322160GS-70	Q67100-Q2017	L-SIM-72-11	DRAM Module (access time 70 ns)

The HYM322160S/GS-60/-70 is a 8 MByte DRAM module organized as 2 097 152 words by 32-Bit in a 72-pin single-in-line package comprising sixteen HYB514400BJ 1M × 4 DRAMs in 300 mil wide SOJ-packages mounted together with eight 0.2 µF ceramic decoupling capacitors on a PC board.

The HYM322160S/GS-60/-70 can also be used as a 4 194 304 words by 16-Bits dynamic RAM module by means of connecting DQ0 and DQ16, DQ1 and DQ17, DQ2 and DQ18, ..., DQ15 and DQ31, respectively.

Each HYB514400BJ is described in the data sheet and is fully electrical tested and processed according to SIEMENS standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

The speed of the module can be detected by the use of four presence detect pins.

The common I/O feature on the HYM 322160S/GS-60/-70 dictates the use of early write cycles.

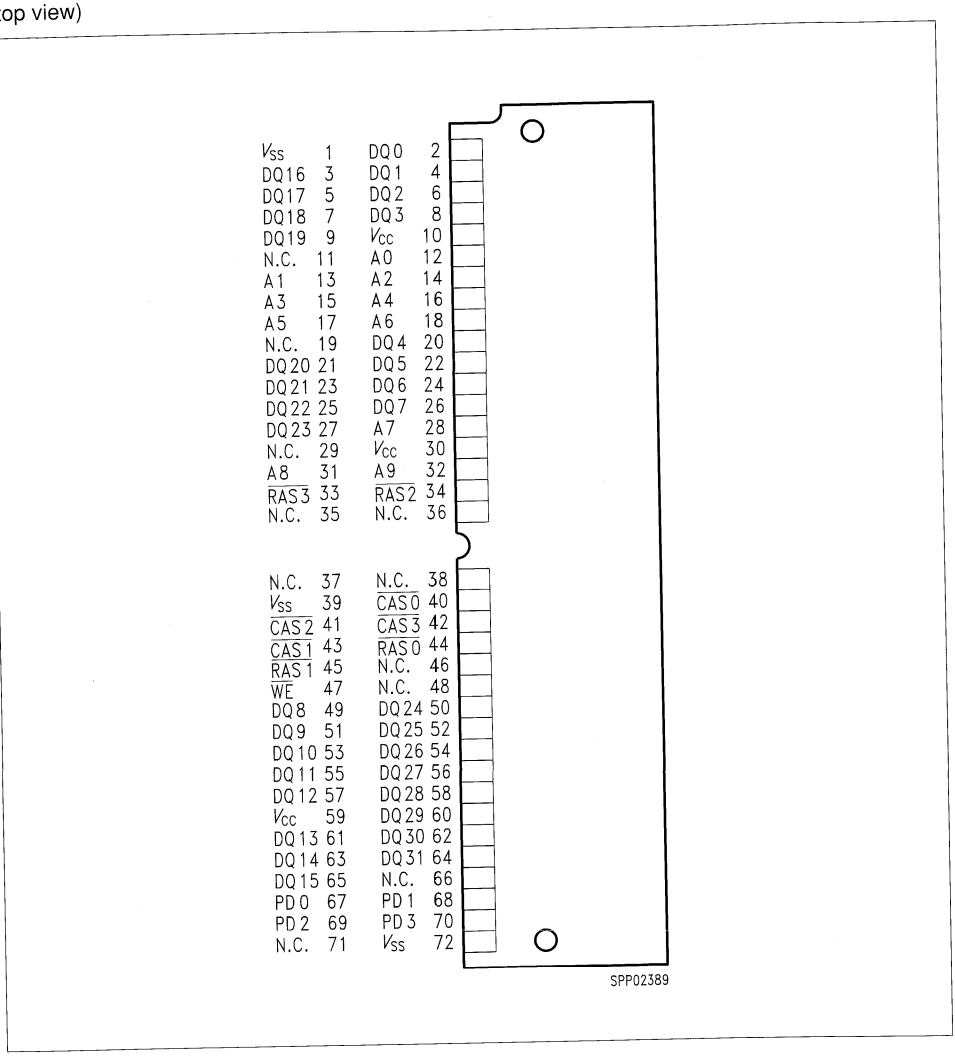
Pin Definitions and Functions

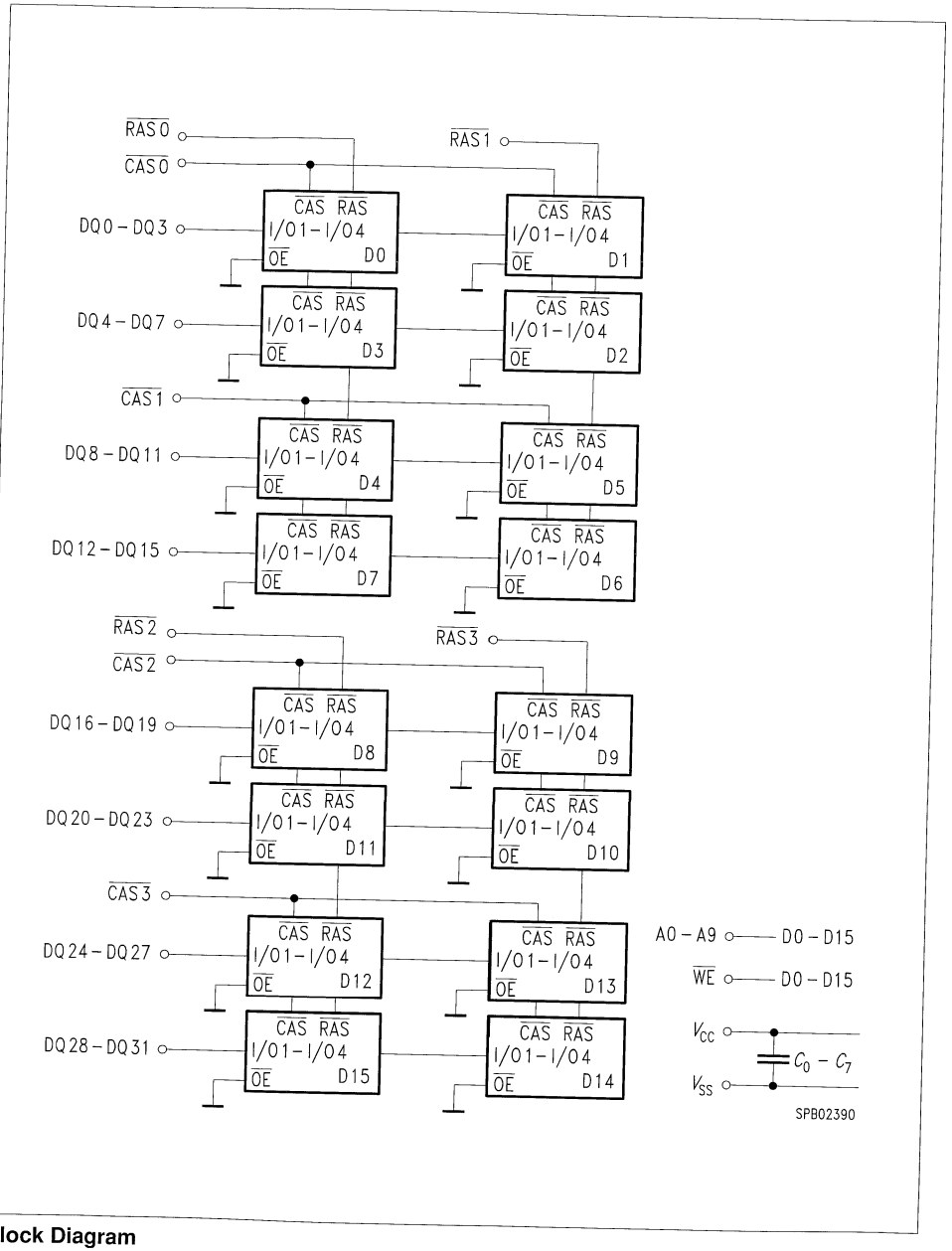
Pin No.	Function
A0-A9	Address Inputs
DQ0-DQ31	Data Input/Output
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
PD	Presence Detect Pin
N.C.	No Connection

Presence Detect Pins

	-60	-70
PD0	N.C.	N.C.
PD1	N.C.	N.C.
PD2	N.C.	V_{SS}
PD3	N.C.	N.C.

Pin Configuration
(top view)





Block Diagram

Absolute Maximum Ratings

Operation temperature range ..... 0 to + 70 °C
Storage temperature range ..... – 55 to 125 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 1 to + 7 V
Power supply voltage ..... – 1 to + 7 V
Power dissipation ..... 6.2 W
Data out current (short circuit) ..... 50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics[1)]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	5.5	V	
Input low voltage	V_{IL}	– 1.0	0.8	V	
Output high voltage (I_{OUT} = – 5 mA)	V_{OH}	2.4	–	V	
Output low voltage (I_{OUT} = 4.2 mA)	V_{OL}	–	0.4	V	
Input leakage current (0 V < V_{IN} < 6.5 V, all other pins = 0 V)	$I_{I(L)}$	– 20	20	µA	
Output leakage current (DO is disabled, 0 V < V_{OUT} < 5.5 V)	$I_{O(L)}$	– 20	20	µA	
Average V_{CC} supply current ($\overline{RAS}$, $\overline{CAS}$, address cycling, t_{RC} = t_{RC} min) -60 version -70 version	I_{CC1}	 – –	 880 800	 mA mA	 2), 3)
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	32	mA	
Average V_{CC} supply current during $\overline{RAS}$ only refresh cycles ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min) -60 version -70 version	I_{CC3}	 – –	 880 800	 mA mA	 2)

DC Characteristics[1] (cont'd)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current during fast page mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling, t_{PC} = t_{PC} min)	I_{CC4}				
-60 version		–	560	mA	[2],
-70 version		–	560	mA	[3]
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	–	16	mA	
Average V_{CC} supply current during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode ($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min)	I_{CC6}				
-60 version		–	880	mA	[2]
-70 version		–	800	mA	

Capacitance

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A9, $\overline{WE}$)	C_{I1}	–	120	pF
Input capacitance ($\overline{RAS0}$-$\overline{RAS2}$, $\overline{CAS0}$-$\overline{CAS3}$)	C_{I2}	–	40	pF
I/O capacitance (DQ0-DQ31)	C_{IO1}	–	29	pF

AC Characteristics [4) 5)]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values				Unit
		HYM 322160S/GS-60		HYM 322160S/GS-70		
		min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	110	–	130	–	ns
Fast page mode cycle time	t_{PC}	40	–	45	–	ns
Access time from $\overline{RAS}$ [6) 11) 12)]	t_{RAC}	–	60	–	70	ns
Access time from $\overline{CAS}$ [6) 11)]	t_{CAC}	–	15	–	20	ns
Access time from column address [6) 12)]	t_{AA}	–	30	–	35	ns
Access time from $\overline{CAS}$ precharge [6)]	t_{CPA}	–	35	–	40	ns
$\overline{CAS}$ to output in low-Z [6)]	t_{CLZ}	0	–	0	–	ns
Output buffer turn-off delay [7)]	t_{OFF}	0	20	0	20	ns
Transition time (rise and fall) [5)]	t_T	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	40	–	50	–	ns
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	ns
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	60	200000	70	200000	ns
$\overline{CAS}$ precharge to $\overline{RAS}$ delay	t_{RHCP}	35	–	40	–	ns
$\overline{RAS}$ hold time	t_{RSH}	15	–	20	–	ns
$\overline{CAS}$ hold time	t_{CSH}	60	–	70	–	ns
$\overline{CAS}$ pulse width	t_{CAS}	15	10000	20	10000	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time [11)]	t_{RCD}	20	45	20	50	ns
$\overline{RAS}$ to column address delay time [12)]	t_{RAD}	15	30	15	35	ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	ns
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	ns
Row address hold time	t_{RAH}	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	ns
Column address hold time	t_{CAH}	15	–	15	–	ns

AC Characteristics[4) 5)] (cont'd)
T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values				Unit
		HYM 322160S/GS-60		HYM 322160S/GS-70		
		min.	max.	min.	max.	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	–	35	–	ns
Read command setup time	t_{RCS}	0	–	0	–	ns
Read command hold time [8)]	t_{RCH}	0	–	0	–	ns
Read command hold time ref. to $\overline{RAS}$ [8)]	t_{RRH}	0	–	0	–	ns
Write command hold time	t_{WCH}	10	–	15	–	ns
Write command pulse width	t_{WP}	10	–	15	–	ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	–	20	–	ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	–	20	–	ns
Data setup time [9)]	t_{DS}	0	–	0	–	ns
Data hold time [9)]	t_{DH}	15	–	15	–	ns
Refresh period	t_{REF}	–	16	–	16	ms
Write command setup time [10)]	t_{WCS}	0	–	0	–	ns
$\overline{CAS}$ setup time [13)]	t_{CSR}	5	–	5	–	ns
$\overline{CAS}$ hold time [13)]	t_{CHR}	15	–	15	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	0	–	0	–	ns
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	ns
Write to $\overline{RAS}$ precharge time [13)]	t_{WRP}	10	–	10	–	ns
Write hold time ref. to $\overline{RAS}$ [13)]	t_{WRH}	10	–	10	–	ns

Notes:

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.

4) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles out of which at least one cycle has to be a refresh cycle before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

5) V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.

6) Measured with a load equivalant of 2 TTL loads and 100 pF.

7) t_{OFF} (max.) defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.

8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9) These parameters are referenced to the $\overline{CAS}$ leading edge.

10) t_{WCS} is not a restrictive operating parameter. This is included in the data sheet as electrical characteristic only. If $t_{WCS} > t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance).

11) Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

12) Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

13) For $\overline{CAS}$-before-$\overline{RAS}$ cycles only.

2M x 32-Bit Dynamic RAM Module

HYM 322030S/GS-60/-70

Advanced Information

- 2 097 152 words by 32-bit organization
- Fast access and cycle time
  60 ns access time
  110 ns cycle time (-60 version)
  70 ns access time
  130 ns cycle time (-70 version)
- Fast page mode capability
  40 ns cycle time (-60 version)
  45 ns cycle time (-70 version)
- Single + 5 V (± 10 %) supply
- Low power dissipation
  max. 3300 mW active (-60 version)
  max. 3025 mW active (-70 version)
  CMOS – 22 mW standby
  TTL – 44 mW standby
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  $\overline{\text{RAS}}$-only-refresh
  Hidden-refresh
- 4 decoupling capacitors mounted on substrate
- All inputs, outputs and clocks fully TTL compatible
- 72 pin Single in-Line Memory Module (L-SIM-72-9) with 20.32 mm (800 mil) height
- Utilizes four 2M × 8 - DRAMs in 400 mil SOJ-packages
- 2048 refresh cycles / 32 ms
- Tin-Lead contact pads (S - version)
- Gold contact pads (GS - version)

Ordering Information

Type	Ordering Code	Package	Description
HYM 322030S-60	Q67100-Q976	L-SIM-72-9	DRAM Module (access time 60 ns)
HYM 322030S-70	Q67100-Q977	L-SIM-72-9	DRAM Module (access time 70 ns)
HYM 322030GS-60	Q67100-Q2018	L-SIM-72-9	DRAM Module (access time 60 ns)
HYM 322030GS-70	Q67100-Q2019	L-SIM-72-9	DRAM Module (access time 70 ns)

The HYM 322030S/GS-60/-70 is a 8 M Byte DRAM module organized as 2 097 152 words by 32-bit in a 72-pin single-in-line package comprising four HYB 5117800BSJ 2M × 8 DRAMs in 400 mil wide SOJ-packages mounted together with four 0.2 µF ceramic decoupling capacitors on a PC board.

Each HYB 5117800BSJ is described in the data sheet and is fully electrical tested and processed according to SIEMENS standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

The speed of the module can be detected by the use of four presence detect pins.

The common I/O feature on the HYM 322030S/GS-60/-70 dictates the use of early write cycles.

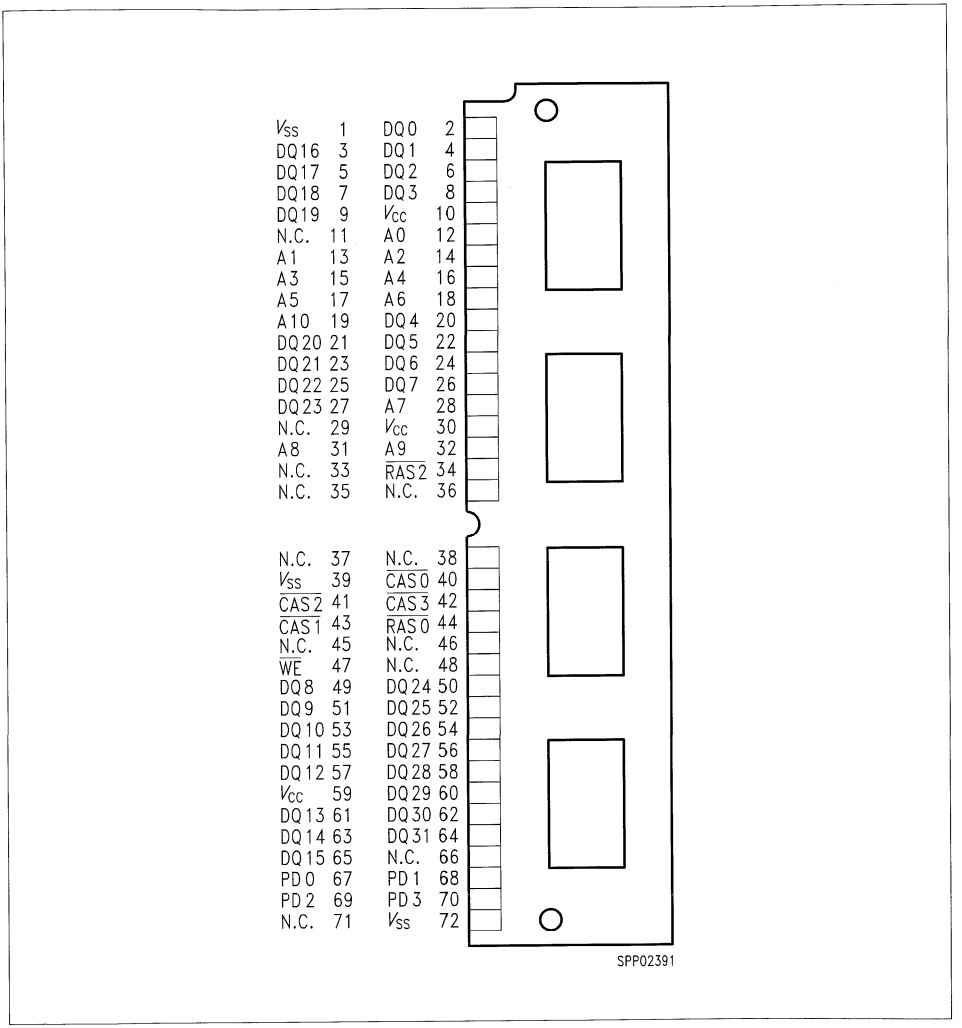
Pin Definitions and Functions

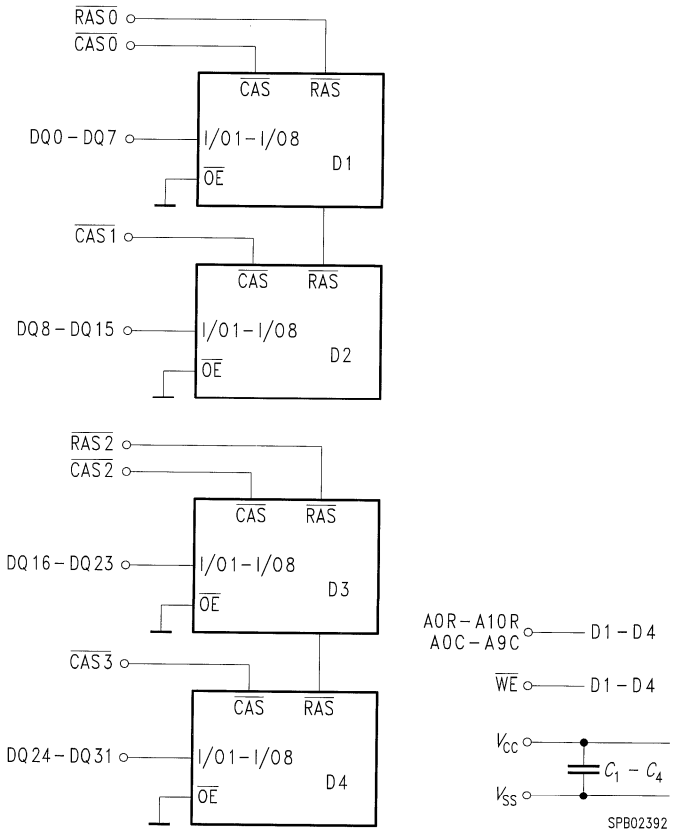
Pin No.	Function
A0R-A10R	Row Address Inputs
A0C-A9C	Column Address Inputs
DQ0-DQ31	Data Input/Output
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
PD	Presence Detect Pin
N.C.	No Connection

Presence Detect Pins

	-60	-70
PD0	N.C.	N.C.
PD1	N.C.	N.C.
PD2	N.C.	V_{SS}
PD3	N.C.	N.C.

Pin Configuration
(top view)





Block Diagram

Absolute Maximum Ratings

Operation temperature range ..... 0 to + 70 °C
Storage temperature range ..... – 55 to 125 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 0.5 V to min (V_{CC} + 0.5, 7.0) V
Power supply voltage ..... – 1 to + 7 V
Power dissipation ..... 4.2 W
Data out current (short circuit) ..... 50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics[1)]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	V_{CC} + 0.5	V	
Input low voltage	V_{IL}	– 0.5	0.8	V	
Output high voltage (I_{OUT} = – 5 mA)	V_{OH}	2.4	–	V	
Output low voltage (I_{OUT} = 4.2 mA)	V_{OL}	–	0.4	V	
Input leakage current (0 V < V_{IN} < 6.5 V, all other pins = 0 V)	$I_{I(L)}$	– 10	10	µA	
Output leakage current (DO is disabled, 0 V < V_{OUT} < 5.5 V)	$I_{O(L)}$	– 10	10	µA	
Average V_{CC} supply current ($\overline{RAS}$, $\overline{CAS}$, address cycling, t_{RC} = t_{RC} min)	I_{CC1}				
-60 version		–	550	mA	2)
-70 version		–	500	mA	3)
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	8	mA	
Average V_{CC} supply current during $\overline{RAS}$ only refresh cycles ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min)	I_{CC3}				
-60 version		–	550	mA	2)
-70 version		–	500	mA	

DC Characteristics[1] (cont'd)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current during fast page mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling, t_{PC} = t_{PC} min)	I_{CC4}				
-60 version		–	550	mA	[2]
-70 version		–	500	mA	[3]
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	–	4	mA	
Average V_{CC} supply current during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode ($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min)	I_{CC6}				
-60 version		–	600	mA	[2]
-70 version		–	550	mA	

Capacitance

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A11)	C_{I1}	–	40	pF
Input capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	C_{I2}	–	45	pF
Input capacitance ($\overline{CAS0}$ - $\overline{CAS3}$)	C_{I3}	–	45	pF
Input capacitance ($\overline{WE}$)	C_{I4}	–	45	pF
I/O capacitance (DQ0-DQ31)	C_{IO}	–	25	pF

AC Characteristics [4) 5)]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values				Unit
		HYM 322030S/GS-60		HYM 322030S/GS-70		
		min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	110	–	130	–	ns
Fast page mode cycle time	t_{PC}	40	–	45	–	ns
Access time from $\overline{RAS}$ [6) 11) 12)]	t_{RAC}	–	60	–	70	ns
Access time from $\overline{CAS}$ [6) 11)]	t_{CAC}	–	15	–	20	ns
Access time from column address [6) 12)]	t_{AA}	–	30	–	35	ns
Access time from $\overline{CAS}$ precharge [6)]	t_{CPA}	–	35	–	40	ns
$\overline{CAS}$ to output in low-Z [6)]	t_{CLZ}	0	–	0	–	ns
Output buffer turn-off delay [7)]	t_{OFF}	0	20	0	20	ns
Transition time (rise and fall) [5)]	t_T	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	40	–	50	–	ns
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	ns
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	60	200000	70	200000	ns
$\overline{CAS}$ precharge to $\overline{RAS}$ delay	t_{RHCP}	35	–	40	–	ns
$\overline{RAS}$ hold time	t_{RSH}	15	–	20	–	ns
$\overline{CAS}$ hold time	t_{CSH}	60	–	70	–	ns
$\overline{CAS}$ pulse width	t_{CAS}	15	10000	20	10000	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time [11)]	t_{RCD}	20	45	20	50	ns
$\overline{RAS}$ to column address delay time [12)]	t_{RAD}	15	30	15	35	ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	ns
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	ns
Row address hold time	t_{RAH}	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	ns
Column address hold time	t_{CAH}	15	–	15	–	ns

AC Characteristics[4) 5)] (cont'd)
T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values				Unit
		HYM 322030S/GS-60		HYM 322030S/GS-70		
		min.	max.	min.	max.	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	–	35	–	ns
Read command setup time	t_{RCS}	0	–	0	–	ns
Read command hold time [8)]	t_{RCH}	0	–	0	–	ns
Read command hold time ref. to $\overline{RAS}$ [8)]	t_{RRH}	0	–	0	–	ns
Write command hold time	t_{WCH}	10	–	15	–	ns
Write command pulse width	t_{WP}	10	–	15	–	ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	–	20	–	ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	–	20	–	ns
Data setup time [9)]	t_{DS}	0	–	0	–	ns
Data hold time [9)]	t_{DH}	15	–	15	–	ns
Refresh period	t_{REF}	–	32	–	32	ms
Write command setup time [10)]	t_{WCS}	0	–	0	–	ns
$\overline{CAS}$ setup time [13)]	t_{CSR}	10	–	10	–	ns
$\overline{CAS}$ hold time [13)]	t_{CHR}	10	–	10	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5	–	5	–	ns
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	ns
Write to $\overline{RAS}$ precharge time [13)]	t_{WRP}	10	–	10	–	ns
Write hold time ref. to $\overline{RAS}$ [13)]	t_{WRH}	10	–	10	–	ns

Notes

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading.
Specified values are measured with the output open.

4) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles out of which at least one cycle has to be a refresh cycle before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

5) V_{IH} (max) and V_{IL} (max) are reference levels for measuring timing of input signals.
Transition times are also measured between V_{IH} and V_{IL}.

6) Measured with a load equivalent of 2 TTL loads and 100 pF.

7) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.

8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9) These parameters are referenced to the $\overline{CAS}$ leading edge.

10) t_{WCS} is not a restrictive operating parameter. This is included in the data sheet as electrical characteristic only. If $t_{WCS} > t_{WCS}$ (min), the cycle is an early write cycle and data out pin will remain open (high impedance).

11) Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAS}.

12) Operation within the t_{HAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.

13) For $\overline{CAS}$-before-$\overline{RAS}$ cycles only.

4M x 32-Bit Dynamic RAM Module

HYM 324020S/GS-60/-70

Preliminary Information

- 4 194 304 words by 32-bit organization (alternative 8 388 608 words by 16-bit)
- Fast access and cycle time
  60 ns access time
  110 ns cycle time (-60 version)
  70 ns access time
  130 ns cycle time (-70 version)
- Fast page mode capability
  40 ns cycle time (-60 version)
  45 ns cycle time (-70 version)
- Single + 5 V (± 10 %) supply
- Low power dissipation
  max. 4840 mW active
  (HYM 324020S/GS-60)
  max. 4400 mW active
  (HYM 324020S/GS-70)
  CMOS – 44 mW standby
  TTL – 88 mW standby
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  $\overline{\text{RAS}}$-only-refresh
  Hidden-refresh
- 8 decoupling capacitors mounted on substrate
- All inputs, outputs and clocks fully TTL compatible
- 72 pin Single in-Line Memory Module with 22.86 mm (900 mil) height
- Utilizes eight 4Mx4-DRAMs in 300mil wide SOJ-packages
- 2048 refresh cycles / 32 ms
- Tin-Lead contact pads (S - version)
- Gold contact pads (GS - version)

Ordering Information

Type	Ordering Code	Package	Description
HYM 324020S-60	Q67100-Q979	L-SIM-72-12	DRAM Module (access time 60 ns)
HYM 324020S-70	Q67100-Q980	L-SIM-72-12	DRAM Module (access time 70 ns)
HYM 324020GS-60	Q67100-Q2005	L-SIM-72-12	DRAM Module (access time 60 ns)
HYM 324020GS-70	on request	L-SIM-72-12	DRAM Module (access time 70 ns)

The HYM 324020S/GS-60/-70 is a 16 M Byte DRAM module organized as 4 194 304 words by 32-bit in a 72-pin single-in-line package comprising eight HYB 5117400BJ 4M x 4 DRAMs in 300 mil wide SOJ-packages mounted together with eight 0.2 µF ceramic decoupling capacitors on a PC board.

The HYM 324020S/GS-60/-70 can also be used as a 8 388 608 words by 16-bits dynamic RAM module by means of connecting DQ0 and DQ16, DQ1 and DQ17, DQ2 and DQ18, ..., DQ15 and DQ31, respectively.

Each HYB 5117400BJ is described in the data sheet and is fully electrical tested and processed according to SIEMENS standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

The speed of the module can be detected by the use of four presence detect pins.

The common I/O feature on the HYM 324020S/GS-60/-70 dictates the use of early write cycles.

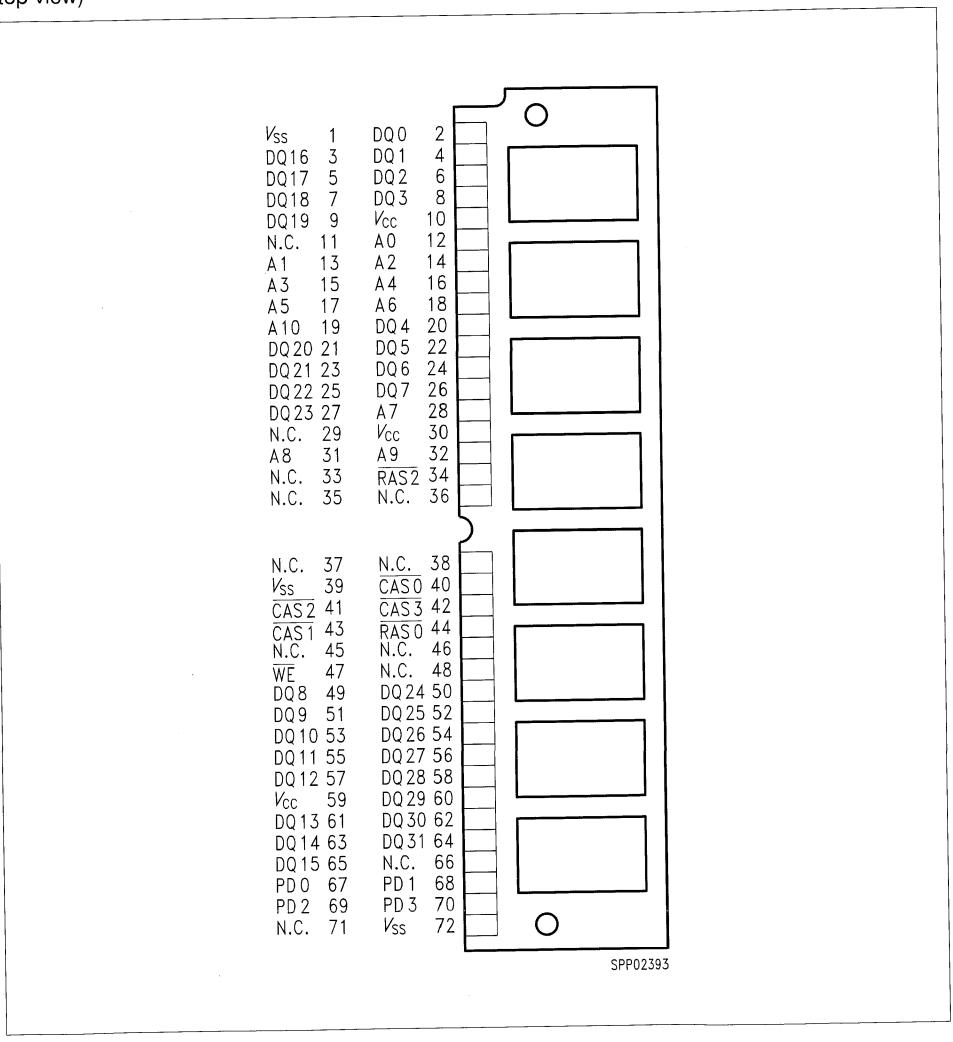
Pin Definitions and Functions

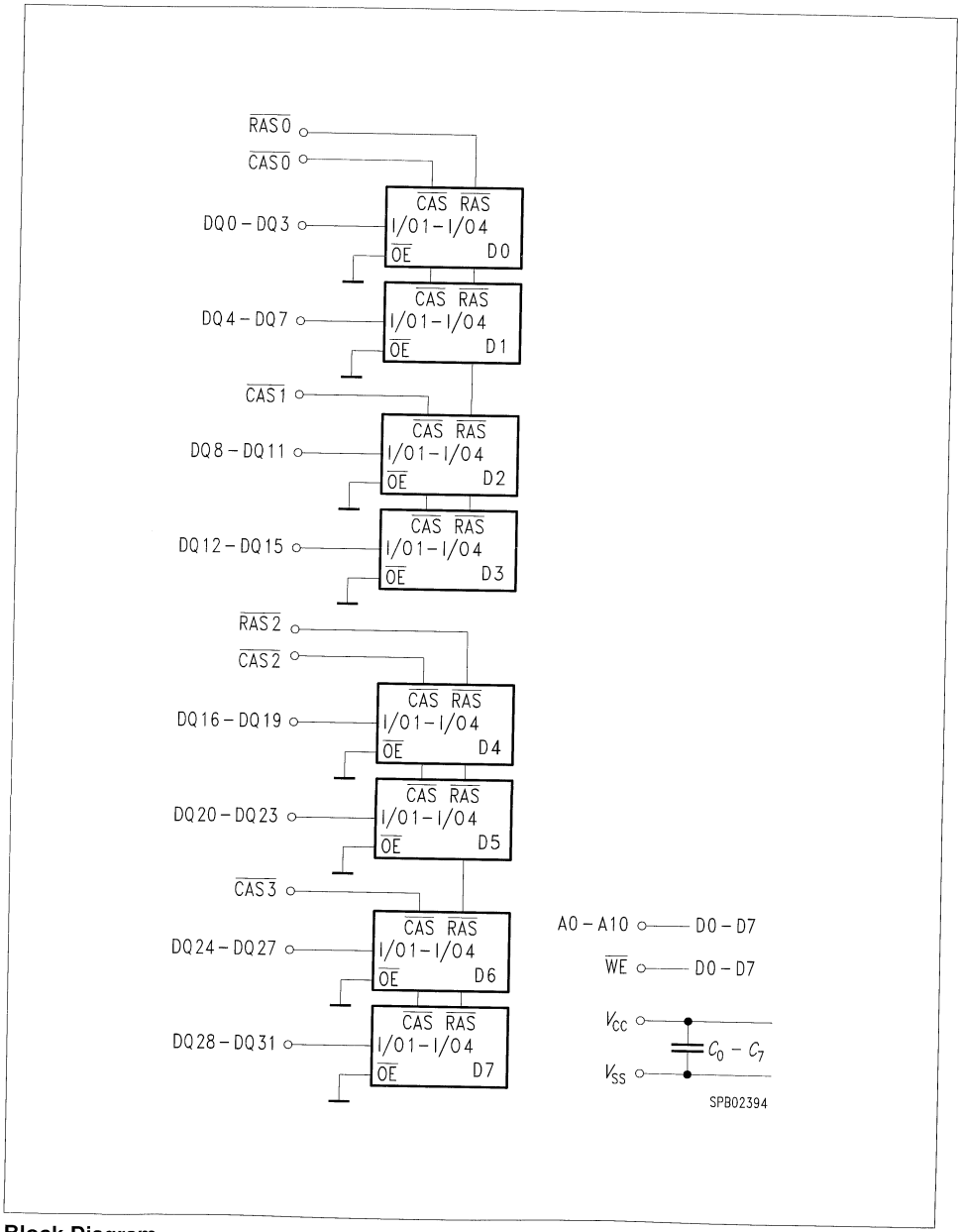
Pin No.	Functions
A0-A10	Address Inputs for HYM 324020S/GS
DQ0-DQ31	Data Input/Output
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
PD	Presence Detect Pin
N.C.	No Connection

Presence Detect Pins

	-60	-70
PD0	V_{SS}	V_{SS}
PD1	N.C.	N.C.
PD2	N.C.	V_{SS}
PD3	N.C.	N.C.

Pin Configuration
(top view)





Block Diagram

Absolute Maximum Ratings

Operation temperature range ..... 0 to + 70 °C
Storage temperature range..... – 55 to 125 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 0.5 V to min (V_{CC} + 0.5, 7.0) V
Power supply voltage..... – 1 to + 7 V
Power dissipation..... 6.16 W
Data out current (short circuit) ..... 50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics[1)]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	V_{CC} + 0.5	V	
Input low voltage	V_{IL}	– 0.5	0.8	V	
Output high voltage (I_{OUT} = – 5 mA)	V_{OH}	2.4	–	V	
Output low voltage (I_{OUT} = 4.2 mA)	V_{OL}	–	0.4	V	
Input leakage current (0 V < V_{IN} < 6.5 V, all other pins = 0 V)	$I_{I(L)}$	– 20	20	µA	
Output leakage current (DO is disabled, 0 V < V_{OUT} < 5.5 V)	$I_{O(L)}$	– 10	10	µA	
Average V_{CC} supply current ($\overline{RAS}$, $\overline{CAS}$, address cycling, t_{RC} = t_{RC} min)	I_{CC1}				
60 ns - Version		–	880	mA	2)
70 ns - Version		–	800	mA	3)
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	16	mA	
Average V_{CC} supply current during $\overline{RAS}$ only refresh cycles ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min)	I_{CC3}				
60 ns - Version		–	880	mA	2)
70 ns - Version		–	800	mA	

DC Characteristics[1] (cont'd)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current during fast page mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling, t_{PC} = t_{PC} min)	I_{CC4}				
60 ns - Version		–	640	mA	2)
70 ns - Version		–	560	mA	3)
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	–	8	mA	
Average V_{CC} supply current during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode ($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min)	I_{CC6}				2)
60 ns - Version		–	880	mA	
70 ns - Version		–	800	mA	

Capacitance

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A10,$\overline{WE}$)	C_{I1}	–	90	pF
Input capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	C_{I2}	–	45	pF
Input capacitance ($\overline{CAS0}$ - $\overline{CAS3}$)	C_{I3}	–	40	pF
I/O capacitance (DQ0-DQ31)	C_{IO}	–	25	pF

AC Characteristics [4) 5)]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values				Unit
		HYM 324020S/GS-60		HYM 324020S/GS-70		
		min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	110	–	130	–	ns
Fast page mode cycle time	t_{PC}	40	–	45	–	ns
Access time from $\overline{RAS}$ [6) 11) 12)]	t_{RAC}	–	60	–	70	ns
Access time from $\overline{CAS}$ [6) 11)]	t_{CAC}	–	15	–	20	ns
Access time from column address [6) 12)]	t_{AA}	–	30	–	35	ns
Access time from $\overline{CAS}$ precharge [6)]	t_{CPA}	–	35	–	40	ns
$\overline{CAS}$ to output in low-Z [6)]	t_{CLZ}	0	–	0	–	ns
Output buffer turn-off delay [7)]	t_{OFF}	0	20	0	20	ns
Transition time (rise and fall) [5)]	t_T	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	40	–	50	–	ns
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	ns
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	60	200000	70	200000	ns
$\overline{CAS}$ precharge to $\overline{RAS}$ delay	t_{RHCP}	35	–	40	–	ns
$\overline{RAS}$ hold time	t_{RSH}	15	–	20	–	ns
$\overline{CAS}$ hold time	t_{CSH}	60	–	70	–	ns
$\overline{CAS}$ pulse width	t_{CAS}	15	10000	20	10000	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time [11)]	t_{RCD}	20	45	20	50	ns
$\overline{RAS}$ to column address delay time [12)]	t_{RAD}	15	30	15	35	ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	ns
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	ns
Row address hold time	t_{RAH}	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	ns
Column address hold time	t_{CAH}	15	–	15	–	ns

AC Characteristics[4) 5)] (cont'd)
T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values				Unit
		HYM 324020S/GS-60		HYM 324020S/GS-70		
		min.	max.	min.	max.	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	–	35	–	ns
Read command setup time	t_{RCS}	0	–	0	–	ns
Read command hold time [8)]	t_{RCH}	0	–	0	–	ns
Read command hold time ref. to $\overline{RAS}$ [8)]	t_{RRH}	0	–	0	–	ns
Write command hold time	t_{WCH}	10	–	15	–	ns
Write command pulse width	t_{WP}	10	–	15	–	ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	–	20	–	ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	–	20	–	ns
Data setup time [9)]	t_{DS}	0	–	0	–	ns
Data hold time [9)]	t_{DH}	15	–	15	–	ns
Refresh period	t_{REF}	–	32	–	32	ms
Write command setup time [10)]	t_{WCS}	0	–	0	–	ns
$\overline{CAS}$ setup time [13)]	t_{CSR}	10	–	10	–	ns
$\overline{CAS}$ hold time [13)]	t_{CHR}	10	–	10	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5	–	5	–	ns
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	ns
Write to $\overline{RAS}$ precharge time [13)]	t_{WRP}	10	–	10	–	ns
Write hold time ref. to $\overline{RAS}$ [13)]	t_{WRH}	10	–	10	–	ns

Notes

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading.
Specified values are measured with the output open.

4) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles out of which at least one cycle has to be a refresh cycle before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

5) V_{IH} (max) and V_{IL} (max) are reference levels for measuring timing of input signals.
Transition times are also measured between V_{IH} and V_{IL}.

6) Measured with a load equivalent of 2 TTL loads and 100 pF.

7) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.

8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9) These parameters are referenced to the $\overline{CAS}$ leading edge.

10) t_{WCS} is not a restrictive operating parameter. This is included in the data sheet as electrical characteristic only. If $t_{WCS} > t_{WCS}$ (min), the cycle is an early write cycle and data out pin will remain open (high impedance).

11) Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAS}.

12) Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.

13) For $\overline{CAS}$-before-$\overline{RAS}$ cycles only.

8M × 32-Bit Dynamic RAM Module

HYM 328020S/GS-60/-70

Preliminary Information

- 8 388 608 words by 32-bit organization (alternative 16 777 216 words by 16-bit)
- Fast access and cycle time
  60 ns access time
  110 ns cycle time (-60 version)
  70 ns access time
  130 ns cycle time (-70 version)
- Fast page mode capability
  40 ns cycle time (-60 version)
  45 ns cycle time (-70 version)
- Single + 5 V (± 10 %) supply
- Low power dissipation
  max. 4840 mW active (-60 version)
  max. 4400 mW active (-70 version)
  CMOS – 88 mW standby
  TTL – 176 mW standby
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  $\overline{\text{RAS}}$-only-refresh
  Hidden-refresh
- 16 decoupling capacitors mounted on substrate
- All inputs, outputs and clocks fully TTL compatible
- 72 pin Single in-Line Memory Module (L-SIM-72) with 25.40 mm height
- Utilizes sixteen 4M x 4-DRAMs in SOJ-packages
- 2048 refresh cycles / 32 ms
- Tin-Lead contact pads (S - version)
- Gold contact pads (GS - version)

Ordering Information

Type	Ordering Code	Package	Description
HYM 328020S-60	Q67100-Q2001	L-SIM-72-15	DRAM Module (access time 60 ns)
HYM 328020S-70	on request	L-SIM-72-15	DRAM Module (access time 70 ns)
HYM 328020GS-60	Q67100-Q2008	L-SIM-72-15	DRAM Module (access time 60 ns)
HYM 328020GS-70	on request	L-SIM-72-15	DRAM Module (access time 70 ns)

The HYM 328020S/GS-60/-70 is a 32 M Byte DRAM module organized as 8 388 608 words by 32-bit in a 72-pin single-in-line package comprising sixteen HYB 5117400BJ 4M × 4 DRAMs in 300 mil wide SOJ-packages mounted together with sixteen 0.2 µF ceramic decoupling capacitors on a PC board.

The HYM 328020S/GS-60/-70 can also be used as a 16 777 360 words by 16-bits dynamic RAM module by means of connecting DQ0 and DQ16, DQ1 and DQ17, DQ2 and DQ18, ..., DQ15 and DQ31, respectively.

Each HYB 5117400BJ is described in the data sheet and is fully electrical tested and processed according to SIEMENS standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

The speed of the module can be detected by the use of four presence detect pins.

The common I/O feature on the HYM 328020S/GS-60/-70 dictates the use of early write cycles.

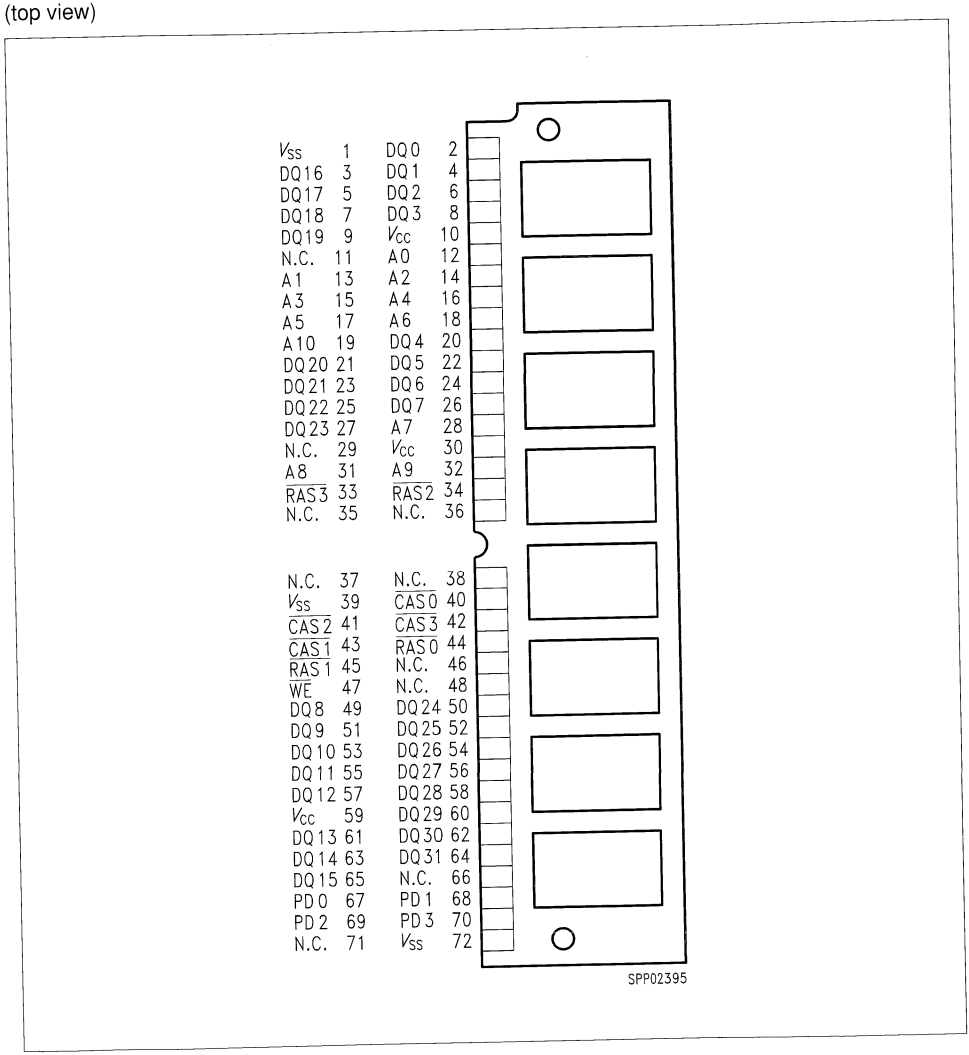
PinDefinitions and Functions

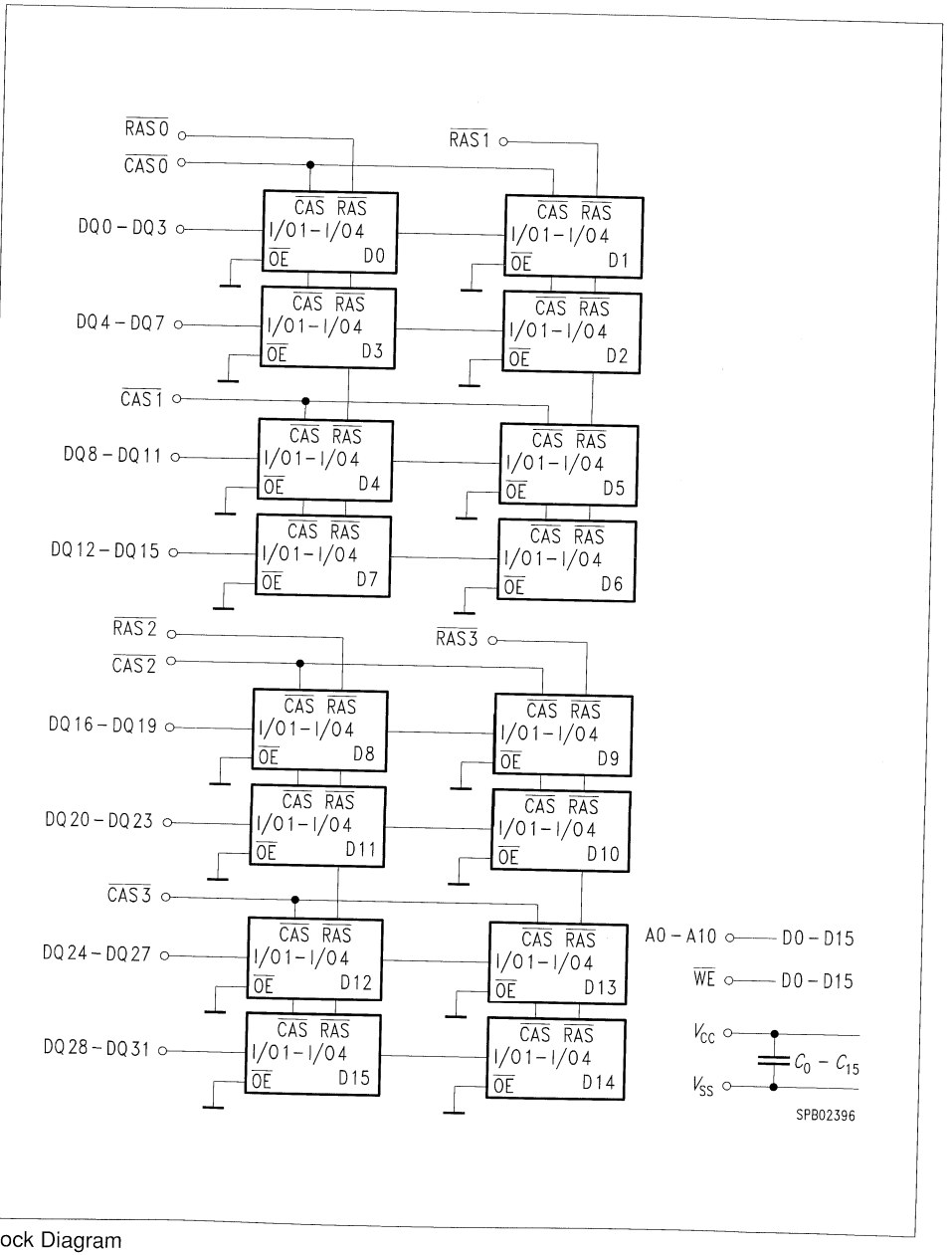
Pin No.	Function
A0-A10	Address Inputs
DQ0-DQ31	Data Input/Output
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
PD	Presence Detect Pin
N.C.	No Connection

Presence Detect Pins

	-60	-70
PD0	N.C.	N.C.
PD1	V_{SS}	V_{SS}
PD2	N.C.	V_{SS}
PD3	N.C.	N.C.

Pin Configuration
(top view)





Block Diagram

Absolute Maximum Ratings

Operation temperature range ..... 0 to + 70 °C
Storage temperature range ..... – 55 to 125 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 0.5 V to min (V_{CC} + 0.5, 7.0) V
Power supply voltage ..... – 1 to + 7 V
Power dissipation ..... 6.16 W
Data out current (short circuit) ..... 50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics[1)]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	V_{CC} + 0.5	V	
Input low voltage	V_{IL}	– 0.5	0.8	V	
Output high voltage (I_{OUT} = – 5 mA)	V_{OH}	2.4	–	V	
Output low voltage (I_{OUT} = 4.2 mA)	V_{OL}	–	0.4	V	
Input leakage current (0 V < V_{IN} < 6.5 V, all other pins = 0 V)	$I_{I(L)}$	– 20	20	µA	
Output leakage current (DO is disabled, 0 V < V_{OUT} < 5.5 V)	$I_{O(L)}$	– 10	10	µA	
Average V_{CC} supply current ($\overline{RAS}$, $\overline{CAS}$, address cycling, t_{RC} = t_{RC} min) -60 version -70 version	I_{CC1}	 – –	 880 800	 mA mA	2), 3)
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	32	mA	
Average V_{CC} supply current during $\overline{RAS}$ only refresh cycles ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min) -60 version -70 version	I_{CC3}	 – –	 880 800	 mA mA	2)

DC Characteristics[1] (cont'd)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current during fast page mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling, t_{PC} = t_{PC} min)	I_{CC4}				
-60 version		–	640	mA	[2],
-70 version		–	560	mA	[3]
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	–	16	mA	
Average V_{CC} supply current during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode ($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min)	I_{CC6}				
-60 version		–	640	mA	[2]
-70 version		–	720	mA	

Capacitance

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A10,$\overline{WE}$)	C_{I1}	–	120	pF
Input capacitance ($\overline{RAS0}$ - $\overline{RAS3}$)	C_{I2}	–	45	pF
Input capacitance ($\overline{CAS0}$ - $\overline{CAS3}$)	C_{I3}	–	40	pF
I/O capacitance (DQ0-DQ31)	C_{IO}	–	25	pF

AC Characteristics [4) 5)]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values				Unit
		HYM 328020S/GS-60		HYM 328020S/GS-70		
		min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	110	–	130	–	ns
Fast page mode cycle time	t_{PC}	40	–	45	–	ns
Access time from $\overline{RAS}$ [6) 11) 12)]	t_{RAC}	–	60	–	70	ns
Access time from $\overline{CAS}$ [6) 11)]	t_{CAC}	–	15	–	20	ns
Access time from column address [6) 12)]	t_{AA}	–	30	–	35	ns
Access time from $\overline{CAS}$ precharge [6)]	t_{CPA}	–	35	–	40	ns
$\overline{CAS}$ to output in low-Z [6)]	t_{CLZ}	0	–	0	–	ns
Output buffer turn-off delay [7)]	t_{OFF}	0	20	0	20	ns
Transition time (rise and fall) [5)]	t_T	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	40	–	50	–	ns
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	ns
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	60	200000	70	200000	ns
$\overline{CAS}$ precharge to $\overline{RAS}$ delay	t_{RHCP}	35	–	40	–	ns
$\overline{RAS}$ hold time	t_{RSH}	15	–	20	–	ns
$\overline{CAS}$ hold time	t_{CSH}	60	–	70	–	ns
$\overline{CAS}$ pulse width	t_{CAS}	15	10000	20	10000	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time [11)]	t_{RCD}	20	45	20	50	ns
$\overline{RAS}$ to column address delay time [12)]	t_{RAD}	15	30	15	35	ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	ns
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	ns
Row address hold time	t_{RAH}	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	ns
Column address hold time	t_{CAH}	15	–	15	–	ns

AC Characteristics[4) 5)] (cont'd)
T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values				Unit
		HYM 328020S/GS-60		HYM 328020S/GS-70		
		min.	max.	min.	max.	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	–	35	–	ns
Read command setup time	t_{RCS}	0	–	0	–	ns
Read command hold time [8)]	t_{RCH}	0	–	0	–	ns
Read command hold time ref. to $\overline{RAS}$ [8)]	t_{RRH}	0	–	0	–	ns
Write command hold time	t_{WCH}	10	–	15	–	ns
Write command pulse width	t_{WP}	10	–	15	–	ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	–	20	–	ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	–	20	–	ns
Data setup time [9)]	t_{DS}	0	–	0	–	ns
Data hold time [9)]	t_{DH}	15	–	15	–	ns
Refresh period	t_{REF}	–	32	–	32	ms
Write command setup time [10)]	t_{WCS}	0	–	0	–	ns
$\overline{CAS}$ setup time [13)]	t_{CSR}	10	–	10	–	ns
$\overline{CAS}$ hold time [13)]	t_{CHR}	10	–	10	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5	–	5	–	ns
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	ns
Write to $\overline{RAS}$ precharge time [13)]	t_{WRP}	10	–	10	–	ns
Write hold time ref. to $\overline{RAS}$ [13)]	t_{WRH}	10	–	10	–	ns

Notes

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading.
Specified values are measured with the output open.

4) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles out of which at least one cycle has to be a refresh cycle before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

5) V_{IH} (max) and V_{IL} (max) are reference levels for measuring timing of input signals.
Transition times are also measured between V_{IH} and V_{IL}.

6) Measured with a load equivalent of 2 TTL loads and 100 pF.

7) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.

8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9) These parameters are referenced to the $\overline{CAS}$ leading edge.

10) t_{WCS} is not a restrictive operating parameter. This is included in the data sheet as electrical characteristic only. If $t_{WCS} > t_{WCS}$ (min), the cycle is an early write cycle and data out pin will remain open (high impedance).

11) Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAS}.

12) Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.

13) For $\overline{CAS}$-before-$\overline{RAS}$ cycles only.

1M × 36-Bit Dynamic RAM Module (2M × 18-Bit Dynamic RAM Module)

HYM 361120/40S/GS-60/-70

Advanced Information

- 1 048 576 words by 36-bit organization (alternative 2 097 152 words by 18-bit)
- Fast access and cycle time
  60 ns access time
  110 ns cycle time (-60 version)
  70 ns access time
  130 ns cycle time (-70 version)
- Fast page mode capability with
  40 ns cycle time (-60 version)
  45 ns cycle time (-70 version)
- Single + 5 V (± 10 %) supply
- Low power dissipation
  max. 6820 mW active (-60 version)
  max. 6160 mW active (-70 version)
  CMOS – 66 mW standby
  TTL – 132 mW standby
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$-only-refresh, Hidden refresh
- 12 decoupling capacitors mounted on substrate
- All inputs, outputs and clock fully TTL compatible
- 72 pin Single in-Line Memory Module
- Utilizes four 1M × 1-DRAMs and eight 1M × 4-DRAMs in 300 mil SOJ packages
- 1024 refresh cycles/16 ms
- Tin-Lead contact pads (S - version)
- Gold contact pads (GS - version)
- HYM 321140S: single sided module with 31.75 mm (1250 mil) height
- HYM 321120S: double sided module with 25.40 mm (1000 mil) height

Ordering Information

Type	Ordering Code	Package	Descriptions
HYM 361140S-60	Q67100-Q959	L-SIM-72-8	DRAM module (access time 60 ns)
HYM 361140S-70	Q67100-Q958	L-SIM-72-8	DRAM module (access time 70 ns)
HYM 361120S-60	Q67100-Q942	L-SIM-72-3	DRAM module (access time 60 ns)
HYM 361120S-70	Q67100-Q741	L-SIM-72-3	DRAM module (access time 70 ns)
HYM 361140GS-60	Q67100-Q1019	L-SIM-72-8	DRAM module (access time 60 ns)
HYM 361140GS-70	Q67100-Q651	L-SIM-72-8	DRAM module (access time 70 ns)
HYM 361120GS-60	Q67100-Q961	L-SIM-72-3	DRAM module (access time 60 ns)
HYM 361120GS-70	Q67100-Q960	L-SIM-72-3	DRAM module (access time 70 ns)

The HYM 361120/40S/GS-60/-70 is a 4 MByte DRAM module organized as 1 048 576 words by 36-bit in a 72-pin single-in-line package comprising four HYB 511000BJ 1M × 1 DRAMs and eight HYB 514400BJ 1M × 4 DRAMs in 300 mil wide SOJ-packages mounted together with twelve 0.2 µF ceramic decoupling capacitors on a PC board.

The HYM 361120/40S/GS-60/-70 can also be used as a 2 097 152 words by 18-bits dynamic RAM module by means of connecting DQ0 and DQ18, DQ1 and DQ19, DQ2 and DQ20, ..., DQ17 and DQ35, respectively.

Each HYB 511000BJ and HYB 514400BJ is described in the data sheet and is fully electrically tested and processed according to Siemens standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

The speed of the module can be detected by the use of four presence detect pins.

The common I/O feature on the HYM 361120/40S/GS-60/-70 dictates the use of early write cycles.

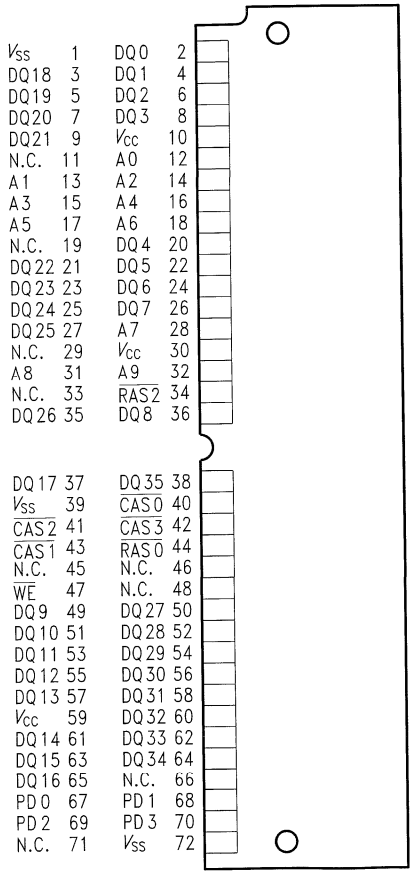
Pin Definitions and Functions

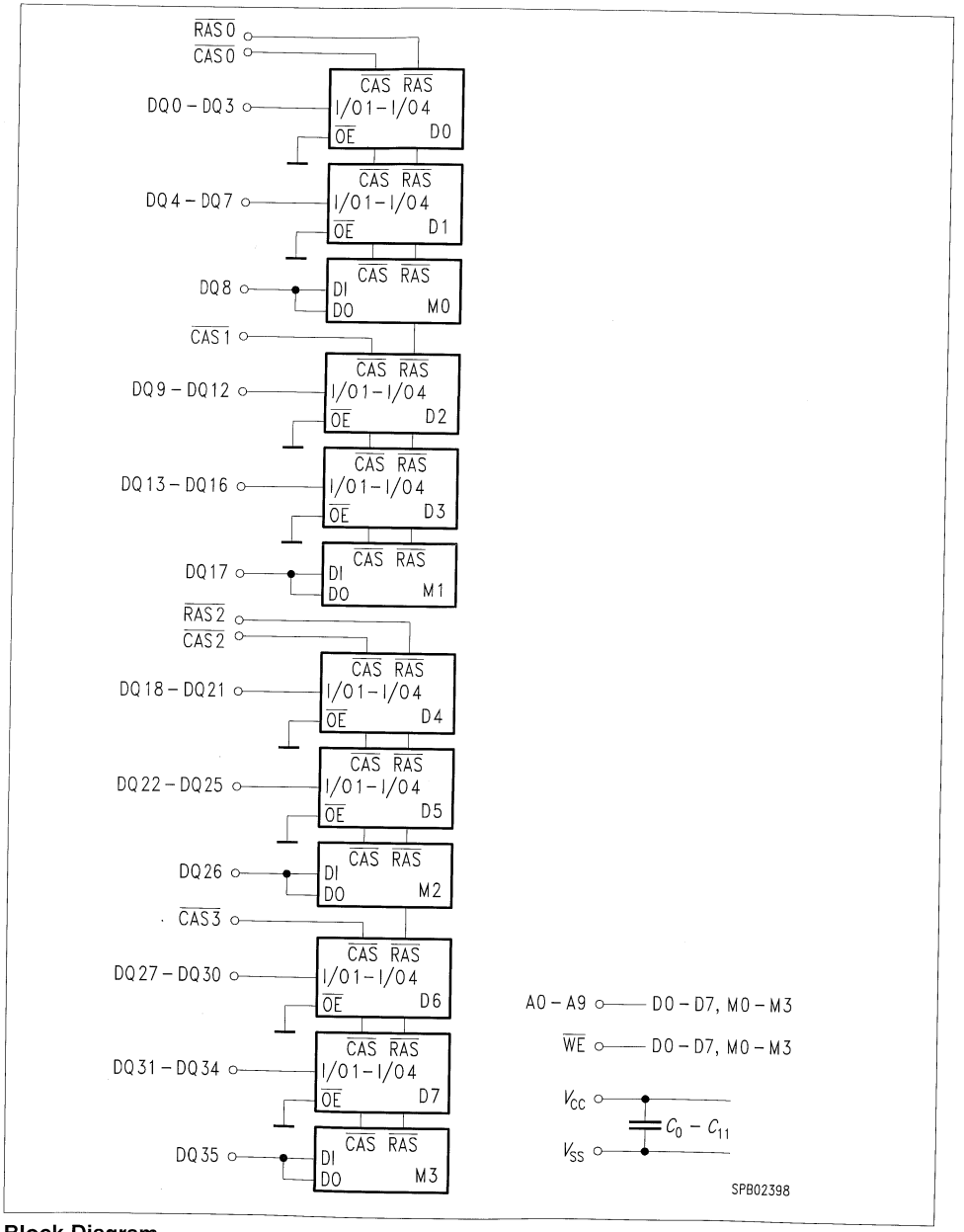
Pin No.	Function
A0-A9	Address Inputs
DQ0-DQ35	Data Input/Output
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
PD	Presence Detect Pin
N.C.	No Connection

Presence Detect Pins

	-60	-70
PD0	V_{SS}	V_{SS}
PD1	V_{SS}	V_{SS}
PD2	N.C.	V_{SS}
PD3	N.C.	N.C.

Pin Configuration
(top view)





Block Diagram

Absolute Maximum Ratings

Operating temperature range ..... 0 to + 70 °C
Storage temperature range ..... – 55 to + 125 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 1 to + 7 V
Power supply voltage ..... – 1 to + 7 V
Power dissipation ..... 8.68 W
Data out current (short circuit) ..... 50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics [1]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	5.5	V	–
Input low voltage	V_{IL}	– 1.0	0.8	V	–
Output high voltage (I_{OUT} = – 5 mA)	V_{OH}	2.4	–	V	–
Output low voltage (I_{OUT} = 4.2 mA)	V_{OL}	–	0.4	V	–
Input leakage current (0 V < V_{IN} < 6.5 V, all other pins = 0 V)	$I_{I(L)}$	– 20	20	µA	–
Output leakage current (DO is disabled, 0 V < V_{OUT} < 5.5 V)	$I_{O(L)}$	– 10	10	µA	–
Average V_{CC} supply current:	I_{CC1}				
-60 version		–	1240	mA	2), 3)
-70 version		–	1120	mA	
($\overline{RAS}$, $\overline{CAS}$, address cycling, t_{RC} = t_{RC} min.)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	24	mA	–
Average V_{CC} supply current during $\overline{RAS}$ only refresh cycles:	I_{CC3}			mA	2)
-60 version		–	1240	mA	
-70 version		–	1120		
($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)					

DC Characteristics (cont'd) [1]

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current during fast page mode:	I_{CC4}				[2], [3]
-60 version		–	840	mA	
-70 version		–	720	mA	
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling t_{PC} = t_{PC} min.)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	–	12	mA	–
Average V_{CC} supply current during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode:	I_{CC6}				[1]
-60 version		–	1240	mA	
-70 version		–	1120	mA	
($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min.)					

Capacitance
T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A9)	C_{I1}	–	80	pF
Input capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	C_{I2}	–	42	pF
Input capacitance ($\overline{CAS0}$-$\overline{CAS3}$)	C_{I3}	–	35	pF
Input capacitance ($\overline{WE}$)	C_{I4}	–	80	pF
I/O capacitance (DQ0-DQ7, DQ9-DQ16, DQ18-DQ25, DQ27-DQ34)	C_{IO1}	–	15	pF
I/O capacitance (DQ8, DQ17, DQ26, DQ35)	C_{IO2}	–	20	pF

AC Characteristics [4) 5)]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values				Unit
		HYM 361120/40S/GS-60		HYM 361120/40S/GS-70		
		min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	110	–	130	–	ns
Fast page mode cycle time	t_{PC}	40	–	45	–	ns
Access time from $\overline{RAS}$ [6) 11) 12)]	t_{RAC}	–	60	–	70	ns
Access time from $\overline{CAS}$ [6) 11)]	t_{CAC}	–	15	–	20	ns
Access time from column address [6) 12)]	t_{AA}	–	30	–	35	ns
Access time from $\overline{CAS}$ precharge [6)]	t_{CPA}	–	35	–	40	ns
$\overline{CAS}$ to output in low-Z [6)]	t_{CLZ}	0	–	0	–	ns
Output buffer turn-off delay [7)]	t_{OFF}	0	20	0	20	ns
Transition time (rise and fall) [5)]	t_T	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	40	–	50	–	ns
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	ns
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	60	200000	70	200000	ns
$\overline{CAS}$ precharge to $\overline{RAS}$ delay	t_{RHCP}	35	–	40	–	ns
$\overline{RAS}$ hold time	t_{RSH}	15	–	20	–	ns
$\overline{CAS}$ hold time	t_{CSH}	60	–	70	–	ns
$\overline{CAS}$ pulse width	t_{CAS}	15	10000	20	10000	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time [11)]	t_{RCD}	20	45	20	50	ns
$\overline{RAS}$ to column address delay time [12)]	t_{RAD}	15	30	15	35	ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	ns
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	ns
Row address hold time	t_{RAH}	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	ns
Column address hold time	t_{CAH}	15	–	15	–	ns

AC Characteristics (cont'd) [4] [5]
T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values				Unit
		HYM 361120/40S/GS-60		HYM 361120/40S/GS-70		
		min.	max.	min.	max.	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	–	35	–	ns
Read command setup time	t_{RCS}	0	–	0	–	ns
Read command hold time [8]	t_{RCH}	0	–	0	–	ns
Read command hold time ref. to $\overline{RAS}$ [8]	t_{RRH}	0	–	0	–	ns
Write command hold time	t_{WCH}	10	–	15	–	ns
Write command pulse width	t_{WP}	10	–	15	–	ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	–	20	–	ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	–	20	–	ns
Data setup time [9]	t_{DS}	0	–	0	–	ns
Data hold time [9]	t_{DH}	15	–	15	–	ns
Refresh period	t_{REF}	–	16	–	16	ms
Write command setup time [10]	t_{WCS}	0	–	0	–	ns
$\overline{CAS}$ setup time [13]	t_{CSR}	5	–	5	–	ns
$\overline{CAS}$ hold time [13]	t_{CHR}	15	–	15	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	0	–	0	–	ns
$\overline{CAS}$ precharge time [13]	t_{CP}	10	–	10	–	ns
Write to $\overline{RAS}$ precharge time [13]	t_{WRP}	10	–	10	–	ns
Write to time ref. to $\overline{RAS}$ [13]	t_{WRH}	10	–	10	–	ns

Notes

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.

4) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles out of which at least one cycle has to be a refresh cycle before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

5) V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.

6) Measured with a load equivalant of 2 TTL loads and 100 pF.

7) t_{OFF} (max.) defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.

8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9) These parameters are referenced to the $\overline{CAS}$ leading edge.

10) t_{WCS} is not a restrictive operating parameter. This is included in the data sheet as electrical characteristic only. If $t_{WCS} > t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance).

11) Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

12) Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

13) For $\overline{CAS}$-before-$\overline{RAS}$ cycles only.

2M x 36-Bit Dynamic RAM Module

HYM 362140S/GS-60/-70

Advanced Information

- 2 097 152 words by 36-bit organization (alternative 4 194 304 words by 18-bit)
- Fast access and cycle time
  60 ns access time
  110 ns cycle time (-60 version)
  70 ns access time
  130 ns cycle time (-70 version)
- Fast page mode capability with
  40 ns cycle time (-60 version)
  45 ns cycle time (-70 version)
- Single + 5 V (± 10 %) supply
- Low power dissipation
  max. 6952 mW active (-60 version)
  max. 6292 mW active (-70 version)
  CMOS – 132 mW standby
  TTL – 264 mW standby
- $\overline{CAS}$-before-$\overline{RAS}$ refresh
  $\overline{RAS}$-only-refresh
  Hidden-refresh
- 12 decoupling capacitors mounted on substrate
- All inputs, outputs and clocks fully TTL compatible
- 72 pin Single in-Line Memory Module with 31.75 mm height
- Utilizes eight 1M × 1-DRAMs and sixteen 1M × 4 DRAMs in 300 mil SOJ-packages
- 1024 refresh cycles / 16 ms
- Tin-Lead contact pads (S - version)
- God contact pads (GS - version)

Ordering Information

Type	Ordering Code	Package	Description
HYM 362140S-60	Q67100-Q955	L-SIM-72-8	DRAM Module (access time 60 ns)
HYM 362140S-70	Q67100-Q954	L-SIM-72-8	DRAM Module (access time 70 ns)
HYM 362140GS-60	Q67100-Q957	L-SIM-72-8	DRAM Module (access time 60 ns)
HYM 362140GS-70	Q67100-Q956	L-SIM-72-8	DRAM Module (access time 70 ns)

The HYM 362140S/GS-60/-70 is a 8 M Byte DRAM module organized as 2 097 152 words by 36-bit in a 72-pin single-in-line package comprising eight HYB 511000BJ 1M × 1 DRAMs and sixteen HYB 514400BJ 1M × 4 DRAMs in 300 mil wide SOJ-packages mounted together with twelve 0.2 µF ceramic decoupling capacitors on a PC board.

The HYM 362140S/GS-60/-70 can also be used as a 4 194 304 words by 18-bits dynamic RAM module by means of connecting DQ0 and DQ18, DQ1 and DQ19, DQ2 and DQ20, ..., DQ17 and DQ35, respectively.

Each HYB 511000BJ and HYB 514400BJ is described in the data sheet and is fully electrical tested and processed according to SIEMENS standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

The speed of the module can be detected by the use of four presence detect pins.

The common I/O feature on the HYM 362140S/GS-60/-70 dictates the use of early write cycles.

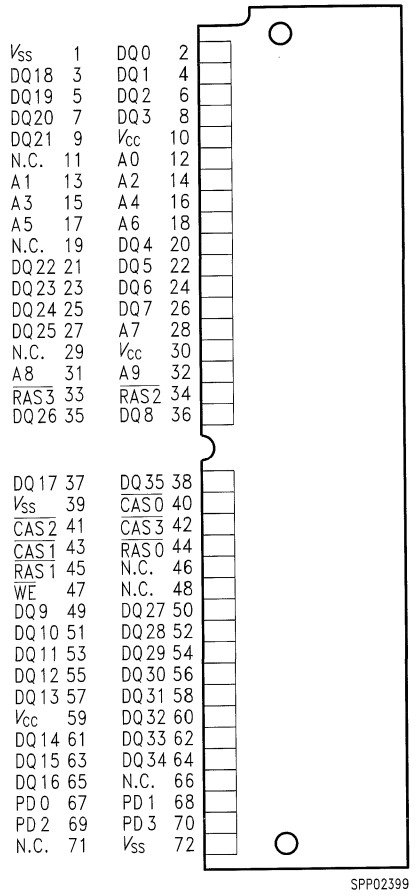
Pin Definitions and Functions

Pin No.	Function
A0-A9	Address Inputs
DQ0-DQ35	Data Input/Output
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
PD	Presence Detect Pin
N.C.	No Connection

Presence Detect Pins

	-60	-70
PD0	N.C.	N.C.
PD1	N.C.	N.C.
PD2	N.C.	V_{SS}
PD3	N.C.	N.C.

Pin Configuration
(top view)



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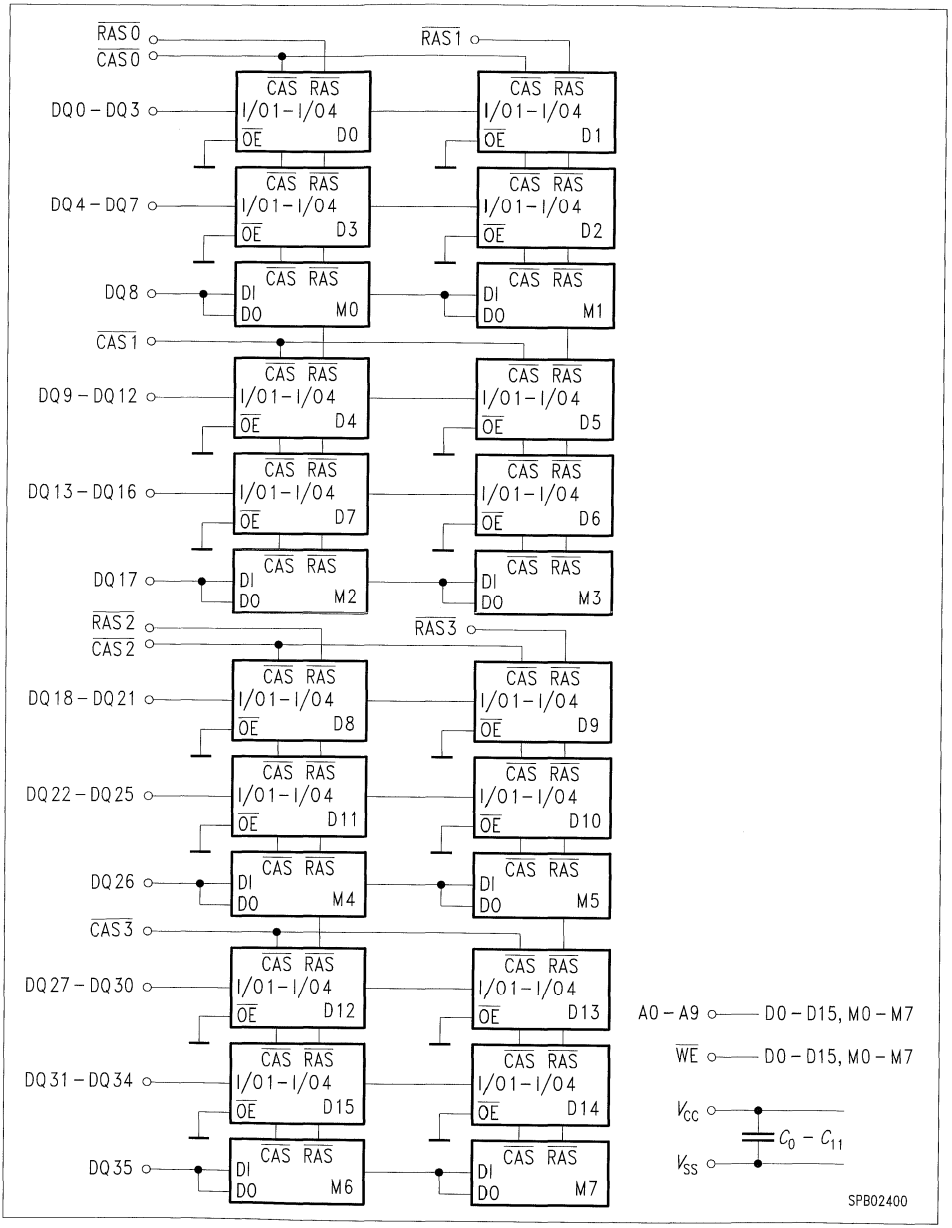


Block Diagram

Absolute Maximum Ratings

Operation temperature range ..... 0 to + 70 °C
Storage temperature range..... – 55 to 125 °C
Soldering temperature ..... 260 °C
Soldering time..... 10 s
Input/output voltage ..... – 1 to + 7 V
Power supply voltage..... – 1 to + 7 V
Power dissipation..... 8.9 W
Data out current (short circuit) ..... 50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics[1)]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	5.5	V	
Input low voltage	V_{IL}	– 1.0	0.8	V	
Output high voltage (I_{OUT} = – 5 mA)	V_{OH}	2.4	–	V	
Output low voltage (I_{OUT} = 4.2 mA)	V_{OL}	–	0.4	V	
Input leakage current (0 V < V_{IN} < 6.5 V, all other pins = 0 V)	$I_{I(L)}$	– 20	20	µA	
Output leakage current (DO is disabled, 0 V < V_{OUT} < 5.5 V)	$I_{O(L)}$	– 20	20	µA	
Average V_{CC} supply current ($\overline{RAS}$, $\overline{CAS}$, address cycling, t_{RC} = t_{RC} min)	I_{CC1}				
-60 version		–	1264	mA	2)
-70 version		–	1144	mA	3)
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	48	mA	
Average V_{CC} supply current during $\overline{RAS}$ only refresh cycles ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min)	I_{CC3}				
-60 version		–	1264	mA	2)
-70 version		–	1144	mA	

DC Characteristics[1] (cont'd)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current during fast page mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling, t_{PC} = t_{PC} min)	I_{CC4}				
-60 version		–	864	mA	[2]
-70 version		–	744	mA	[3]
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	–	24	mA	
Average V_{CC} supply current during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode ($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min)	I_{CC6}				
-60 version		–	1264	mA	[2]
-70 version		–	1144	mA	

Capacitance

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A9, $\overline{WE}$)	C_{I1}	–	180	pF
Input capacitance ($\overline{RAS0}$-$\overline{RAS3}$, $\overline{CAS0}$-$\overline{CAS3}$)	C_{I2}	–	45	pF
I/O capacitance (DQ0-DQ7, DQ9-DQ16, DQ18-DQ25, DQ27-DQ34)	C_{IO1}	–	25	pF
I/O capacitance (DQ8, DQ17, DQ26, DQ35)	C_{IO2}	–	35	pF

AC Characteristics [4) 5)]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values				Unit
		HYM 362140S/GS-60		HYM 362140S/GS-70		
		min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	110	–	130	–	ns
Fast page mode cycle time	t_{PC}	40	–	45	–	ns
Access time from $\overline{RAS}$ [6) 11) 12)]	t_{RAC}	–	60	–	70	ns
Access time from $\overline{CAS}$ [6) 11)]	t_{CAC}	–	15	–	20	ns
Access time from column address [6) 12)]	t_{AA}	–	30	–	35	ns
Access time from $\overline{CAS}$ precharge [6)]	t_{CPA}	–	35	–	40	ns
$\overline{CAS}$ to output in low-Z [6)]	t_{CLZ}	0	–	0	–	ns
Output buffer turn-off delay [7)]	t_{OFF}	0	20	0	20	ns
Transition time (rise and fall) [5)]	t_T	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	40	–	50	–	ns
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	ns
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	60	200000	70	200000	ns
$\overline{CAS}$ precharge to $\overline{RAS}$ delay	t_{RHCP}	35	–	40	–	ns
$\overline{RAS}$ hold time	t_{RSH}	15	–	20	–	ns
$\overline{CAS}$ hold time	t_{CSH}	60	–	70	–	ns
$\overline{CAS}$ pulse width	t_{CAS}	15	10000	20	10000	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time [11)]	t_{RCD}	20	45	20	50	ns
$\overline{RAS}$ to column address delay time [12)]	t_{RAD}	15	30	15	35	ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	ns
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	ns
Row address hold time	t_{RAH}	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	ns
Column address hold time	t_{CAH}	15	–	15	–	ns

AC Characteristics[4) 5)] (cont'd)
T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values				Unit
		HYM 362140S/GS-60		HYM 362140S/GS-70		
		min.	max.	min.	max.	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	–	35	–	ns
Read command setup time	t_{RCS}	0	–	0	–	ns
Read command hold time [8)]	t_{RCH}	0	–	0	–	ns
Read command hold time ref. to $\overline{RAS}$ [8)]	t_{RRH}	0	–	0	–	ns
Write command hold time	t_{WCH}	10	–	15	–	ns
Write command pulse width	t_{WP}	10	–	15	–	ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	–	20	–	ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	–	20	–	ns
Data setup time [9)]	t_{DS}	0	–	0	–	ns
Data hold time [9)]	t_{DH}	15	–	15	–	ns
Refresh period	t_{REF}	–	16	–	16	ms
Write command setup time [10)]	t_{WCS}	0	–	0	–	ns
$\overline{CAS}$ setup time [13)]	t_{CSR}	5	–	5	–	ns
$\overline{CAS}$ hold time [13)]	t_{CHR}	15	–	15	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	0	–	0	–	ns
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	ns
Write to $\overline{RAS}$ precharge time [13)]	t_{WRP}	10	–	10	–	ns
Write hold time ref. to $\overline{RAS}$ [13)]	t_{WRH}	10	–	10	–	ns

Notes:

1) All voltages are referenced to V_{SS}.
2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
3) I_{CC1} and I_{CC4} depend on output loading.
   Specified values are measured with the output open.
4) An initial pause of 200 µs is required after power-up followed by 8 RAS cycles out of which at least one cycle has to be a refresh cycle before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS cycles are required.
5) $V_{IH\,(max)}$ and $V_{IL\,(max)}$ are reference levels for measuring timing of input signals.
   Transition times are also measured between V_{IH} and V_{IL}.
6) Measured with a load equivalent of 2 TTL loads and 100 pF.
7) $t_{OFF\,(max)}$ defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.
8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9) These parameters are referenced to the CAS leading edge.
10) t_{WCS} is not a restrictive operating parameter. This is included in the data sheet as electrical characteristic only. If $t_{WCS} > t_{WCS\,(min)}$, the cycle is an early write cycle and data out pin will remain open (high impedance).
11) Operation within the $t_{RCD\,(max)}$ limit insures that $t_{RAC\,(max)}$ can be met. $t_{RCD\,(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD\,(max)}$ limit, then access time is controlled by t_{CAS}.
12) Operation within the $t_{RAD\,(max)}$ limit insures that $t_{RAC\,(max)}$ can be met. $t_{RAD\,(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD\,(max)}$ limit, then access time is controlled by t_{AA}.
13) For CAS-before-RAS cycles only.

4M x 36-Bit Dynamic RAM Module

HYM 364020S/GS-60/-70

Preliminary Information

- 4 194 304 words by 36-Bit organization (alternative 8 388 608 words by 18-bit)
- Fast access and cycle time
  60 ns access time
  110 ns cycle time (-60 version)
  70 ns access time
  130 ns cycle time (-70 version)
- Fast page mode capability
  40 ns cycle time (-60 version)
  45 ns cycle time (-70 version)
- Single + 5 V (± 10 %) supply
- Low power dissipation
  max. 7260 mW active (-60 version)
  max. 6600 mW active (-70 version)
  CMOS – 66 mW standby
  TTL – 132 mW standby
- $\overline{CAS}$-before-$\overline{RAS}$ refresh
  $\overline{RAS}$-only-refresh
  Hidden-refresh
- 12 decoupling capacitors mounted on substrate
- All inputs, outputs and clocks fully TTL compatible
- 72 pin Single in-Line Memory Module (L-SIM-72) with 22.9 mm (900 mil) height
- Utilizes eight 4Mx4-DRAMs and four 4M x 1-DRAMs in SOJ-packages
- 2048 refresh cycles / 32 ms
- Tin-Lead contact pads (S - version)
- Gold contact pads (GS - version)

Ordering Information

Type	Ordering Code	Package	Description
HYM 364020S-60	Q67100-Q2006	L-SIM-72-12	DRAM Module (access time 60 ns)
HYM 364020S-70	on request	L-SIM-72-12	DRAM Module (access time 70 ns)
HYM 364020GS-60	Q67100-Q982	L-SIM-72-12	DRAM Module (access time 60 ns)
HYM 364020GS-70	Q67100-Q983	L-SIM-72-12	DRAM Module (access time 70 ns)

The HYM 364020S/GS-60/-70 is a 16 M Byte DRAM module organized as 4 194 304 words by 36-Bit in a 72-pin single-in-line package comprising eight HYB 5117400BJ 4M × 4 DRAMs and four HYB 514100BJ 4M x 1 DRAMS in 300 mil wide SOJ-packages mounted together with twelve 0.2 µF ceramic decoupling capacitors on a PC board.

The HYM 364020S/GS-60/-70 can also be used as a 8 388 608 words by 18-bits dynamic RAM module by means of connecting DQ0 and DQ18, DQ1 and DQ19, DQ2 and DQ20, ..., DQ17 and DQ35, respectively.

Each HYB 5117400BJ and HYB 514100BJ is described in the data sheet and is fully electrical tested and processed according to SIEMENS standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

The speed of the module can be detected by the use of four presence detect pins.

The common I/O feature on the HYM 364020S/GS-60/-70 dictates the use of early write cycles.

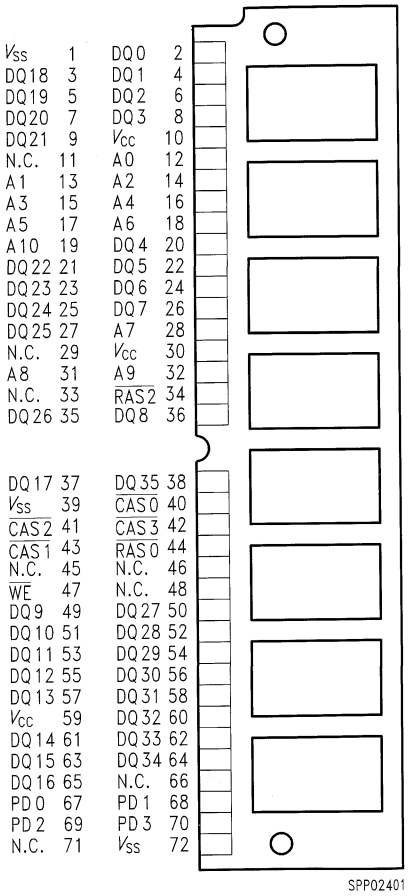
Pin Definitions and Functions

Pin No.	Function
A0-A10	Address Inputs
DQ0-DQ35	Data Input/Output
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
PD	Presence Detect Pin
N.C.	No Connection

Presence Detect Pins

	-60	-70
PD0	V_{SS}	V_{SS}
PD1	N.C.	N.C.
PD2	N.C.	V_{SS}
PD3	N.C.	N.C.

Pin Configuration
(top view)



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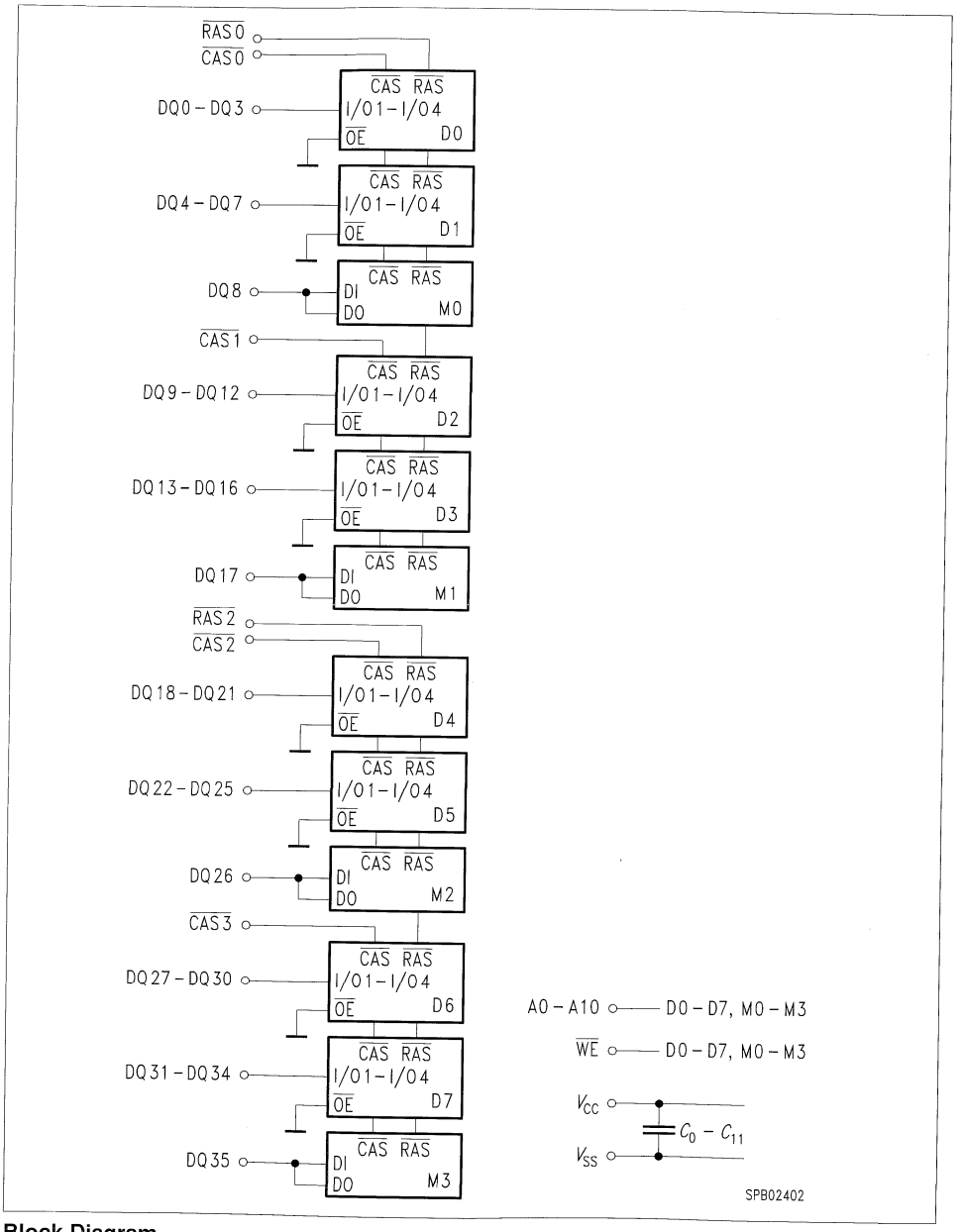


Block Diagram

Absolute Maximum Ratings

Operation temperature range ..... 0 to + 70 °C
Storage temperature range ..... – 55 to 125 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 0.5 V to min (V_{CC} + 0.5, 7.0) V
Power supply voltage ..... – 1 to + 7 V
Power dissipation ..... 9.3 W
Data out current (short circuit) ..... 50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics[1)]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	V_{CC} + 0.5	V	
Input low voltage	V_{IL}	– 0.5	0.8	V	
Output high voltage (I_{OUT} = – 5 mA)	V_{OH}	2.4	–	V	
Output low voltage (I_{OUT} = 4.2 mA)	V_{OL}	–	0.4	V	
Input leakage current (0 V < V_{IN} < 6.5 V, all other pins = 0 V)	$I_{I(L)}$	– 20	20	µA	
Output leakage current (DO is disabled, 0 V < V_{OUT} < 5.5 V)	$I_{O(L)}$	– 10	10	µA	
Average V_{CC} supply current ($\overline{RAS}$, $\overline{CAS}$, address cycling, t_{RC} = t_{RC} min)	I_{CC1}				
-60 version		–	1320	mA	2)
-70 version		–	1200	mA	3)
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	24	mA	
Average V_{CC} supply current during $\overline{RAS}$ only refresh cycles ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min)	I_{CC3}				
-60 version		–	1320	mA	2)
-70 version		–	1200	mA	

DC Characteristics[1] (cont'd)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current during fast page mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling, t_{PC} = t_{PC} min)	I_{CC4}				
-60 version		–	920	mA	[2],
-70 version		–	840	mA	[3]
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	–	12	mA	
Average V_{CC} supply current during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode ($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min)	I_{CC6}				
-60 version		–	1320	mA	[2]
-70 version		–	1200	mA	

Capacitance

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A10, $\overline{WE}$)	C_{I1}	–	90	pF
Input capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	C_{I2}	–	45	pF
Input capacitance ($\overline{CAS0}$ - $\overline{CAS3}$)	C_{I3}	–	40	pF
I/O capacitance(DQ0-DQ7,DQ9-DQ16,DQ18-DQ25,DQ27-DQ34)	C_{IO1}	–	20	pF
I/O capacitcance (DQ8,DQ17,DQ26,DQ35)	C_{IO2}	–	25	pF

AC Characteristics [4) 5)]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values				Unit
		HYM 364020S/GS-60		HYM 364020S/GS-70		
		min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	110	–	130	–	ns
Fast page mode cycle time	t_{PC}	40	–	45	–	ns
Access time from $\overline{RAS}$ [6) 11) 12)]	t_{RAC}	–	60	–	70	ns
Access time from $\overline{CAS}$ [6) 11)]	t_{CAC}	–	15	–	20	ns
Access time from column address [6) 12)]	t_{AA}	–	30	–	35	ns
Access time from $\overline{CAS}$ precharge [6)]	t_{CPA}	–	35	–	40	ns
$\overline{CAS}$ to output in low-Z [6)]	t_{CLZ}	0	–	0	–	ns
Output buffer turn-off delay [7)]	t_{OFF}	0	20	0	20	ns
Transition time (rise and fall) [5)]	t_T	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	40	–	50	–	ns
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	ns
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	60	200000	70	200000	ns
$\overline{CAS}$ precharge to $\overline{RAS}$ delay	t_{RHCP}	35	–	40	–	ns
$\overline{RAS}$ hold time	t_{RSH}	15	–	20	–	ns
$\overline{CAS}$ hold time	t_{CSH}	60	–	70	–	ns
$\overline{CAS}$ pulse width	t_{CAS}	15	10000	20	10000	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time [11)]	t_{RCD}	20	45	20	50	ns
$\overline{RAS}$ to column address delay time [12)]	t_{RAD}	15	30	15	35	ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	ns
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	ns
Row address hold time	t_{RAH}	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	ns
Column address hold time	t_{CAH}	15	–	15	–	ns

AC Characteristics[4) 5)] (cont'd)
T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values				Unit
		HYM 364020S/GS-60		HYM 364020S/GS-70		
		min.	max.	min.	max.	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	–	35	–	ns
Read command setup time	t_{RCS}	0	–	0	–	ns
Read command hold time [8)]	t_{RCH}	0	–	0	–	ns
Read command hold time ref. to $\overline{RAS}$ [8)]	t_{RRH}	0	–	0	–	ns
Write command hold time	t_{WCH}	10	–	15	–	ns
Write command pulse width	t_{WP}	10	–	15	–	ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	–	20	–	ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	–	20	–	ns
Data setup time [9)]	t_{DS}	0	–	0	–	ns
Data hold time [9)]	t_{DH}	15	–	15	–	ns
Refresh period	t_{REF}	–	32	–	32	ms
Write command setup time [10)]	t_{WCS}	0	–	0	–	ns
$\overline{CAS}$ setup time [13)]	t_{CSR}	10	–	10	–	ns
$\overline{CAS}$ hold time [13)]	t_{CHR}	10	–	10	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5	–	5	–	ns
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	ns
Write to $\overline{RAS}$ precharge time [13)]	t_{WRP}	10	–	10	–	ns
Write hold time ref. to $\overline{RAS}$ [13)]	t_{WRH}	10	–	10	–	ns

Notes

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading.
Specified values are measured with the output open.

4) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles out of which at least one cycle has to be a refresh cycle before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

5) V_{IH} (max) and V_{IL} (max) are reference levels for measuring timing of input signals.
Transition times are also measured between V_{IH} and V_{IL}.

6) Measured with a load equivalent of 2 TTL loads and 100 pF.

7) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.

8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9) These parameters are referenced to the $\overline{CAS}$ leading edge.

10) t_{WCS} is not a restrictive operating parameter. This is included in the data sheet as electrical characteristic only. If $t_{WCS} > t_{WCS}$ (min), the cycle is an early write cycle and data out pin will remain open (high impedance).

11) Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAS}.

12) Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.

13) For $\overline{CAS}$-before-$\overline{RAS}$ cycles only.

SIEMENS

8M x 36-Bit Dynamic RAM Module

HYM 368020S/GS-60/-70

Preliminary Information

- 8 388 608 words by 36-bit organization (alternative 16 777 216 words by 18-bit)
- Fast access and cycle time
  60 ns access time
  110 ns cycle time (-60 version)
  70 ns access time
  130 ns cycle time (-70 version)
- Fast page mode capability
  40 ns cycle time (-60 version)
  45 ns cycle time (-70 version)
- Single + 5 V (± 10 %) supply
- Low power dissipation
  max. 7260 mW active (-60 version)
  max. 6600 mW active (-70 version)
  CMOS – 132 mW standby
  TTL – 264 mW standby
- $\overline{CAS}$-before-$\overline{RAS}$ refresh
  $\overline{RAS}$-only-refresh
  Hidden-refresh
- 24 decoupling capacitors mounted on substrate
- All inputs, outputs and clocks fully TTL compatible
- 72 pin Single in-Line Memory Module (L-SIM-72-14) with 31.75 mm height
- Utilizes sixteen 4Mx4-DRAMs and eight 4 M x 1 DRAMs in 300 mil wide SOJ-packages
- 2048 refresh cycles / 32 ms
- Tin-Lead contact pads (S- version)
- Gold contact pads (GS - version)

Ordering Information

Type	Ordering Code	Package	Description
HYM 368020S-60	Q67100-Q985	L-SIM-72-14	DRAM Module (access time 60 ns)
HYM 368020S-70	Q67100-Q986	L-SIM-72-14	DRAM Module (access time 70 ns)
HYM 368020GS-60	Q67100-Q2007	L-SIM-72-14	DRAM Module (access time 60 ns)
HYM 368020GS-70	on request	L-SIM-72-14	DRAM Module (access time 70 ns)

The HYM 368020S/GS-60/-70 is a 32 M Byte DRAM module organized as 8 388 608 words by 36-Bit in a 72-pin single-in-line package comprising sixteen HYB 5117400BJ 4M × 4 DRAMs and eight HYB 514100BJ 4M x 1 DRAMs in 300 mil wide SOJ-packages mounted together with 24 0.2 µF ceramic decoupling capacitors on a PC board.

The HYM 368020S/GS-60/-70 can also be used as a 16 777 360 words by 18-bits dynamic RAM module by means of connecting DQ0 and DQ18, DQ1 and DQ19, DQ2 and DQ20, ..., DQ17 and DQ35, respectively.

Each HYB 5117400BJ and HYB 514100BJ is described in the data sheet and is fully electrical tested and processed according to SIEMENS standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

The speed of the module can be detected by the use of four presence detect pins.

The common I/O feature on the HYM 368020S/GS-60/-70 dictates the use of early write cycles.

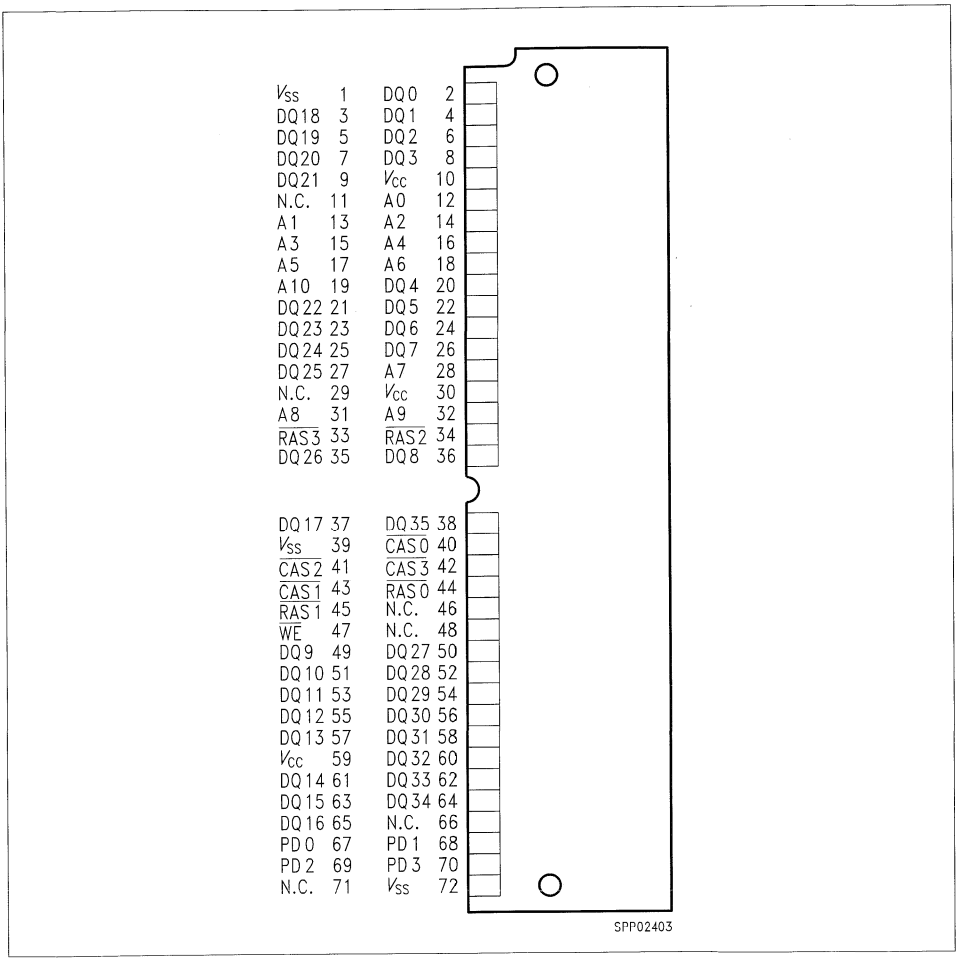
Pin Definitions and Functions

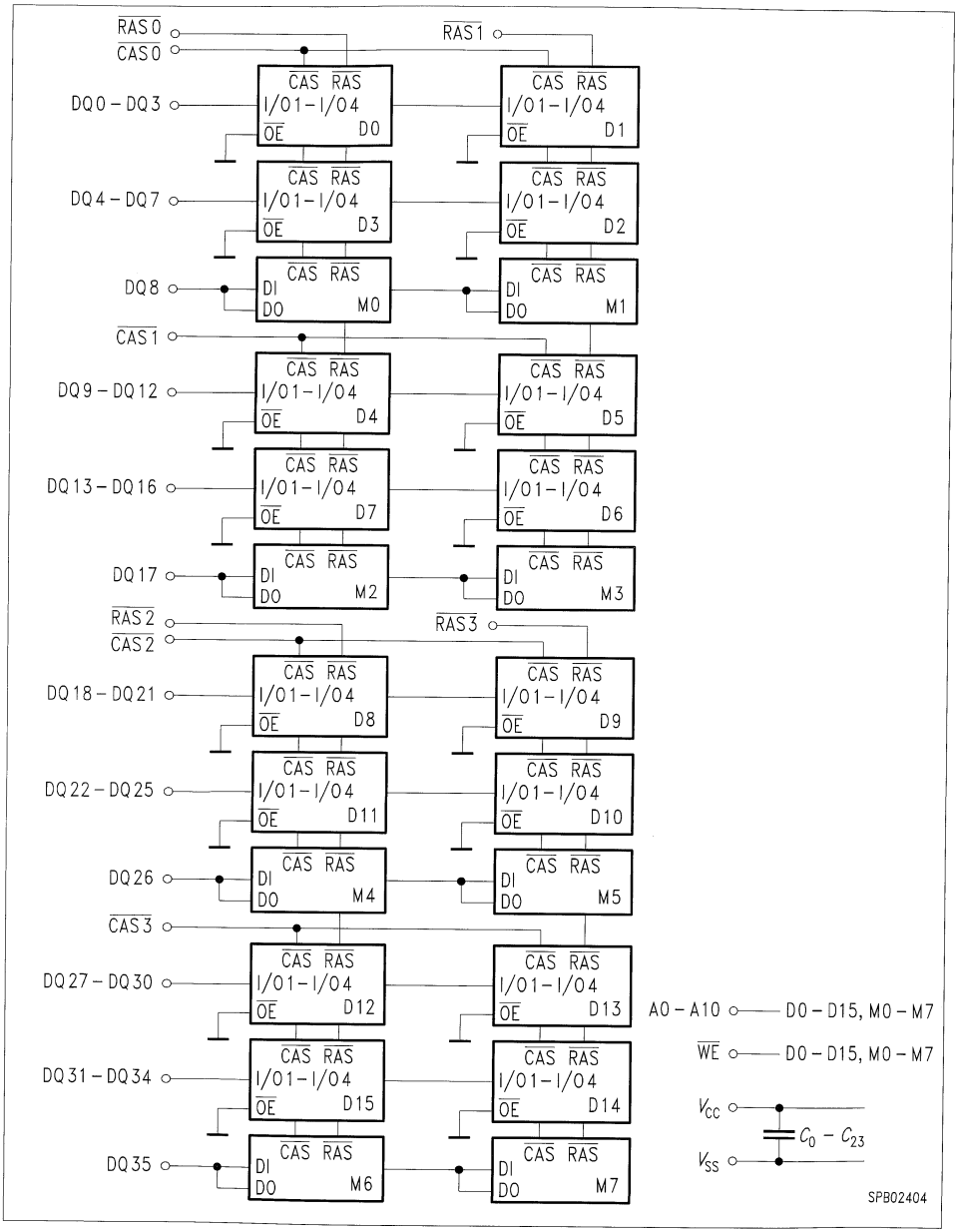
Pin No.	Function
A0-A10	Address Inputs
DQ0-DQ35	Data Input/Output
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$- $\overline{RAS3}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
PD	Presence Detect Pin
N.C.	No Connection

Presence Detect Pins

	-60	-70
PD0	N.C.	N.C.
PD1	V_{SS}	V_{SS}
PD2	N.C.	V_{SS}
PD3	N.C.	N.C.

Pin Configuration
(top view)





Block Diagram

Absolute Maximum Ratings

Operation temperature range ..... 0 to + 70 °C
Storage temperature range ..... – 55 to 125 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 0.5 V to min (V_{CC} + 0.5, 7.0) V
Power supply voltage ..... – 1 to + 7 V
Power dissipation ..... 9.24 W
Data out current (short circuit) ..... 50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics[1)]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	V_{CC} + 0.5	V	
Input low voltage	V_{IL}	– 0.5	0.8	V	
Output high voltage (I_{OUT} = – 5 mA)	V_{OH}	2.4	–	V	
Output low voltage (I_{OUT} = 4.2 mA)	V_{OL}	–	0.4	V	
Input leakage current (0 V < V_{IN} < 6.5 V, all other pins = 0 V)	$I_{I(L)}$	– 20	20	µA	
Output leakage current (DO is disabled, 0 V < V_{OUT} < 5.5 V)	$I_{O(L)}$	– 20	20	µA	
Average V_{CC} supply current ($\overline{RAS}$, $\overline{CAS}$, address cycling, t_{RC} = t_{RC} min) -60 version -70 version	I_{CC1}	 – –	 1320 1200	 mA mA	2), 3)
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	48	mA	
Average V_{CC} supply current during $\overline{RAS}$ only refresh cycles ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min) -60 version -70 version	I_{CC3}	 – –	 1320 1200	 mA mA	2)

DC Characteristics[1] (cont'd)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current during fast page mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling, t_{PC} = t_{PC} min)	I_{CC4}				
-60 version		–	920	mA	[2],
-70 version		–	840	mA	[3]
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	–	24	mA	
Average V_{CC} supply current during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode ($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min)	I_{CC6}				
-60 version		–	1320	mA	[2]
-70 version		–	1200	mA	

Capacitance

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A10,$\overline{WE}$)	C_{I1}	–	180	pF
Input capacitance ($\overline{RAS0}$ - $\overline{RAS2}$)	C_{I2}	–	50	pF
Input capacitance ($\overline{CAS0}$ - $\overline{CAS3}$)	C_{I3}	–	40	pF
I/O capacitance (DQ0-DQ35)	C_{IO}	–	25	pF

AC Characteristics [4] [5]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values				Unit
		HYM 368020S/GS-60		HYM 368020S/GS-70		
		min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	110	–	130	–	ns
Fast page mode cycle time	t_{PC}	40	–	45	–	ns
Access time from $\overline{RAS}$ [6] [11] [12]	t_{RAC}	–	60	–	70	ns
Access time from $\overline{CAS}$ [6] [11]	t_{CAC}	–	15	–	20	ns
Access time from column address [6] [12]	t_{AA}	–	30	–	35	ns
Access time from $\overline{CAS}$ precharge [6]	t_{CPA}	–	35	–	40	ns
$\overline{CAS}$ to output in low-Z [6]	t_{CLZ}	0	–	0	–	ns
Output buffer turn-off delay [7]	t_{OFF}	0	20	0	20	ns
Transition time (rise and fall) [5]	t_T	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	40	–	50	–	ns
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	ns
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	60	200000	70	200000	ns
$\overline{CAS}$ precharge to $\overline{RAS}$ delay	t_{RHCP}	35	–	40	–	ns
$\overline{RAS}$ hold time	t_{RSH}	15	–	20	–	ns
$\overline{CAS}$ hold time	t_{CSH}	60	–	70	–	ns
$\overline{CAS}$ pulse width	t_{CAS}	15	10000	20	10000	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time [11]	t_{RCD}	20	45	20	50	ns
$\overline{RAS}$ to column address delay time [12]	t_{RAD}	15	30	15	35	ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	ns
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	ns
Row address hold time	t_{RAH}	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	ns
Column address hold time	t_{CAH}	15	–	15	–	ns

AC Characteristics[4) 5)] (cont'd)
T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values				Unit
		HYM 368020S/GS-60		HYM 368020S/GS-70		
		min.	max.	min.	max.	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	–	35	–	ns
Read command setup time	t_{RCS}	0	–	0	–	ns
Read command hold time [8)]	t_{RCH}	0	–	0	–	ns
Read command hold time ref. to $\overline{RAS}$ [8)]	t_{RRH}	0	–	0	–	ns
Write command hold time	t_{WCH}	10	–	15	–	ns
Write command pulse width	t_{WP}	10	–	15	–	ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	–	20	–	ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	–	20	–	ns
Data setup time [9)]	t_{DS}	0	–	0	–	ns
Data hold time [9)]	t_{DH}	15	–	15	–	ns
Refresh period	t_{REF}	–	32	–	32	ms
Write command setup time [10)]	t_{WCS}	0	–	0	–	ns
$\overline{CAS}$ setup time [13)]	t_{CSR}	10	–	10	–	ns
$\overline{CAS}$ hold time [13)]	t_{CHR}	10	–	10	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5	–	5	–	ns
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	ns
Write to $\overline{RAS}$ precharge time [13)]	t_{WRP}	10	–	10	–	ns
Write hold time ref. to $\overline{RAS}$ [13)]	t_{WRH}	10	–	10	–	ns

Notes

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading.
Specified values are measured with the output open.

4) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles out of which at least one cycle has to be a refresh cycle before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

5) V_{IH} (max) and V_{IL} (max) are reference levels for measuring timing of input signals.
Transition times are also measured between V_{IH} and V_{IL}.

6) Measured with a load equivalent of 2 TTL loads and 100 pF.

7) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.

8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9) These parameters are referenced to the $\overline{CAS}$ leading edge.

10) t_{WCS} is not a restrictive operating parameter. This is included in the data sheet as electrical characteristic only. If $t_{WCS} > t_{WCS}$ (min), the cycle is an early write cycle and data out pin will remain open (high impedance).

11) Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAS}.

12) Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.

13) For $\overline{CAS}$-before-$\overline{RAS}$ cycles only.

1M × 64-Bit Dynamic RAM Module

HYM 641010GS-60/-70
HYM 641020GS-60/-70

Preliminary Information

- 1 048 576 words by 64-bit organization
- Fast access and cycle time
  60 ns access time
  110 ns cycle time (-60 version)
  70 ns access time
  130 ns cycle time (-70 version)
- Fast page mode capability with
  40 ns cycle time (-60 version)
  45 ns cycle time (-70 version)
- Single + 5 V (± 10 %) supply
- Low power dissipation
  max. 9680 mW active (-60 version)
  max. 8800 mW active (-70 version)
  CMOS – 451 mW standby
  TTL – 550 mW standby
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$-only-refresh
- 16 decoupling capacitors mounted on substrate
- All inputs, outputs and clock fully TTL compatible
- 4 Byte interleave enabled, Dual Address inputs (A0/B0)
- Buffered inputs except $\overline{\text{RAS}}$ and DQ
- 168 pin, dual read-out, Single in-Line Memory Module
- Utilizes sixteen 1M × 4 - DRAMs (HYB 514400BJ/BT) and four BiCMOS 8-bit buffers/line drivers 74ABT244
- Two version:
  HYM 641010S with SOJ-components (8.89 mm module thickness
  HYM 641020GS with TSOPII-components (4.06 mm module thickness)
- 1024 refresh cycles / 16 ms
- Gold contact pad
- double sided module with 25.35 mm (1000 mil) height

Ordering Information

Type	Ordering Code	Package	Descriptions
HYM 641020GS-60	Q67100 - Q2003	L-DIM-168-1	60 ns DRAM module
HYM 641020GS-70	on request	L-DIM-168-1	70 ns DRAM module
HYM 641010GS-60	Q67100 - Q2002	L-DIM-168-1	60 ns DRAM module
HYM 641010GS-70	on request	L-DIM-168-1	70 ns DRAM module

The HYM 641010/20GS-60/-70 is a 8 M Byte DRAM module organized as 1 048 576 words by 64-bit in a 168-pin, dual read-out, single-in-line package comprising sixteen HYB 514400BJ/BT 1M × 4 DRAMs in 300 mil wide SOJ or TSOPII - packages mounted together with sixteen 0.2 µF ceramic decoupling capacitors on a PC board. All inputs except $\overline{RAS}$ and DQ are buffered by using four BiCMOS 8-bit buffers/line drivers.

Each HYB 514400BJ/BT is described in the data sheet and is fully electrically tested and processed according to Siemens standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

The density and speed of the module can be detected by the use of presence detect pins.

Pin Definitions and Functions

Pin No	Function
A0-A9,B0	Address Input
DQ0 - DQ63	Data Input/Output
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Column Address Strobe
$\overline{WE0}$, $\overline{WE2}$	Read / Write Input
$\overline{OE0}$, $\overline{OE2}$	Output Enable
V_{cc}	Power (+ 5 V)
V_{ss}	Ground
PD1 - PD8	Presence Detect Pins
PDE	Presence Detect Enable
ID0 , ID1	ID indentification bit
N.C.	No Connection

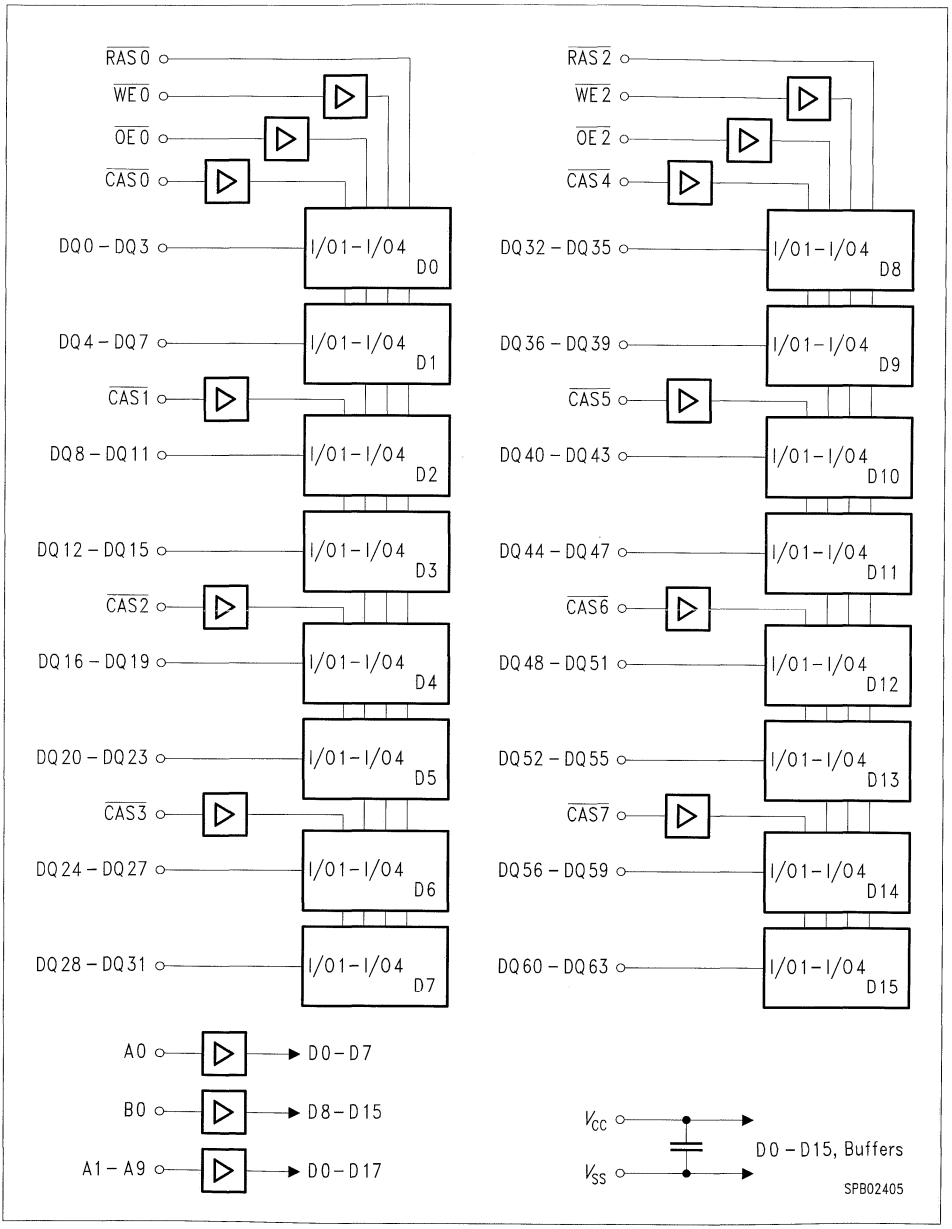
Presence-Detect and ID-pin Thruth Table:

Module	ID0	ID1	PD1	PD2	PD3	PD4	PD5	PD6	PD7	PD8
HYM 641010/20GS-60	V_{ss}	V_{ss}	0	0	1	0	0	1	1	1
HYM 641010/20GS-70	V_{ss}	V_{ss}	0	0	1	0	0	0	1	1

Note: 1= high level (driver output), 0 = low level (driver output) for $\overline{PDE}$ active (ground) . For $\overline{PDE}$ at a high level all PD terminals are in tri-state.

Pin Configuration

PIN #	Symbol	PIN #	Symbol	PIN #	Symbol	PIN #	Symbol
1	V_{ss}	43	V_{ss}	85	V_{ss}	127	V_{ss}
2	DQ0	44	OE2	86	DQ32	128	NC
3	DQ1	45	RAS2	87	DQ33	129	NC
4	DQ2	46	CAS4	88	DQ34	130	CAS5
5	DQ3	47	CAS6	89	DQ35	131	CAS7
6	V_{CC}	48	WE2	90	V_{CC}	132	PDE
7	DQ4	49	V_{CC}	91	DQ36	133	V_{CC}
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	DQ16	94	DQ39	136	DQ48
11	NC	53	DQ17	95	NC	137	DQ49
12	V_{ss}	54	V_{ss}	96	V_{ss}	138	V_{ss}
13	DQ8	55	DQ18	97	DQ40	139	DQ50
14	DQ9	56	DQ19	98	DQ41	140	DQ51
15	DQ10	57	DQ20	99	DQ42	141	DQ52
16	DQ11	58	DQ21	100	DQ43	142	DQ53
17	DQ12	59	V_{CC}	101	DQ44	143	V_{CC}
18	V_{CC}	60	DQ22	102	V_{CC}	144	DQ54
19	DQ13	61	NC	103	DQ45	145	NC
20	DQ14	62	NC	104	DQ46	146	NC
21	DQ15	63	NC	105	DQ47	147	NC
22	NC	64	NC	106	NC	148	NC
23	V_{ss}	65	DQ23	107	V_{ss}	149	DQ55
24	NC	66	NC	108	NC	150	NC
25	NC	67	DQ24	109	NC	151	DQ55
26	V_{CC}	68	V_{ss}	110	V_{CC}	152	V_{ss}
27	WE0	69	DQ25	111	NC	153	DQ57
28	CAS0	70	DQ26	112	CAS1	154	DQ58
29	CAS2	71	DQ27	113	CAS3	155	DQ59
30	RAS0	72	DQ28	114	NC	156	DQ60
31	OE0	73	V_{CC}	115	NC	157	V_{CC}
32	V_{ss}	74	DQ29	116	V_{ss}	158	DQ61
33	A0	75	DQ30	117	A1	159	DQ62
34	A2	76	DQ31	118	A3	160	DQ63
35	A4	77	NC	119	A5	161	NC
36	A6	78	V_{ss}	120	A7	162	V_{ss}
37	A8	79	PD1	121	A9	163	PD2
38	NC	80	PD3	122	NC	164	PD4
39	NC	81	PD5	123	NC	165	PD6
40	V_{CC}	82	PD7	124	V_{CC}	166	PD8
41	NC	83	ID0	125	NC	167	ID1
42	NC	84	V_{CC}	126	B0	168	V_{CC}



Block Diagram

Absolute Maximum Ratings

Operating temperature range ..... 0 to + 70 °C
Storage temperature range ..... – 55 to + 125 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 1 to + 7 V
Power supply voltage ..... – 1 to + 7 V
Power dissipation ..... 12,32 W
Data out current (short circuit) ..... 50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics [1)]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	5.5	V	–
Input low voltage	V_{IL}	– 1.0	0.8	V	–
Output high voltage (I_{OUT} = – 5 mA)	V_{OH}	2.4	–	V	–
Output low voltage (I_{OUT} = 4.2 mA)	V_{OL}	–	0.4	V	–
Input leakage current (0 V < V_{IN} < 6.5 V, all other pins = 0 V)	$I_{I(L)}$	– 10	10	µA	–
Output leakage current (DO is disabled, 0 V < V_{OUT} < 5.5 V)	$I_{O(L)}$	– 10	10	µA	–
Average V_{CC} supply current: HYM 641010/20GS-60 HYM 641010/20GS-70 ($\overline{RAS}$, $\overline{CAS}$, address cycling, t_{RC} = t_{RC} min.)	I_{CC1}	 – –	 1760 1600	 mA mA	2), 3)
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	50	mA	–
Average V_{CC} supply current during $\overline{RAS}$ only refresh cycles: HYM 641010/20GS-60 HYM 641010/20GS-70 ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)	I_{CC3}	 – –	 1760 1600	 mA mA	2)

DC Characteristics (cont'd) [1]

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current during fast page mode:	I_{CC4}				2), 3)
HYM 641010/20GS-60		–	1120	mA	
HYM 641010/20GS-70		–	1120	mA	
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling t_{PC} = t_{PC} min.)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	–	30	mA	–
Average V_{CC} supply current during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode:	I_{CC6}				1)
HYM 641010/20GS-60		–	1760	mA	
HYM 641010/20GS-70		–	1600	mA	
($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min.)					

Capacitance

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A9,B0)	C_{I1}	–	20	pF
Input capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	C_{I2}	–	80	pF
Input capacitance ($\overline{CAS0}$-$\overline{CAS7}$)	C_{I3}	–	20	pF
Input capacitance ($\overline{WE0}$,$\overline{WE2}$,$\overline{OE0}$,$\overline{OE2}$)	C_{I4}	–	20	pF
I/O capacitance (DQ0-DQ63)	C_{IO1}	–	20	pF

AC Characteristics [4) 5)14)]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values				Unit
		HYM 641010/20GS-60		HYM 641010/20GS-70		
		min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	110	–	130	–	ns
Fast page mode cycle time	t_{PC}	40	–	45	–	ns
Access time from $\overline{RAS}$ [6) 11) 12)]	t_{RAC}	–	60	–	70	ns
Access time from $\overline{CAS}$ [6) 11)]	t_{CAC}	–	15	–	20	ns
Access time from column address [6) 12)]	t_{AA}	–	30	–	35	ns
Access time from $\overline{CAS}$ precharge [6)]	t_{CPA}	–	35	–	40	ns
$\overline{CAS}$ to output in low-Z [6)]	t_{CLZ}	0	–	0	–	ns
Output buffer turn-off delay [7)]	t_{OFF}	0	20	0	20	ns
Transition time (rise and fall) [5)]	t_T	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	40	–	50	–	ns
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	ns
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	60	200000	70	200000	ns
$\overline{CAS}$ precharge to $\overline{RAS}$ delay	t_{RHCP}	35	–	40	–	ns
$\overline{RAS}$ hold time	t_{RSH}	15	–	20	–	ns
$\overline{CAS}$ hold time	t_{CSH}	60	–	70	–	ns
$\overline{CAS}$ pulse width	t_{CAS}	15	10000	20	10000	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time [11)]	t_{RCD}	20	45	20	50	ns
$\overline{RAS}$ to column address delay time [12)]	t_{RAD}	15	30	15	35	ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	ns
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	ns
Row address hold time	t_{RAH}	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	ns
Column address hold time	t_{CAH}	15	–	15	–	ns

AC Characteristics (cont'd) [4) 5)14)]
T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values				Unit
		HYM 641010/20GS-60		HYM 641010/20GS-70		
		min.	max.	min.	max.	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	–	35	–	ns
Read command setup time	t_{RCS}	0	–	0	–	ns
Read command hold time [8)]	t_{RCH}	0	–	0	–	ns
Read command hold time ref. to $\overline{RAS}$ [8)]	t_{RRH}	0	–	0	–	ns
Write command hold time	t_{WCH}	10	–	15	–	ns
Write command pulse width	t_{WP}	10	–	15	–	ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	–	20	–	ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	–	20	–	ns
Data setup time [9)]	t_{DS}	0	–	0	–	ns
Data hold time [9)]	t_{DH}	15	–	15	–	ns
Refresh period	t_{REF}	–	16	–	16	ms
Write command setup time [10)]	t_{WCS}	0	–	0	–	ns
$\overline{CAS}$ setup time [13)]	t_{CSR}	5	–	5	–	ns
$\overline{CAS}$ hold time [13)]	t_{CHR}	15	–	15	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	0	–	0	–	ns
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	ns
Write to $\overline{RAS}$ precharge time [13)]	t_{WRP}	10	–	10	–	ns
Write to time ref. to $\overline{RAS}$ [13)]	t_{WRH}	10	–	10	–	ns

Notes

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.

4) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles out of which at least one cycle has to be a refresh cycle before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

5) V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.

6) Measured with a load equivalant of 2 TTL loads and 100 pF.

7) t_{OFF} (max.) defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.

8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9) These parameters are referenced to the $\overline{CAS}$ leading edge.

10) t_{WCS} is not a restrictive operating parameter. This is included in the data sheet as electrical characteristic only. If $t_{WCS} > t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance).

11) Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

12) Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{HAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

13) For $\overline{CAS}$-before-$\overline{RAS}$ cycles only.

14) A $\pm$ 2 ns timing skew has to be added to all values due to the use of the buffers / line drivers

1M × 72-Bit Dynamic RAM Module (ECC - Module)

HYM 721000GS-60/-70

Preliminary Information

- 1 048 576 words by 72-bit ECC - mode organization
- Fast access and cycle time
  60 ns access time
  110 ns cycle time (-60 version)
  70 ns access time
  130 ns cycle time (-70 version)
- Fast page mode capability with
  40 ns cycle time (-60 version)
  45 ns cycle time (-70 version)
- Single + 5 V (± 10 %) supply
- Low power dissipation
  max. 10890 mW active (-60 version)
  max. 9900 mW active (-70 version)
  CMOS – 451 mW standby
  TTL – 550 mW standby
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$-only-refresh
- 18 decoupling capacitors mounted on substrate
- All inputs, outputs and clock fully TTL compatible
- 4 Byte interleave enabled, Dual Address inputs (A0/B0)
- Buffered inputs excepts $\overline{\text{RAS}}$ and DQ
- 168 pin, dual read-out, Single in-Line Memory Module
- Utilizes eighteen 1M × 4 - DRAMs in TSOPII-packages and four BiCMOS 8-bit buffers/line drivers 74ABT244
- 4.06 mm module thickness
- 1024 refresh cycles / 16 ms
- Gold contact pad
- double sided module with 25.35 mm (1000 mil) height

Ordering Information

Type	Ordering Code	Package	Descriptions
HYM 721000GS-60	Q67100-Q2004	L-DIM-168-2	DRAM module (access time 60 ns)
HYM 721000GS-70	on request	L-DIM-168-2	DRAM module (access time 70 ns)

The HYM 721000GS-60/-70 is a 8 M Byte DRAM module organized as 1 048 576 words by 72-bit in a 168-pin, dual read-out, single-in-line package comprising eighteen HYB 514400BT 1M × 4 DRAMs in 300 mil wide TSOPII - packages mounted together with eighteen 0.2 µF ceramic decoupling capacitors on a PC board. All inputs except $\overline{RAS}$ and DQ are buffered by using four BiCMOS 8-bit buffers/line drivers.

Each HYB 514400BT is described in the data sheet and is fully electrically tested and processed according to Siemens standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

The density and speed of the module can be detected by the use of presence detect pins.

Pin Definitions and Functions

Pin No.	Function
A0-A9,B0	Address Input
DQ0 - DQ71	Data Input/Output
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS2}$	Column Address Strobe
$\overline{WE0}$, $\overline{WE2}$	Read / Write Input
$\overline{OE0}$, $\overline{OE2}$	Output Enable
V_{cc}	Power (+ 5 V)
V_{ss}	Ground
PD1 - PD8	Presence Detect Pins
$\overline{PDE}$	Presence Detect Enable
ID0 , ID1	ID indentification bit
N.C.	No Connection

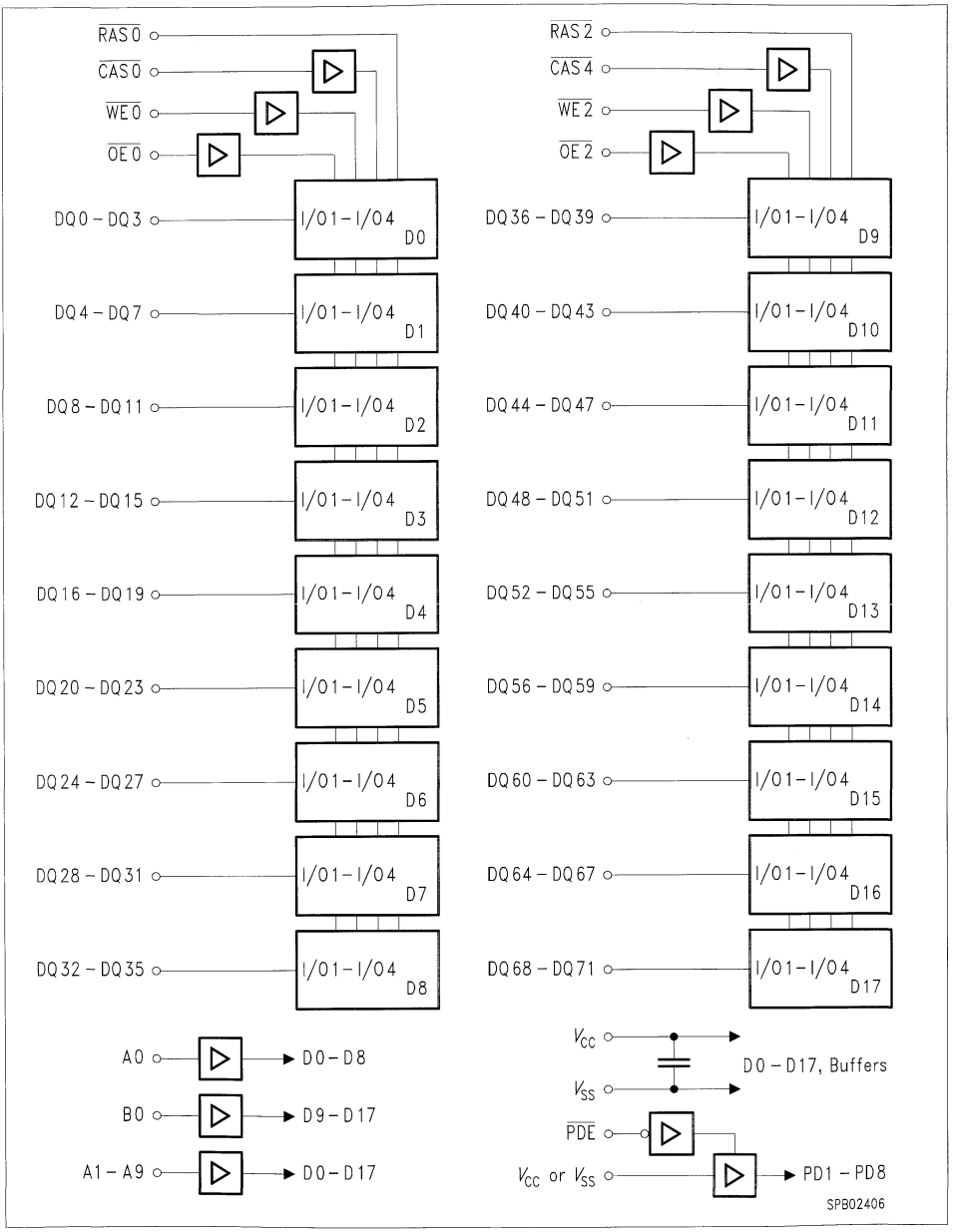
Presence-Detect and ID-pin Thruth Table:

Module	ID0	ID1	PD1	PD2	PD3	PD4	PD5	PD6	PD7	PD8
HYM 721000GS-60	V_{ss}	V_{ss}	0	0	1	0	0	1	1	0
HYM 721000GS-70	V_{ss}	V_{ss}	0	0	1	0	0	0	1	0

Note: 1 = High Level (Driver Output) , 0 = Low Level (Driver Output) for $\overline{PDE}$ active (ground) . For $\overline{PDE}$ at a high level all PD terminal are in tri-state.

Pin Configuration

PIN #	Symbol	PIN #	Symbol		PIN #	Symbol	PIN #	Symbol
1	V_{SS}	43	V_{SS}		85	V_{SS}	127	V_{SS}
2	DQ0	44	OE2		86	DQ36	128	NC
3	DQ1	45	RAS2		87	DQ37	129	NC
4	DQ2	46	CAS4		88	DQ38	130	NC
5	DQ3	47	NC		89	DQ39	131	NC
6	V_{CC}	48	WE2		90	V_{CC}	132	PDE
7	DQ4	49	V_{CC}		91	DQ40	133	V_{CC}
8	DQ5	50	NC		92	DQ41	134	NC
9	DQ6	51	NC		93	DQ42	135	NC
10	DQ7	52	DQ18		94	DQ43	136	DQ54
11	DQ8	53	DQ19		95	DQ44	137	DQ55
12	V_{SS}	54	V_{SS}		96	V_{SS}	138	V_{SS}
13	DQ9	55	DQ20		97	DQ45	139	DQ56
14	DQ10	56	DQ21		98	DQ46	140	DQ57
15	DQ11	57	DQ22		99	DQ47	141	DQ58
16	DQ12	58	DQ23		100	DQ48	142	DQ59
17	DQ13	59	V_{CC}		101	DQ49	143	V_{CC}
18	V_{CC}	60	DQ24		102	V_{CC}	144	DQ60
19	DQ14	61	NC		103	DQ50	145	NC
20	DQ15	62	NC		104	DQ51	146	NC
21	DQ16	63	NC		105	DQ52	147	NC
22	DQ17	64	NC		106	DQ53	148	NC
23	V_{SS}	65	DQ25		107	V_{SS}	149	DQ61
24	NC	66	DQ26		108	NC	150	DQ62
25	NC	67	DQ27		109	NC	151	DQ63
26	V_{CC}	68	V_{SS}		110	V_{CC}	152	V_{SS}
27	WE0	69	DQ28		111	NC	153	DQ64
28	CAS0	70	DQ29		112	NC	154	DQ65
29	NC	71	DQ30		113	NC	155	DQ66
30	RAS0	72	DQ31		114	NC	156	DQ67
31	OE0	73	V_{CC}		115	NC	157	V_{CC}
32	V_{SS}	74	DQ32		116	V_{SS}	158	DQ68
33	A0	75	DQ33		117	A1	159	DQ69
34	A2	76	DQ34		118	A3	160	DQ70
35	A4	77	DQ35		119	A5	161	DQ71
36	A6	78	V_{SS}		120	A7	162	V_{SS}
37	A8	79	PD1		121	A9	163	PD2
38	NC	80	PD3		122	NC	164	PD4
39	NC	81	PD5		123	NC	165	PD6
40	V_{CC}	82	PD7		124	V_{CC}	166	PD8
41	NC	83	ID0 (V_{SS})		125	NC	167	ID1 (V_{SS})
42	NC	84	V_{CC}		126	B0	168	V_{CC}



Block Diagram

Absolute Maximum Ratings

Operating temperature range ..... 0 to + 70 °C
Storage temperature range ..... – 55 to + 125 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 1 to + 7 V
Power supply voltage ..... – 1 to + 7 V
Power dissipation ..... 13.86 W
Data out current (short circuit) ..... 50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics [1]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	5.5	V	–
Input low voltage	V_{IL}	– 1.0	0.8	V	–
Output high voltage (I_{OUT} = – 5 mA)	V_{OH}	2.4	–	V	–
Output low voltage (I_{OUT} = 4.2 mA)	V_{OL}	–	0.4	V	–
Input leakage current (0 V < V_{IN} < 6.5 V, all other pins = 0 V)	$I_{I(L)}$	– 10	10	µA	–
Output leakage current (DO is disabled, 0 V < V_{OUT} < 5.5 V)	$I_{O(L)}$	– 10	10	µA	–
Average V_{CC} supply current:	I_{CC1}				
HYM 721000GS-60		–	1980	mA	2), 3)
HYM 721000GS-70		–	1800	mA	
($\overline{RAS}$, $\overline{CAS}$, address cycling, t_{RC} = t_{RC} min.)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	50	mA	–
Average V_{CC} supply current during $\overline{RAS}$ only refresh cycles:	I_{CC3}				2)
HYM 721000GS-60		–	1980	mA	
HYM 721000GS-70		–	1800	mA	
($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)					

DC Characteristics (cont'd) [1]

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current during fast page mode:	I_{CC4}				[2], [3]
HYM 721000GS-60		–	1260	mA	
HYM 721000GS-70		–	1260	mA	
		–			
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling t_{PC} = t_{PC} min.)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	–	30	mA	–
Average V_{CC} supply current during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode:	I_{CC6}				[1]
HYM 721000GS-60		–	1980	mA	
HYM 721000GS-70		–	1800	mA	
($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min.)					

Capacitance

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A9,B0)	C_{I1}	–	20	pF
Input capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	C_{I2}	–	80	pF
Input capacitance ($\overline{CAS0}$-$\overline{CAS7}$)	C_{I3}	–	20	pF
Input capacitance ($\overline{WE0}$,$\overline{WE2}$,$\overline{OE0}$,$\overline{OE2}$)	C_{I4}	–	20	pF
I/O capacitance (DQ0-DQ71)	C_{IO1}	–	20	pF

AC Characteristics [4) 5)14)]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values				Unit
		HYM 721000GS-60		HYM 721000GS-70		
		min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	110	–	130	–	ns
Fast page mode cycle time	t_{PC}	40	–	45	–	ns
Access time from $\overline{RAS}$ [6) 11) 12)]	t_{RAC}	–	60	–	70	ns
Access time from $\overline{CAS}$ [6) 11)]	t_{CAC}	–	15	–	20	ns
Access time from column address [6) 12)]	t_{AA}	–	30	–	35	ns
Access time from $\overline{CAS}$ precharge [6)]	t_{CPA}	–	35	–	40	ns
$\overline{CAS}$ to output in low-Z [6)]	t_{CLZ}	0	–	0	–	ns
Output buffer turn-off delay [7)]	t_{OFF}	0	20	0	20	ns
Transition time (rise and fall) [5)]	t_T	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	40	–	50	–	ns
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	ns
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	60	200000	70	200000	ns
$\overline{CAS}$ precharge to $\overline{RAS}$ delay	t_{RHCP}	35	–	40	–	ns
$\overline{RAS}$ hold time	t_{RSH}	15	–	20	–	ns
$\overline{CAS}$ hold time	t_{CSH}	60	–	70	–	ns
$\overline{CAS}$ pulse width	t_{CAS}	15	10000	20	10000	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time [11)]	t_{RCD}	20	45	20	50	ns
$\overline{RAS}$ to column address delay time [12)]	t_{RAD}	15	30	15	35	ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	ns
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	ns
Row address hold time	t_{RAH}	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	ns
Column address hold time	t_{CAH}	15	–	15	–	ns

AC Characteristics (cont'd) [4) 5)14)]
T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values				Unit
		HYM 721000GS-60		HYM 721000GS-70		
		min.	max.	min.	max.	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	–	35	–	ns
Read command setup time	t_{RCS}	0	–	0	–	ns
Read command hold time 8)	t_{RCH}	0	–	0	–	ns
Read command hold time ref. to $\overline{RAS}$ 8)	t_{RRH}	0	–	0	–	ns
Write command hold time	t_{WCH}	10	–	15	–	ns
Write command pulse width	t_{WP}	10	–	15	–	ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	–	20	–	ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	–	20	–	ns
Data setup time 9)	t_{DS}	0	–	0	–	ns
Data hold time 9)	t_{DH}	15	–	15	–	ns
Refresh period	t_{REF}	–	16	–	16	ms
Write command setup time 10)	t_{WCS}	0	–	0	–	ns
$\overline{CAS}$ setup time 13)	t_{CSR}	5	–	5	–	ns
$\overline{CAS}$ hold time 13)	t_{CHR}	15	–	15	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	0	–	0	–	ns
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	ns
Write to $\overline{RAS}$ precharge time 13)	t_{WRP}	10	–	10	–	ns
Write to time ref. to $\overline{RAS}$ 13)	t_{WRH}	10	–	10	–	ns

Notes

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.

4) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles out of which at least one cycle has to be a refresh cycle before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

5) V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.

6) Measured with a load equivalant of 2 TTL loads and 100 pF.

7) t_{OFF} (max.) defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.

8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9) These parameters are referenced to the $\overline{CAS}$ leading edge.

10) t_{WCS} is not a restrictive operating parameter. This is included in the data sheet as electrical characteristic only. If $t_{WCS} > t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance).

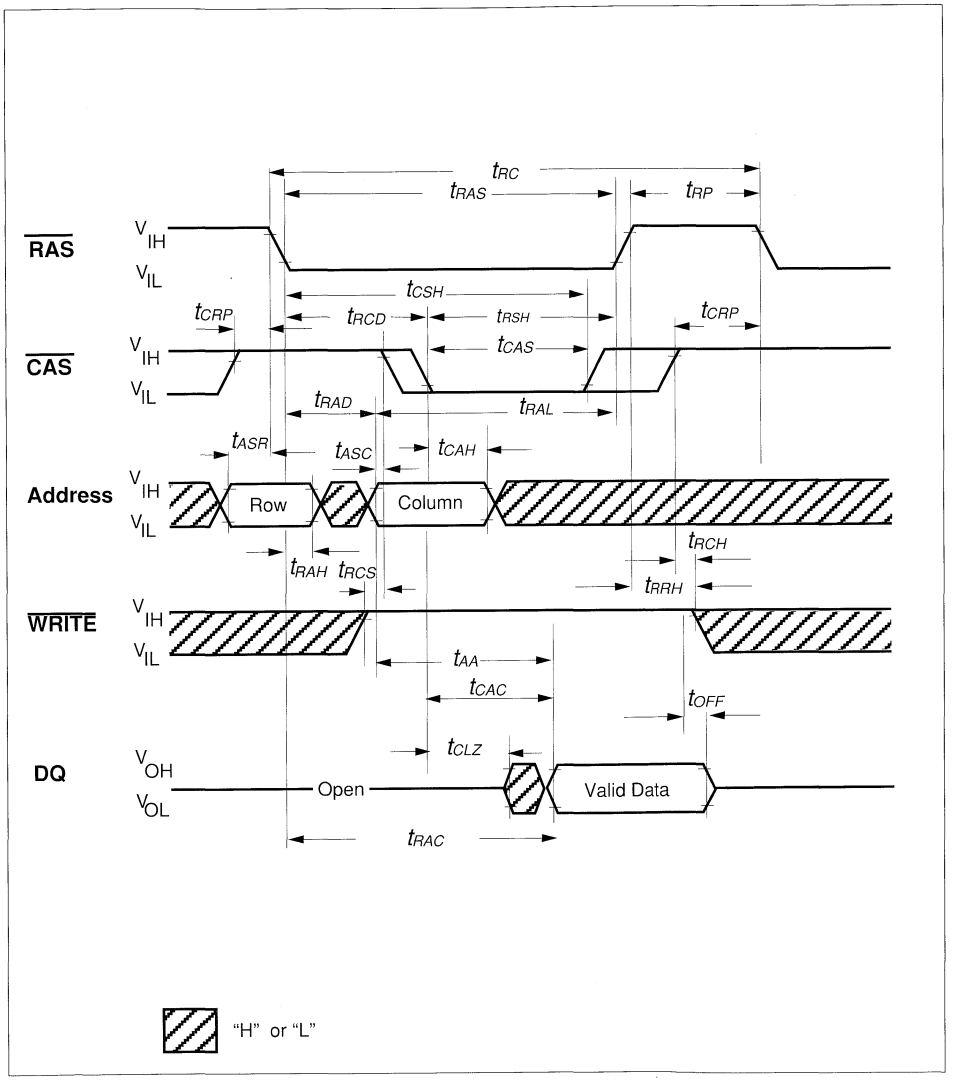
11) Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

12) Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

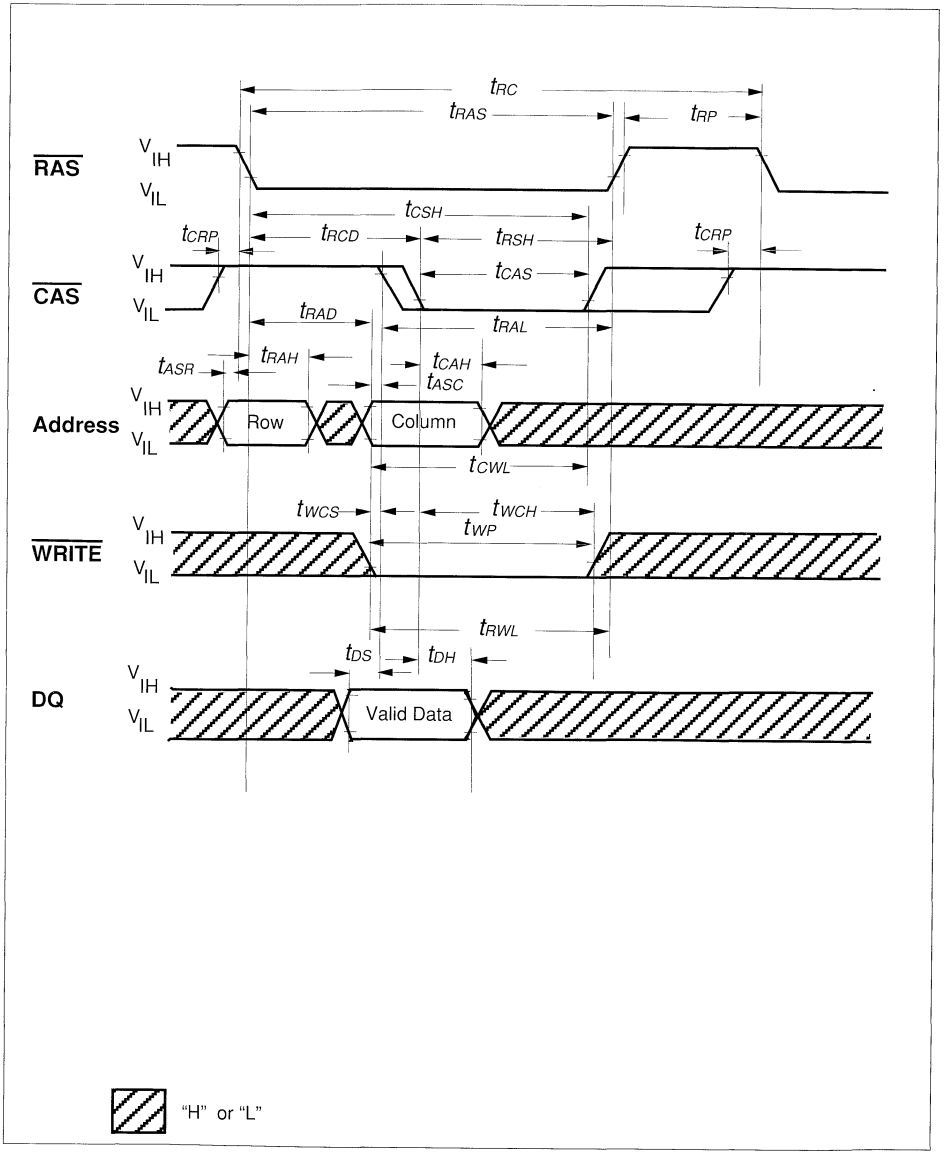
13) For $\overline{CAS}$-before-$\overline{RAS}$ cycles only.

14) A ± 2 ns timing skew has to be added to all values due to the use of the buffers / line drivers.

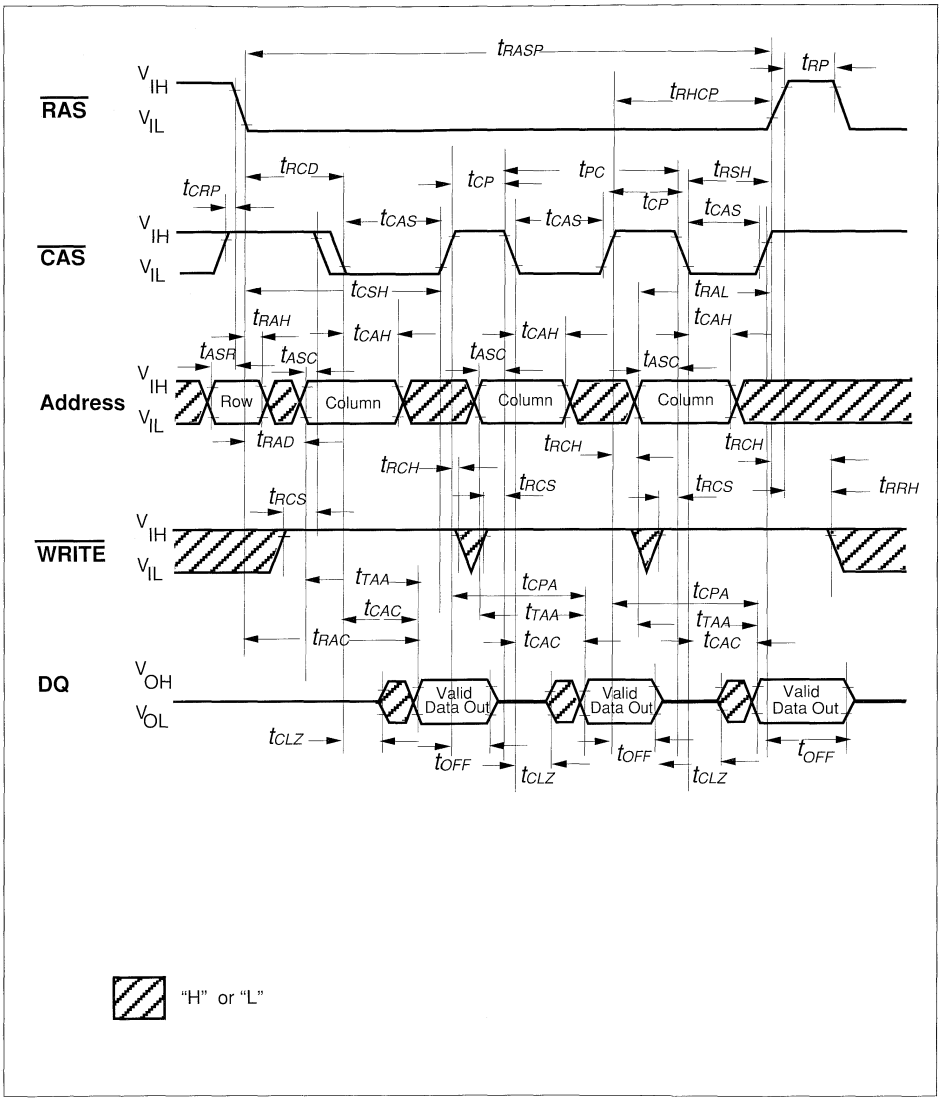
Waveforms



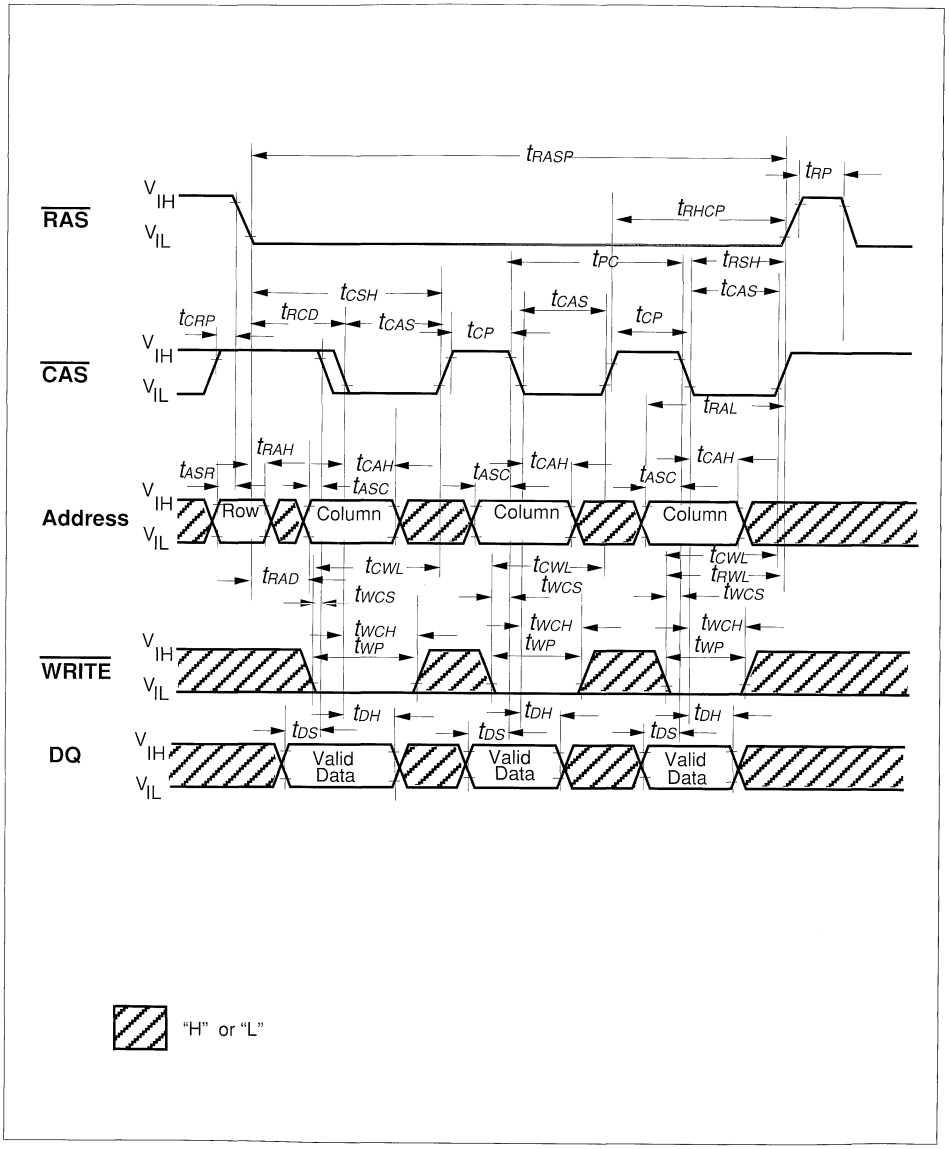
Read Cycle



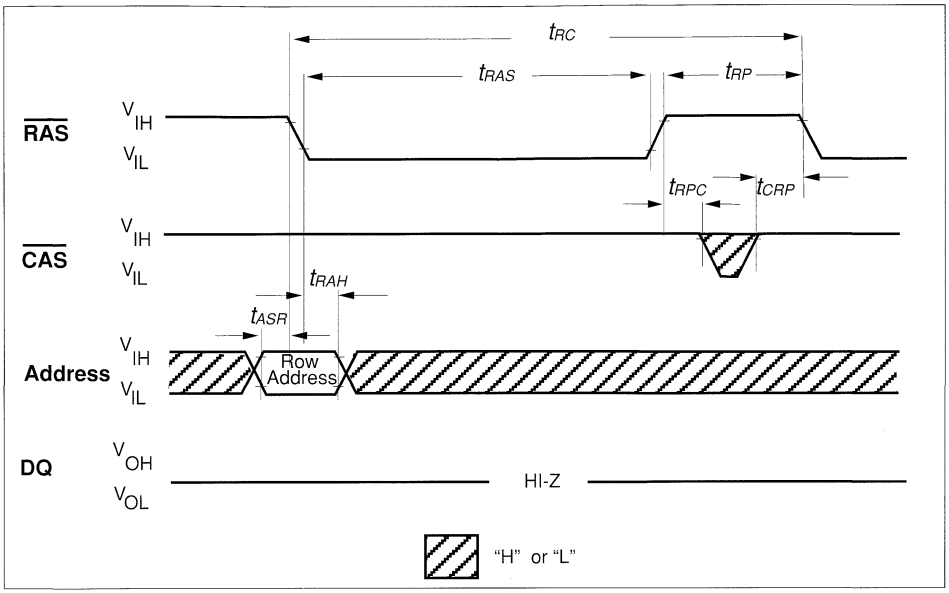
Write Cycle (early write)



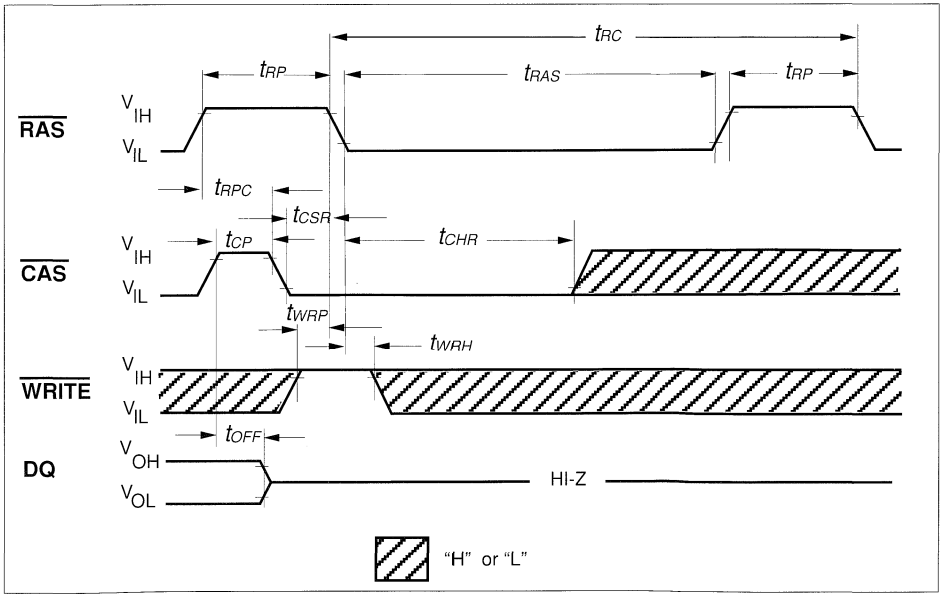
Fast Page Mode Read Cycle



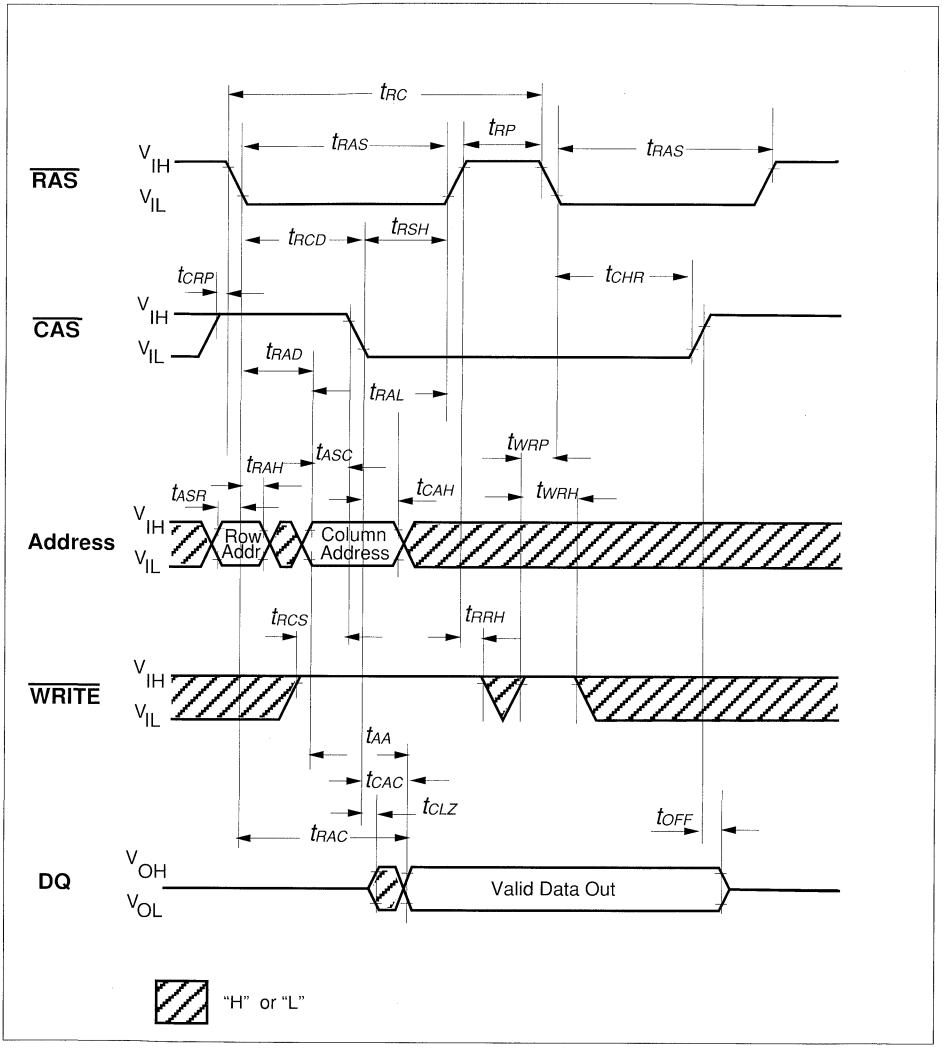
Fast Page Mode Write Cycle (early write)



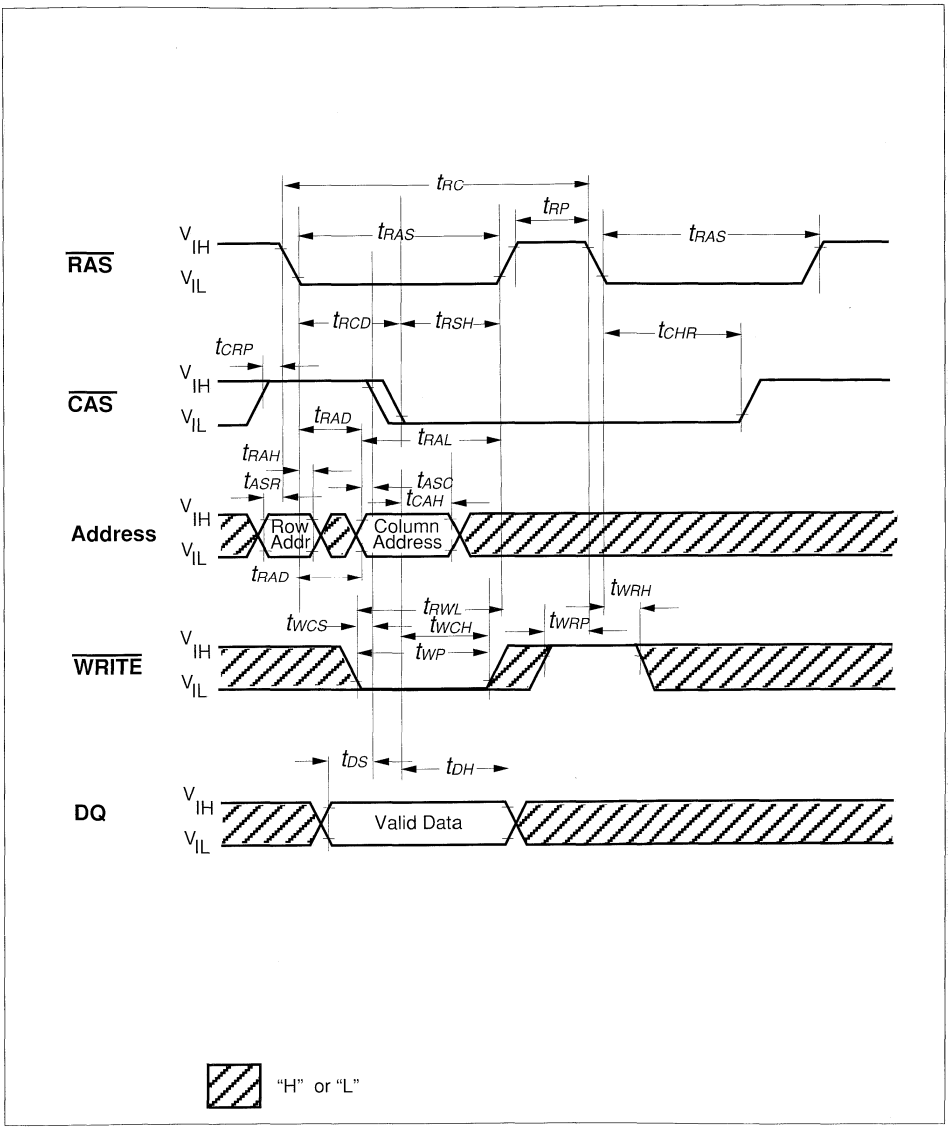
RAS-Only Refresh Cycle



CAS-Before-RAS Refresh Cycle



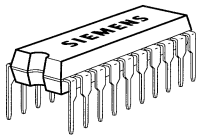
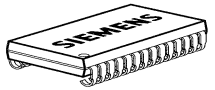
Hidden Refresh Cycle (read)



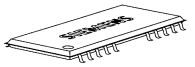
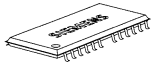
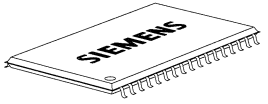
Hidden Refresh Cycle (write)

Package Outlines

Memory Components

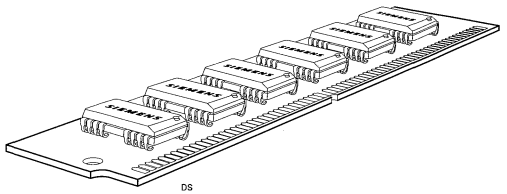
	**P-DIP-20-2** **Plastic Package** (Plastic dual in-line package)
	**P-SOJ-26/20-1 (SMD)** **Plastic Package** (Plastic small outline J-lead)
	**P-SOJ-26/20-5 (SMD)** **Plastic Package** (Plastic dual in-line package)
	**P-SOJ-28-2 (SMD)** **Plastic Package** (Plastic small outline J-lead)

	**P-SOJ-40-1 (SMD)** **Plastic Package** (Plastic small outline J-lead)
	**P-SOJ-26/24-1 (300 mil) (SMD)** **Plastic Package** (Plastic small outline J-lead)
	**P-SOJ-28-3 (SMD)** **Plastic Package**
	**P-SOJ-34-1 (SMD)** **Plastic Package**

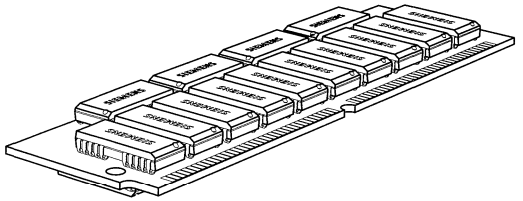
	**P-SOJ-42-1 (SMD)** **Plastic Package** (Plastic small outline J-lead)
	**P-TSOPII-26/20-1 300 mil (SMD)** **Plastic Package** (Thin small outline package)
	**P-TSOPII-26/24-1 (SMD)** **Plastic Package** (Thin small outline package)
	**P-TSOPII-34-1 (SMD)** **Plastic Package** (Thin small outline package)

P-TSOPII-54-1 (SMD)
Plastic Package
(Thin small outline package)

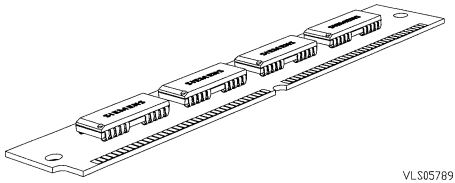
Memory Module



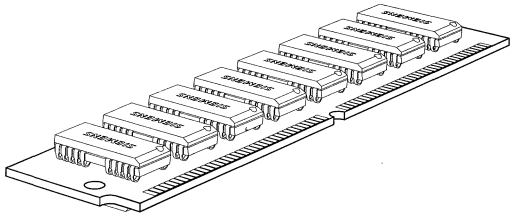
L-SIM-72-3
Module Package
(Double sided socket type)
(Single in-line memory module)



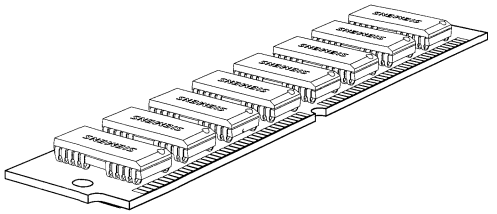
L-SIM-72-8
Module Package
(Double sided socket type)
(Single in-line memory module)



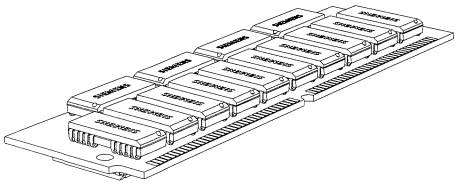
L-SIM-72-9
Module Package
(Single sided socket type)
(Single in-line memory module)



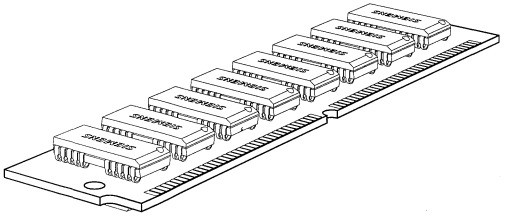
L-SIM-72-11
Module Package
(Double sided socket type)
(Single in-line memory module)



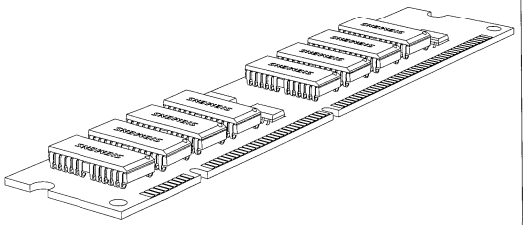
L-SIM-72-12 (Double sided socket type)
Module Package
(Single in-line memory module)



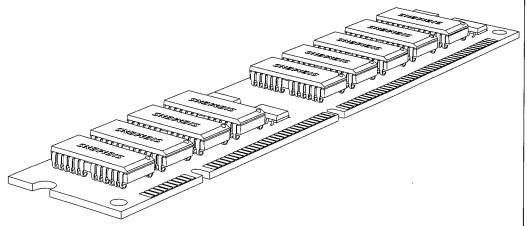
L-SIM-72-14 (Double sided socket type)
Module Package
(Single in-line memory module)



L-SIM-72-15 (Double sided socket type)
Module Package
(Single in-line memory module)

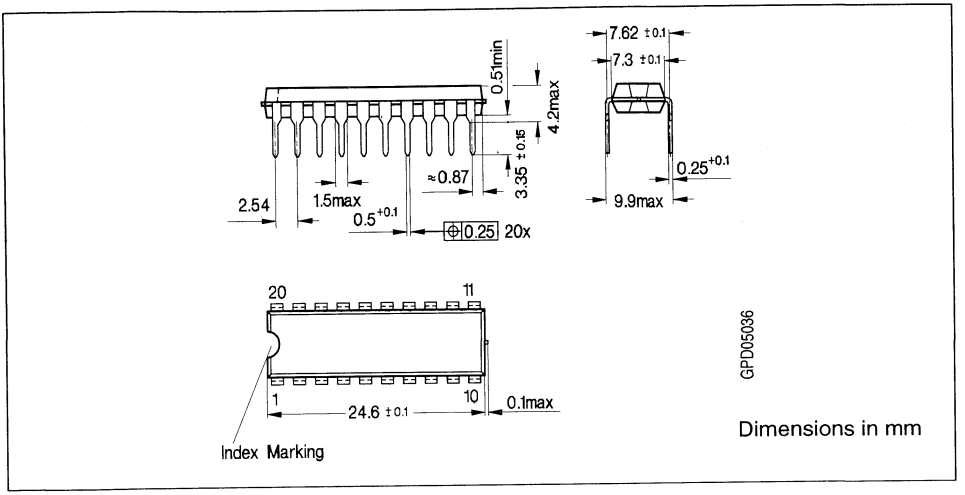


L-DIM-168-1
Module Package
(Double in-line memory module)

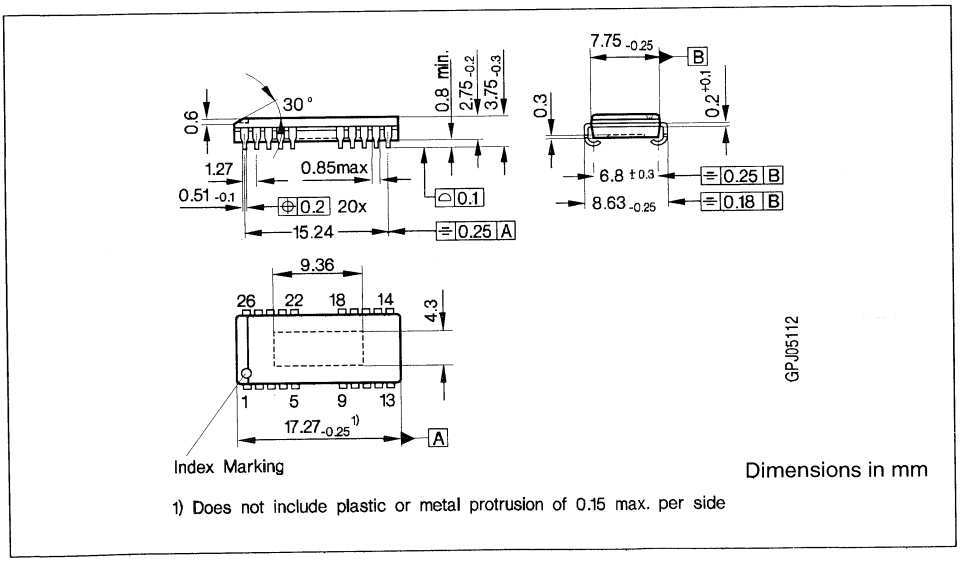


L-DIM-168-2
Module Package
(Double in-line memory module)

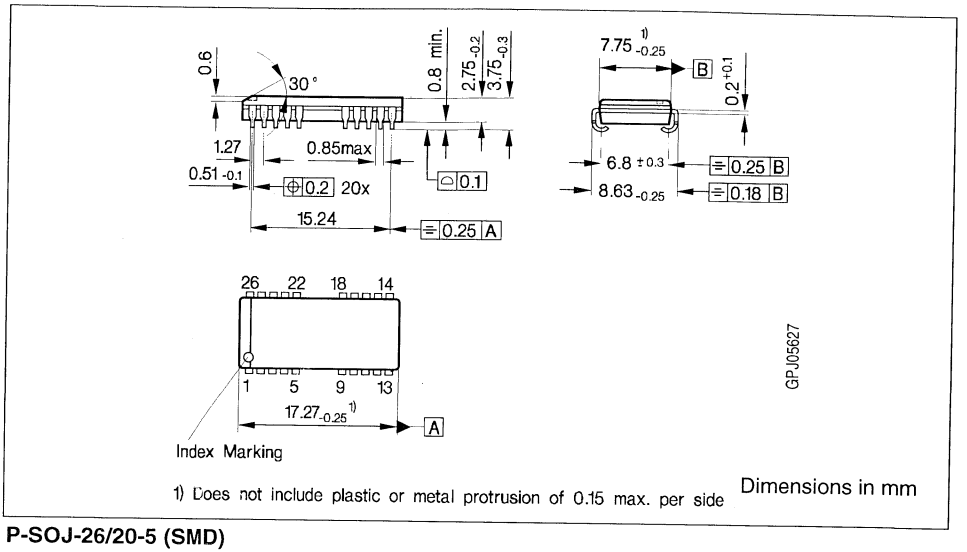
Memory Components



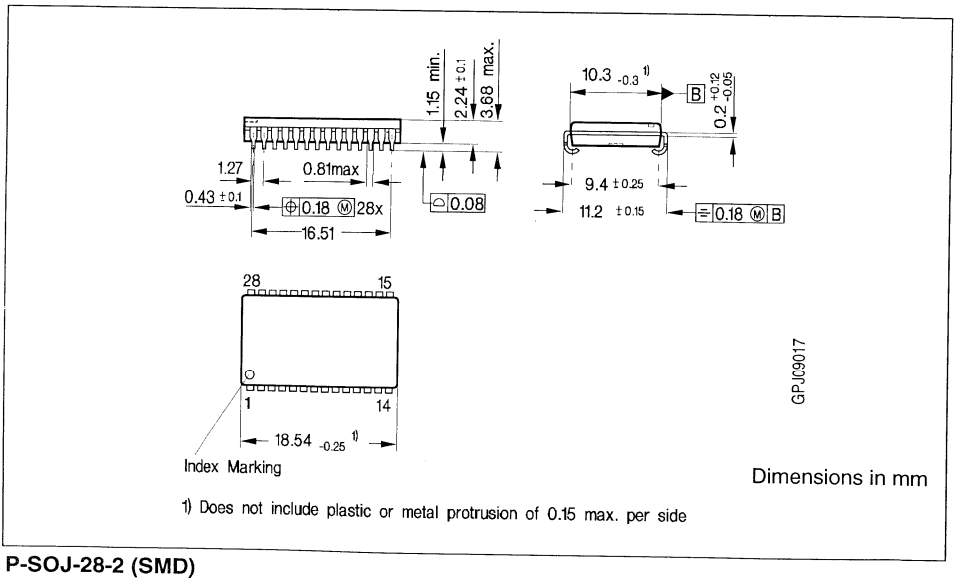
P-DIP-20-2
Plastic Package
(Plastic dual in-line package)



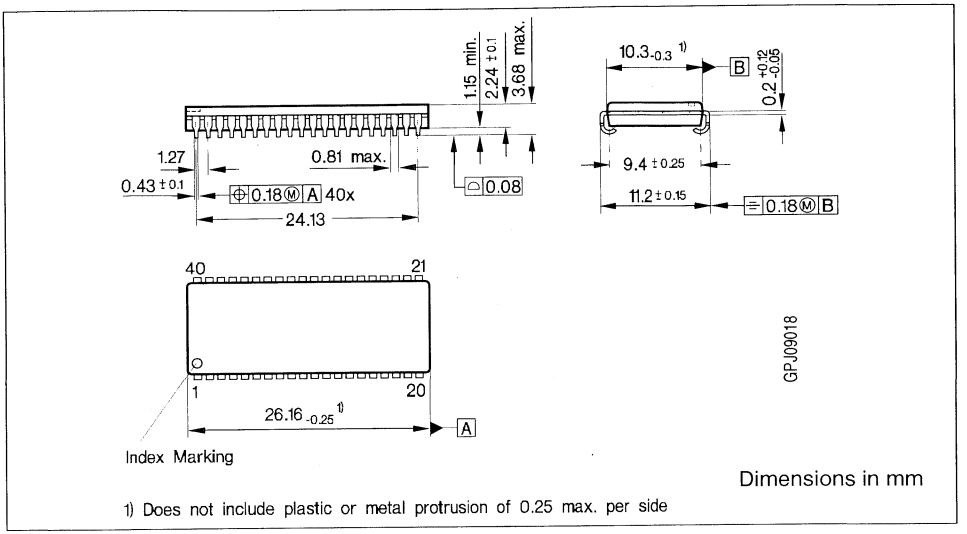
P-SOJ-26/20-1 (SMD)
Plastic Package
(Plastic small outline J-lead)



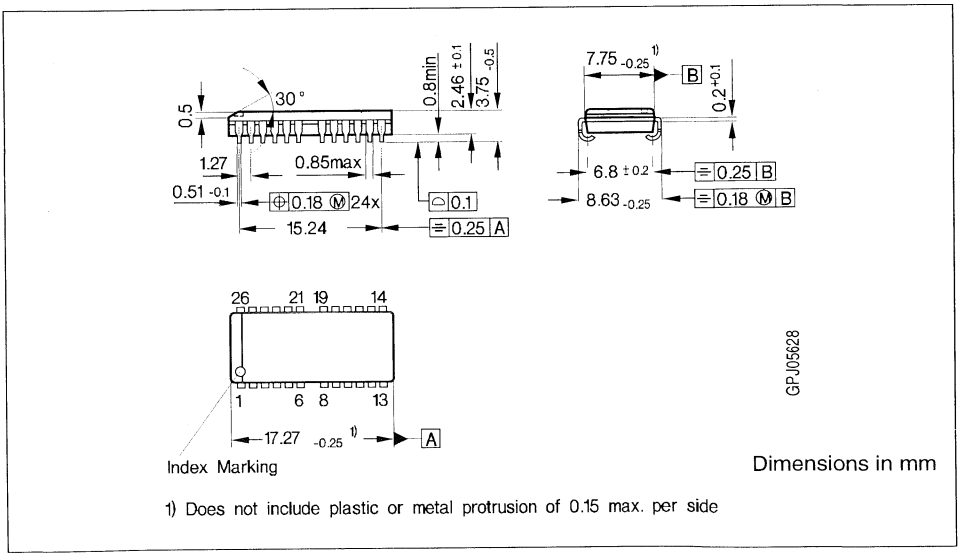
P-SOJ-26/20-5 (SMD)
Plastic Package
(Plastic dual in-line package)



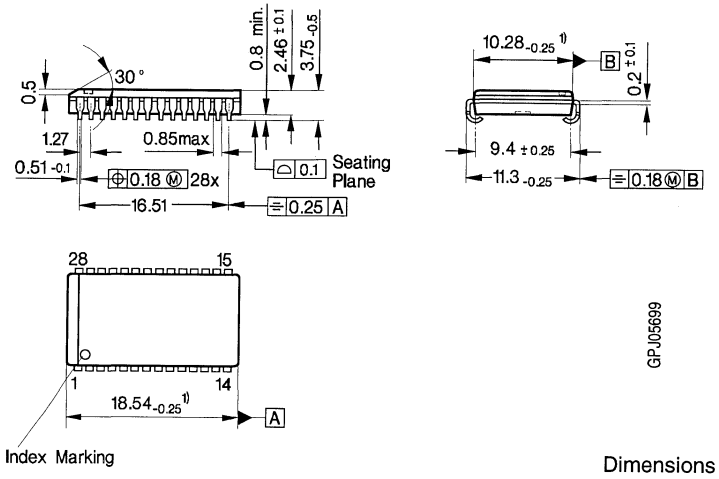
P-SOJ-28-2 (SMD)
Plastic Package
(Plastic small outline J-lead)



P-SOJ-40-1 (SMD)
Plastic Package
(Plastic small outline J-lead)

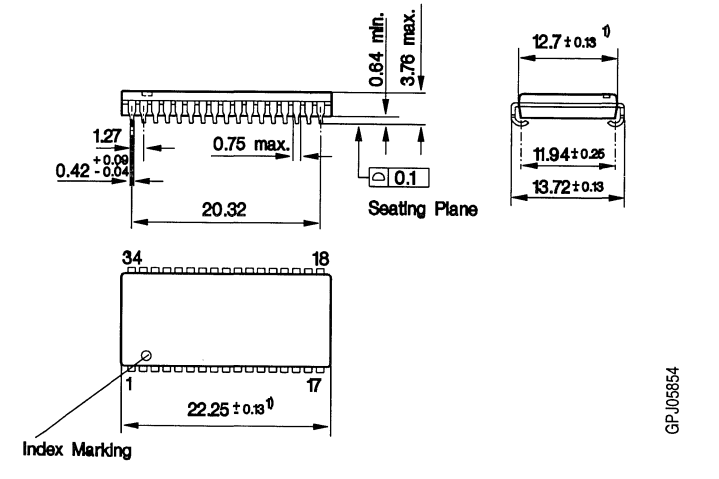


P-SOJ-26/24-1 (300 mil) (SMD)
Plastic Package
(Plastic small outline J-lead)



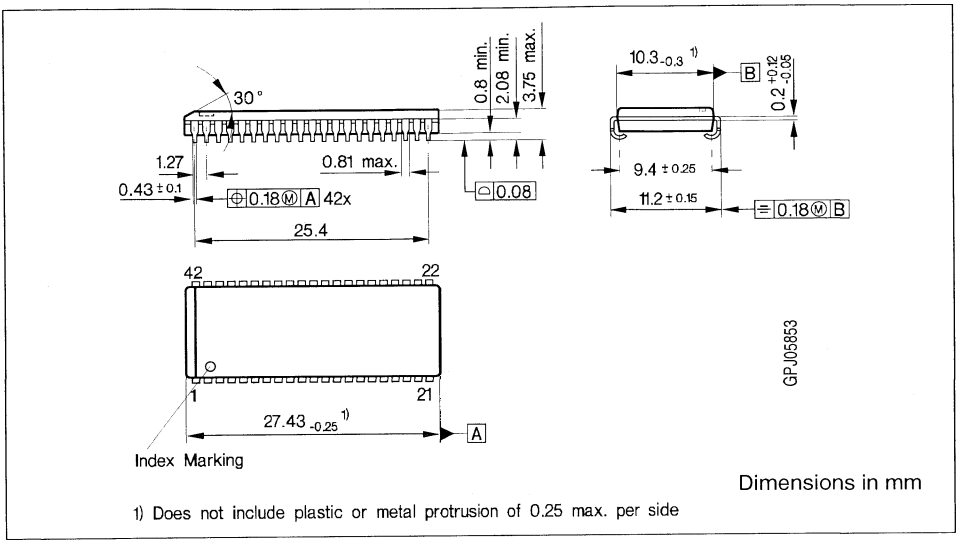
1) Does not include plastic or metal protrusion of 0.15 max. per side

P-SOJ-28-3 (SMD)
Plastic Package

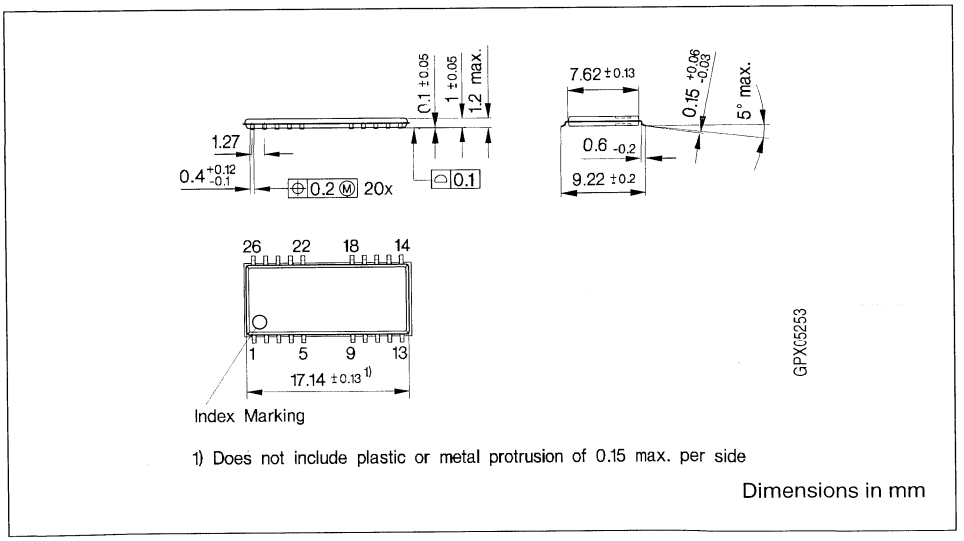


1) Does not include plastic or metal protrusion of 0.15 max. per side

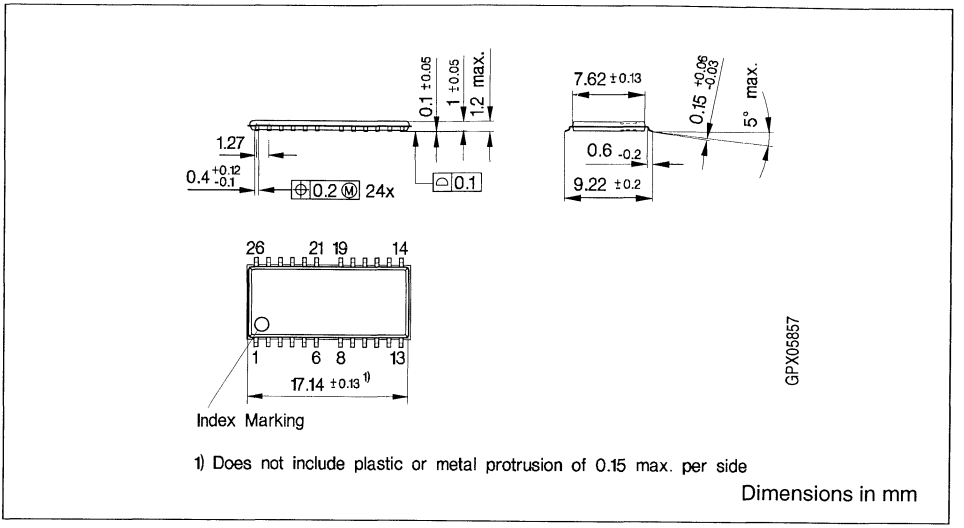
P-SOJ-34-1 (SMD)
Plastic Package



P-SOJ-42-1 (SMD)
Plastic Package
(Plastic small outline J-lead)



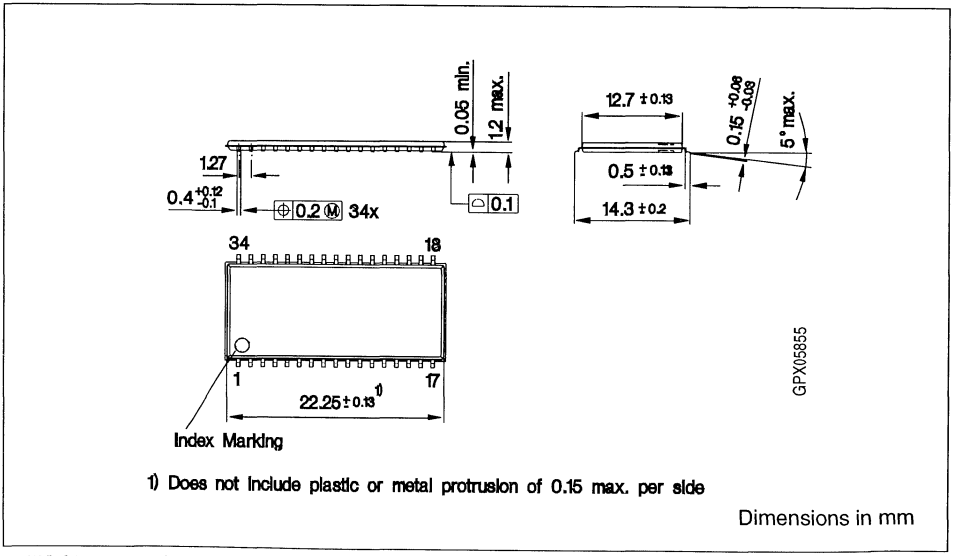
P-TSOPII-26/20-1 (300 mil) (SMD)
Plastic Package
(Thin small outline package)



1) Does not include plastic or metal protrusion of 0.15 max. per side

Dimensions in mm

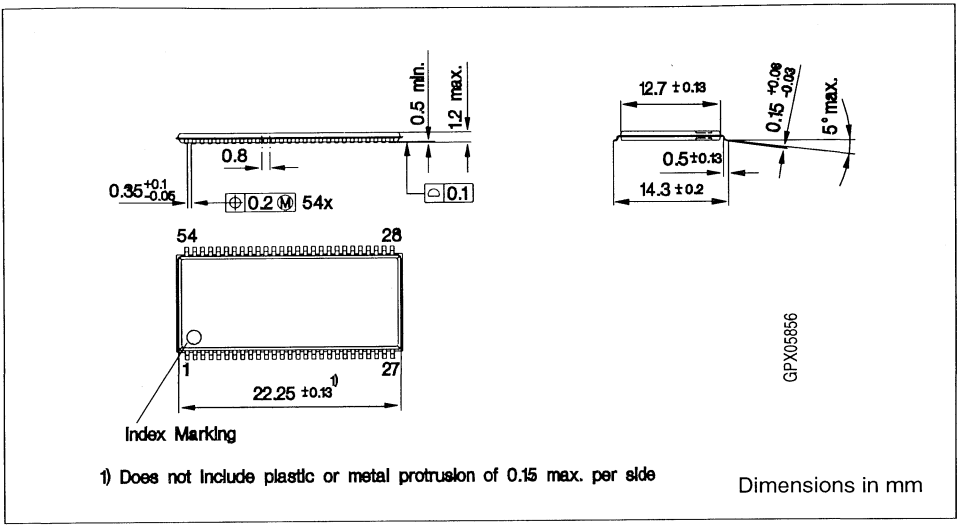
P-TSOPII-26/24-1 (SMD)
Plastic Package
(Thin small outline package)



1) Does not include plastic or metal protrusion of 0.15 max. per side

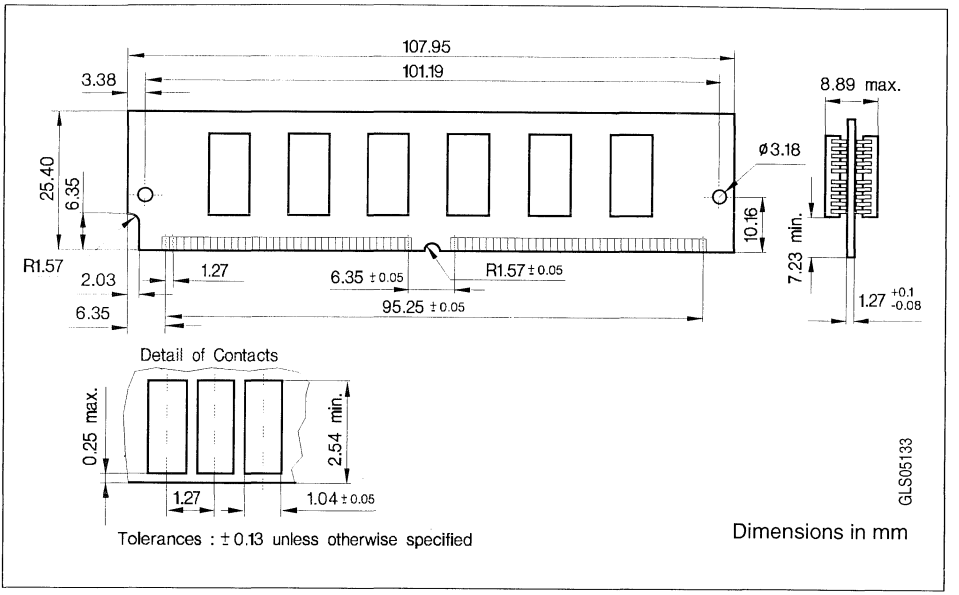
Dimensions in mm

P-TSOPII-34-1 (SMD)
Plastic Package
(Thin small outline package)

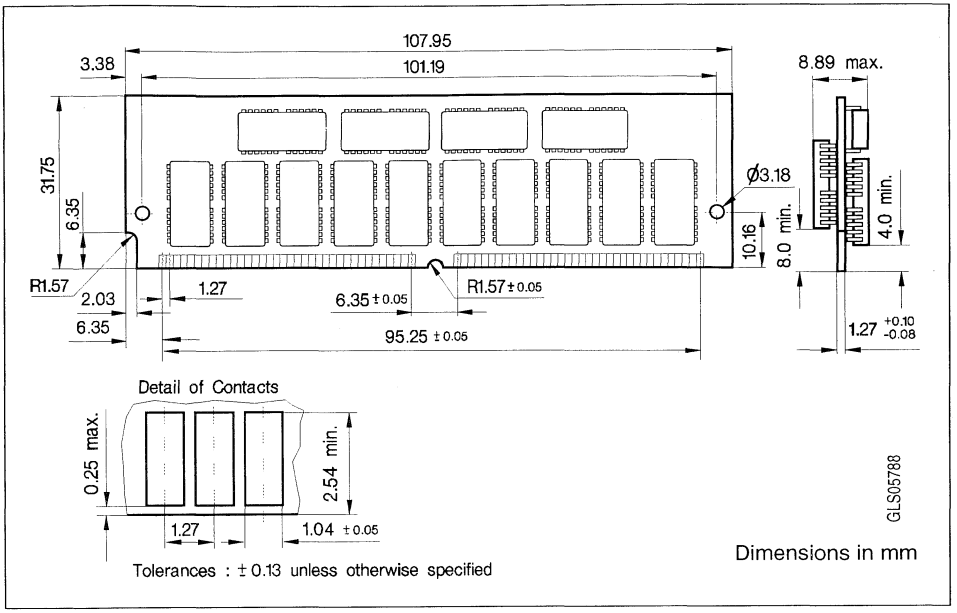


P-TSOPII-54-1 (SMD)
Plastic Package
(Thin small outline package)

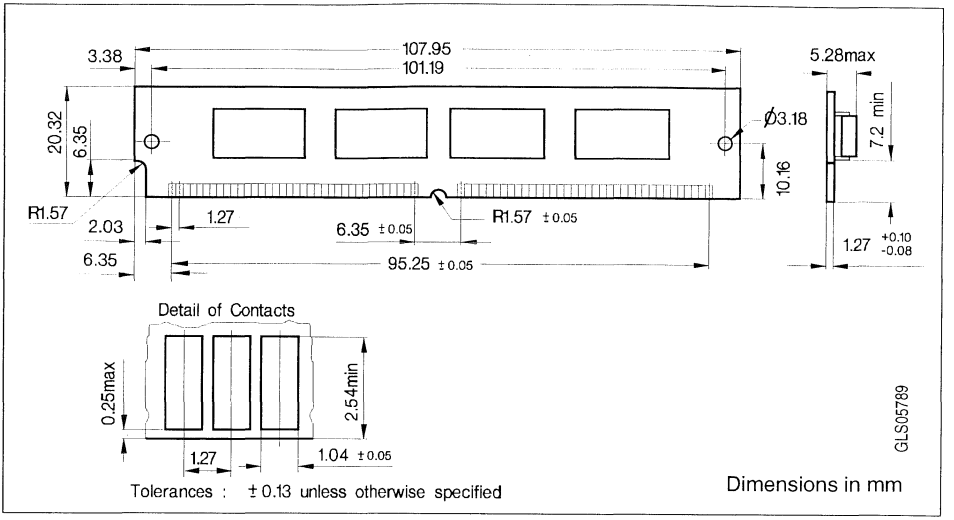
Memory Modules



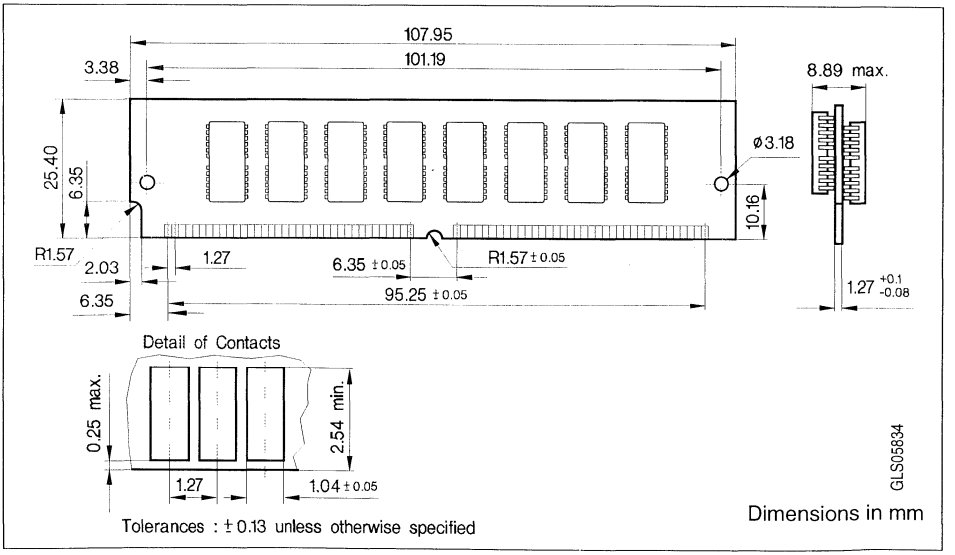
L-SIM-72-3 (Double sided socket type)
Module Package
(Single in-line memory module)



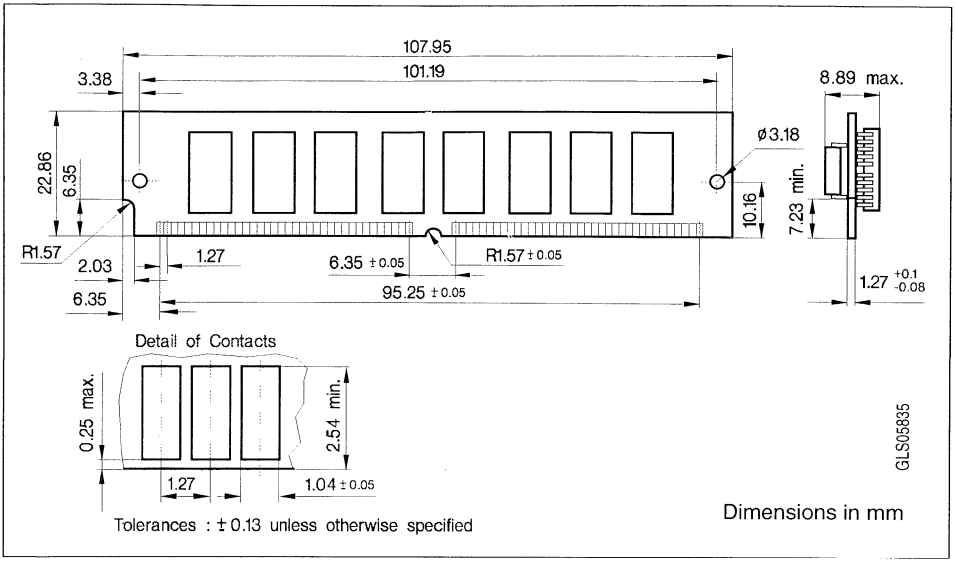
L-SIM-72-8 (Double sided socket type)
Module Package
(Single in-line memory module)



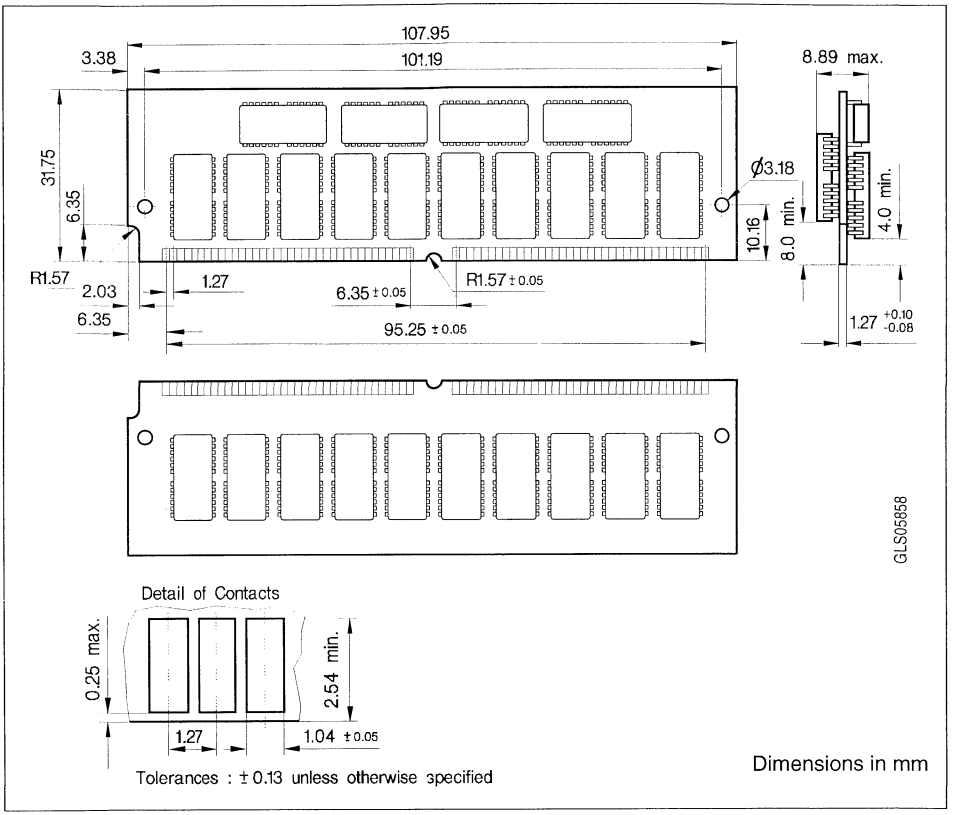
L-SIM-72-9 (Single sided socket type)
Module Package
(Single in-line memory module)



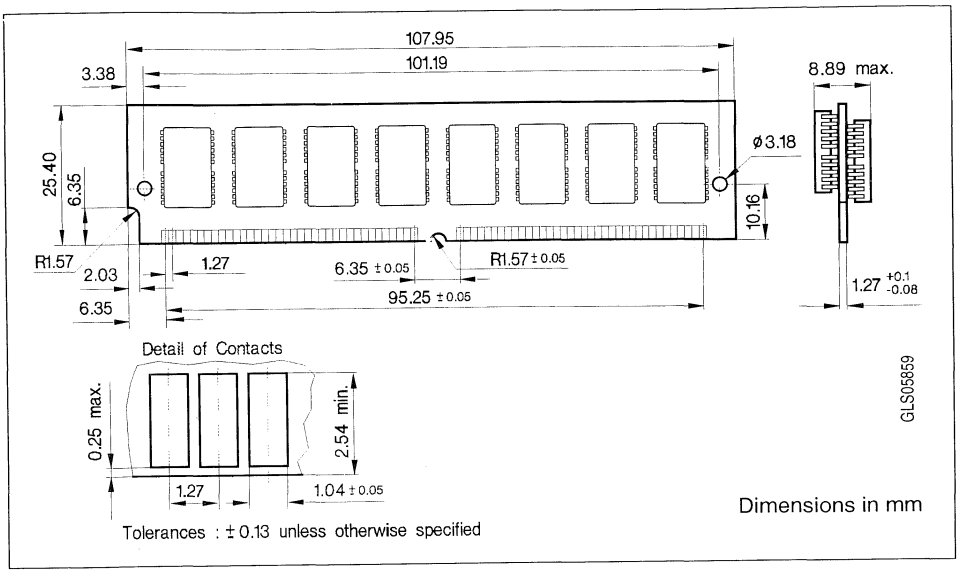
L-SIM-72-11 (Double sided socket type)
Module Package
(Single in-line memory module)



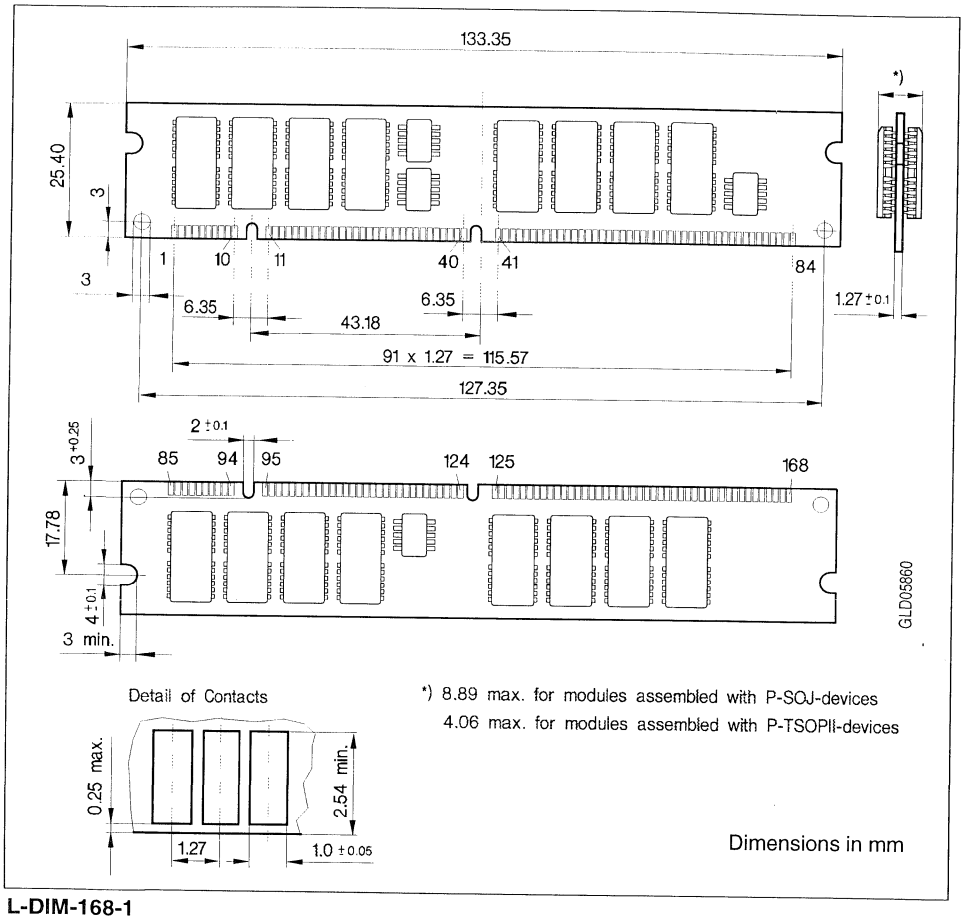
L-SIM-72-12 (Double sided socket type)
Module Package
(Single in-line memory module)



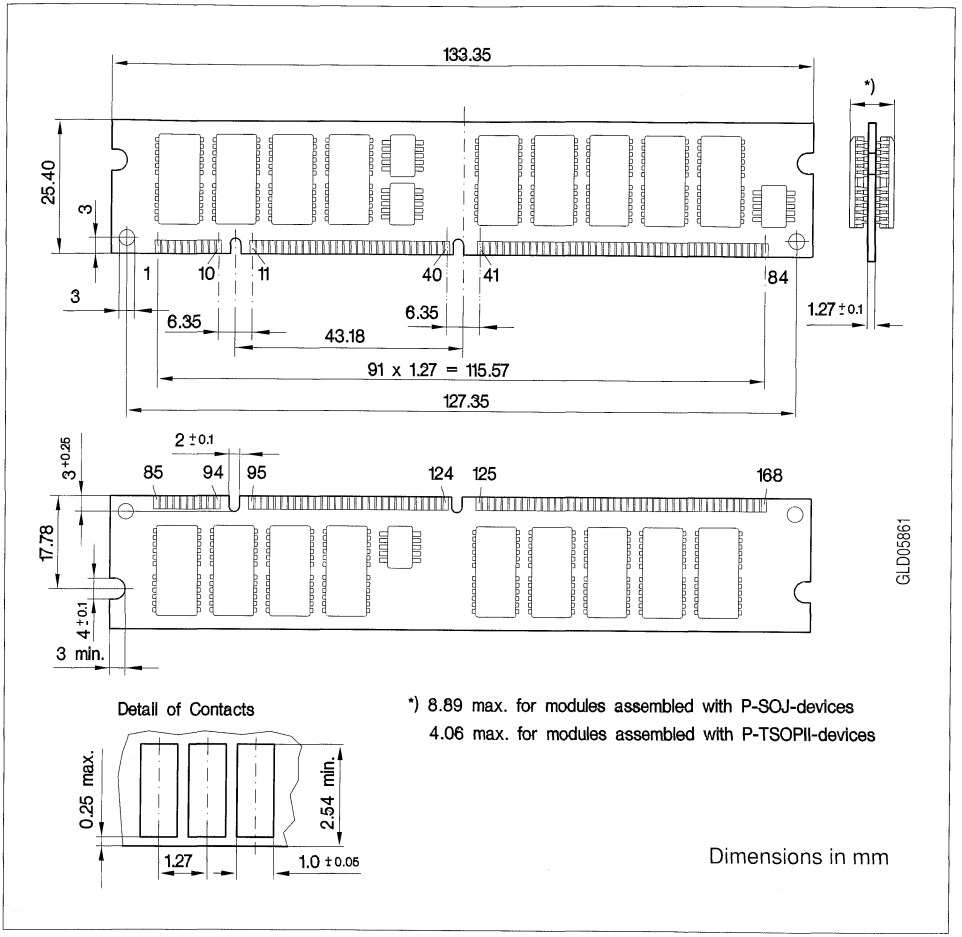
L-SIM-72-14 (Double sided socket type)
Module Package
(Single in-line memory module)



L-SIM-72-15 (Double sided socket type)
Module Package
(Single in-line memory module)



L-DIM-168-1
Module Package
(Double in-line memory module)



L-DIM-168-2
Module Package
(Double in-line memory module)

Summary of Types in Alphanumerical Order
Information on Literature
Semiconductor Group – Addresses

Summary of Types in Alphanumerical Order

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HYB 3116160BSJ-50	on request	403
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HYB 3116160BSJ-70	on request	403
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HYB 3116400BJ-60	on request	223
HYB 3116400BJ-70	on request	223
HYB 3116400BT-50	on request	223
HYB 3116400BT-60	on request	223
HYB 3116400BT-70	on request	223
HYB 3117400BJ-50	on request	249
HYB 3117400BJ-60	on request	249
HYB 3117400BJ-70	on request	249
HYB 3117400BT-50	on request	249
HYB 3117400BT-60	on request	249
HYB 3117400BT-70	on request	249
HYB 3118160BSJ-50	on request	403
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HYB 3118160BSJ-70	on request	403
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HYB 3164800T-60	on request	483

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HYB 3165400J-60	on request	455
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HYB 3165400T-50	on request	455
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HYB 5116165BSJ-60	on request	429
HYB 5116165BSJ-70	on request	429
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HYB 5116400BJ-60	Q67100-Q1050	171
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HYB 5116405BT-60	on request	275
HYB 5116405BT-70	on request	275
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HYB 5116805BJ-70	Q67100-Q1106	329
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HYB 5117800BSJ-60	Q67100-Q1093	303
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HYB 5118160BSJ-60	Q67100-Q1073	355
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HYB 514100BJ-70	Q67100-Q760	77
HYB 514100BJL-50	on request	77
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HYB 514400BJL-60	Q67100-Q1030	99
HYB 514400BJL-70	Q67100-Q762	99
HYB 514400BT-50	Q67100-Q2013	99
HYB 514400BT-60	Q67100-Q749	99
HYB 514400BT-70	Q67100-Q750	99
HYB 514400BTL-50	on request	99
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= SMD

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HYM 721000GS-70	on request	641

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Sprachenschlüssel der Bestellnummern

Englisch	-X-X-7600
Deutsch/Englisch	-X-X-7400

Inhalte der Druckschriften-Arten

Datenbuch (DB)
Sammlung der zu den Produktfamilien gehörenden Datenblätter, zusätzlich allgemeine Hinweise (Verarbeitung, Lagerung, Qualität, Anwendung).

Datenblatt (DA)
Es enthält alle für den Anwender des Halbleiters erforderlichen Angaben.

Produktschrift (PS)
Ausführliche Beschreibung zur Funktion und Anwendung der Halbleiter, z.T. mit Auszügen aus dem Datenblatt.

Themenbuch (TB)
Anwendungsorientierte Themen, z.B.
— Digitales Fernsehen
— Schaltnetzteile
— Anwendungsbeispiele
— Qualität und Zuverlässigkeit
— User's Manual.

Lieferprogramm (LM)
Überblick der lieferbaren Halbleiter. Technische Angaben beschränken sich auf das Notwendigste.

▼ Neuerscheinung

Information on Literature

Language Code of Ordering No.

English	-X-X-7600
German/English	-X-X-7400

Classification of Technical Publications

Data Book (DB)
Collection of Data Sheets belonging to the product families, including general notes (processing, storage, quality, application).

Data Sheet (DA)
Contains all details necessary for the user of the semiconductor.

Product Information (PS)
Detailed description of operation and application of semiconductors, sometimes with extracts from the Data Sheet.

Special Subject Book (TB)
Application-oriented subjects, e.g.
— Digital television
— Switch-mode power supplies
— Application Notes
— Quality and reliability
— User's Manual.

Short Form Catalog (LM)
Overview of semiconductors in production program. Technical details are confined to essentials.

▼ New Edition

Auszug aus unserem
Literaturverzeichnis 10.94

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Ordering No.: B192-H6763-G1-X-7400

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▼ Thermische Eigenschaften von Halbleiter-Gehäusen / Thermal Characteristics of Semiconductor Packages	B192-H6805-X-X-7400	TB	09.94	80	II
▼ Global PartnerChip for Systems on Silicon Bereich Halbleiter	B191-H6801	TB	09.94	20	—
▼ Global PartnerChip for Systems on Silicon Semiconductor Group	B191-H6801-X-X-7600	TB	09.94	20	—
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